FAIRCHILD SEMICONDUCTOR

MOS/CCD DATA BOOK

FAIRCHILD
SEMICONDUCTOR

464 Ellis Street, Mountain View, California 94042

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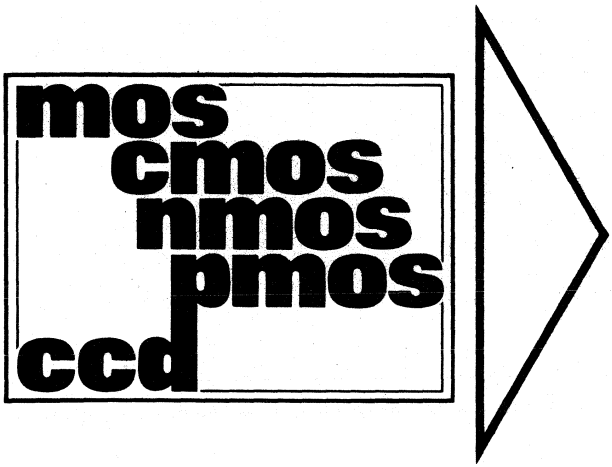
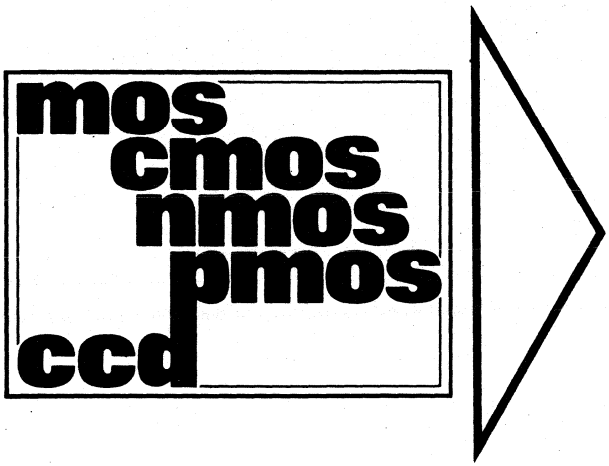


INTRODUCTION

This data book provides complete technical information on Fairchild's full lines of n and p-channel MOS, CMOS, and charge-coupled devices (CCD). These products have important features in common – similar technologies, high packing densities providing low cost per bit, and applications in moderate speed, low power digital systems.

While most of the CMOS circuits are of SSI or MSI (< 200 gates) complexity, MOS and CCD are LSI devices that can provide subsystems from several hundred to tens of thousands of memory or logic elements. Recent MOS technology improvements, refinement of the Isoplanar process in particular, have quadrupled circuit performance in the past few years, at the same time substantially reducing cost. Today, the equipment designer has a wide choice of standard low-cost MOS, CMOS and CCD devices to meet virtually all system requirements from simple logic gates to 16,000-bit memories. Of course, no single design approach covers all needs. However, striking the right balance among these high performance products is the key to successful cost-effective design.

For easy reference to the broad range of MOS, CMOS and CCD products, information within each section of this data book is organized by function. Also, an alphanumeric listing, order information, and sales and distributor locations are included.



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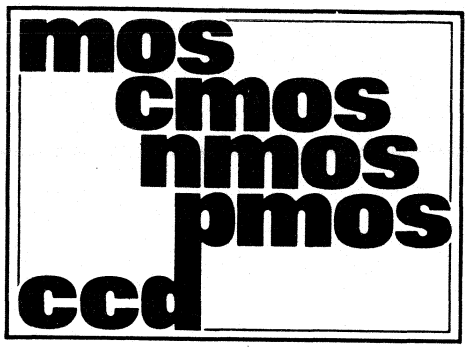


NMOS-PMOS INTRODUCTION

During the past few years, improved MOS technology resulting in increased chip densities and higher yields has caused a significant reduction in the cost of MOS/LSI devices. In digital processing systems that do not require critically high circuit speeds or drive capability, MOS/LSI ensures appreciable cost savings in overall system development and production. MOS/LSI subsystems are now available, ranging in complexity from digital clocks and TV sync generators to large memories for mainframe computers, at a fraction of the cost of other types of circuits. The selection guide included in this section best illustrates the wide range of available products.

Perhaps the most significant new MOS/LSI product is the general-purpose microprocessor, a family of standard building blocks offering the logic versatility previously found only in custom LSI. The F8 Microprocessor consists of five individual modules that can be combined to implement virtually any programmed digital system. For many applications such as data terminals, calculators and appliance controllers, only two chips are required, thus reducing part count from up to 30 devices using other microprocessors and dramatically cutting system cost. More powerful systems can be realized by simply adding more F8 modules. A description of this universal microprocessor is included in this section. Contact the nearest Fairchild sales office or representative for more complete data and design assistance.

SELECTOR GUIDE BY FUNCTION

*Detailed product literature available from local Fairchild sales offices, representatives and distributors.

1103

1024×1 DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION – The 1103 is a fully decoded 1024-word by 1-bit Dynamic Random Access Memory, especially suited for main memory applications. The circuitry is designed for maximum speed and low standby power dissipation. It requires two power supplies and two clocks including the Chip Enable ($\overline{CE}$). Readout is non destructive and the Data Out can be wired-OR for ease of expansion. Exercise of the 32 row addresses is required for refresh.

The 1103 is manufactured with the p-channel Isoplanar process. It is available in 18-pin ceramic Dual In-line Packages in the commercial temperature range.

- **FAST ACCESS (120, 150, 220 AND 300 ns)**
- **LOW POWER**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **WIRED-OR CAPABILITY**
- **18-PIN CERAMIC DUAL IN-LINE PACKAGE**

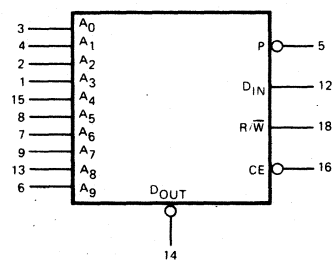
PIN NAMES

A_n	Address Inputs
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{CE}$	Chip Enable
$R/\overline{W}$	Read/Write
P	Precharge

ABSOLUTE MAXIMUM RATINGS

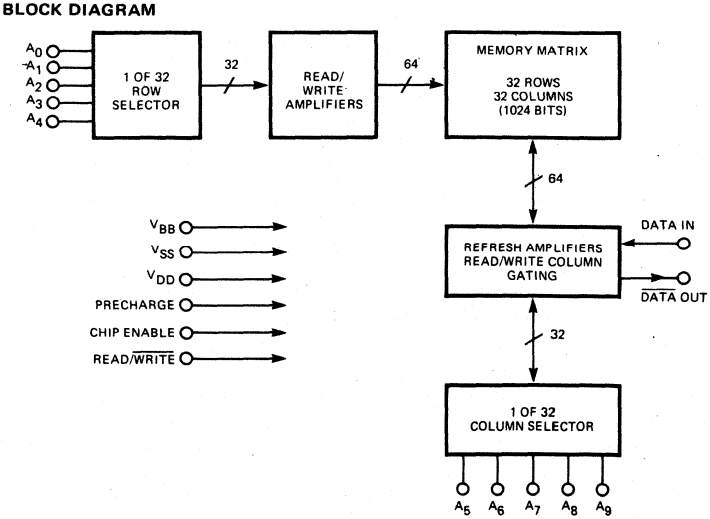
All Pins with Respect to V_{BB}	−25 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature: 1103-1, 1103S, 1103F	0°C to +55°C
1103	0°C to +70°C

LOGIC SYMBOL

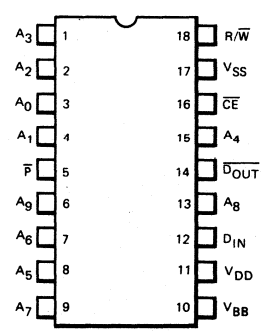


V_{BB} = Pin 10
V_{SS} = Pin 17
V_{DD} = Pin 11

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



DC REQUIREMENTS: 1103F, T_A = 0°C to +55°C; **1103**, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{SS}	Positive Supply Voltage	18	20	15.2	16.8	V	
V_{BB}	Bias Supply Voltage	V_{SS}+3	V_{SS}+4	V_{SS}+3	V_{SS}+4	V	
V_{DD}	Negative Supply Voltage	0	0	0	0	V	
V_{IH1}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−1	V_{SS}+1	V	T_A = Min
V_{IH2}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−0.7	V_{SS}+1	V	T_A = Max
V_{IL1}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−14.2	V	T_A = Min
V_{IL2}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−14.5	V	T_A = Max
V_{IL3}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−14.7	V	T_A = Min
V_{IL4}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−17	V_{SS}−15	V	T_A = Max

*See waveforms input type.

DC CHARACTERISITCS: 1103F, T_A = 0°C to +55°C; **1103**, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{OH1}	Output HIGH Voltage	115	700	60	400	mV	T_A = 25°C, Note 1
V_{OH2}	Output HIGH Voltage	90	700	50	400	mV	T_A = Max Operating Temperature, Note 1
V_{OL}	Output LOW Voltage						Note 2
I_{OH1}	Output HIGH Current	1150	7000	600	4000	μA	T_A = 25°C
I_{OH2}	Output HIGH Current	900	7000	500	4000	μA	T_A = Max Operating Temperature
I_{OL}	Output LOW Current						Note 2
I_{IN}	Input Load Current		10		1.0	μA	
I_{OUT}	Output Leakage Current		10		1.0	μA	
I_{BB}	V_{BB} Supply Current		100		100	μA	
I_{DD1}	Supply Current During t_{PC}		60		56	mA	T_A = 25°C
I_{DD2}	Supply Current During t_{OV}		68.5		59	mA	
I_{DD3}	Supply Current During t_{POV}		11		11	mA	
I_{DD4}	Supply Current During t_{CP}		4.0		4.0	mA	
I_{DDAV}	Average Supply Current		26		25	mA	T_A = 25°C, Note 3

1. Assumes a load resistor of 100 Ω.
2. The output current and voltage for LOW is a function of load resistor.
3. t_{RWC} = min; Precharge width at 50%: 1103F, 60 ns; 1103, 190 ns.

AC REQUIREMENTS: 1103F, T_A = 0°C to +55°C; **1103**, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{REF}	Time Between Refresh		2.0		2.0	ms	
t_{AC}	Address to Chip Enable Set-up Time	30		115		ns	
t_{CA}	Chip Enable to Address Hold Time	10		20		ns	
t_{PC}	Precharge to Chip Enable Delay	35		125		ns	
t_{CP}	Chip Enable to Precharge Delay	40		85		ns	
t_{OVL}	Precharge and Chip Enable Overlap LOW			25	75	ns	
t_{OVH}	Precharge and Chip Enable Overlap HIGH				140	ns	
t_{OVM}	Precharge and Chip Enable Overlap, 50% Points	13	50	45	95	ns	
t_{RC}	Read Cycle	238		480		ns	Note 4
t_{POV}	Precharge to End Chip Enable (Read Cycle)	114	700	165	500	ns	
t_{WC}	Write Cycle	270		580		ns	Note 4
t_{RWC}	Read/Write Cycle	270		580		ns	Note 4
t_{PW}	Precharge to Read/Write Delay	114	700	165	500	ns	
t_{WP}	Read/Write Pulse Width	20		50		ns	
t_W	Read/Write Set-up Time	20		80		ns	
t_{DW}	Data Set-up Time	25		105		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{CW}	Relationship between Chip Enable and Read/Write		5.0		0	ns	

4. Assumes τ_t = 12 ns for 1103F, 20 ns for 1103.

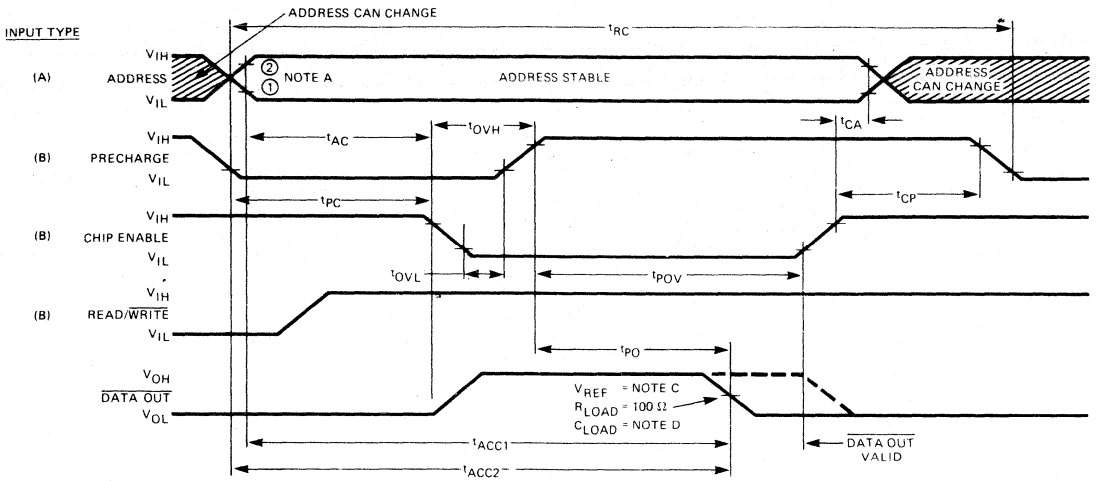
AC CHARACTERISTICS: 1103F, T_A = 0°C to 55°C; 1103, T_A = 0°C to +70°C

SYMBOL	PARAMETER	1103F		1103		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{PO}	End of Precharge to Output Delay (See Waveforms)		65		120	ns	
t_{ACC1}	Address to Output Access		120		300	ns	Note 5
t_{ACC2}	Precharge to Output Access		125		310	ns	Note 6

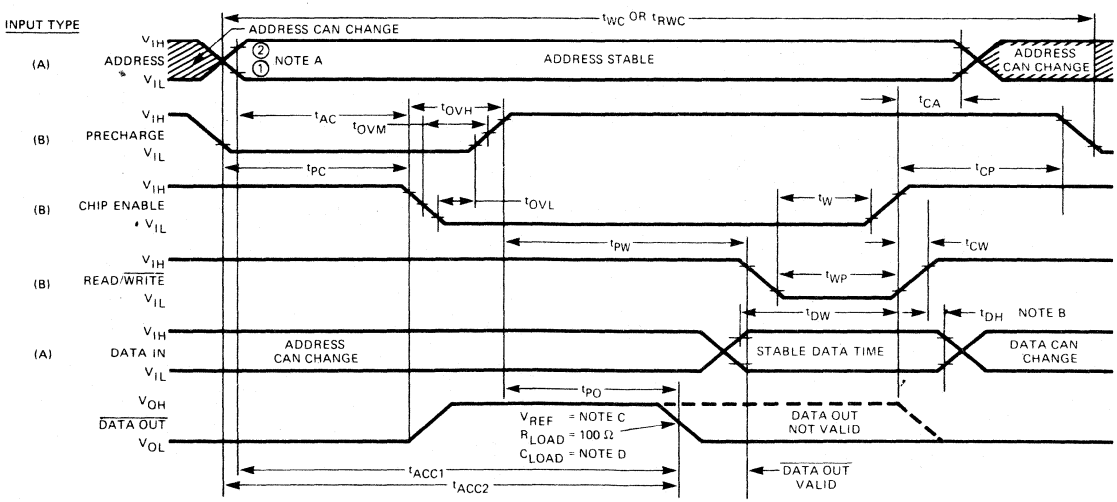
5. $t_{ACC1(max)} = t_{AC}$ min + t_{OVL} min + t_{PO} max + $2\tau_t$.
6. t_{ACC2} (max) = t_{PC} min + t_{OVL} min + t_{PO} max + $2\tau_t$.

WAVEFORMS

READ CYCLE



WRITE CYCLE OR READ/WRITE CYCLE



NOTES:

A. Point ① = V_{DD} +2.0 V
Point ② = V_{SS} − 2.0 V
} τ_t is defined as the transitions between these two points.

B. t_{DH} is referenced to point ② of the rising edge of Chip Enable or Read/$\overline{\text{Write}}$; whichever occurs first.

C. V_{REF} = 80 mV (1103F,1103-1) , 40 mV (1103,1103S)

D. C_{LOAD} = 50 pF (1103F, 1103-1), 100 pF (1103, 1103S)

DC REQUIREMENTS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{SS}	Positive Supply Voltage	18.05	19.95	18.05	19.95	V	
V_{BB}	Bias Supply Voltage	V_{SS}+3	V_{SS}+4	V_{SS}+3	V_{SS}+4	V	
V_{DD}	Negative Supply Voltage	0	0	0	0	V	
V_{IH1}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−1	V_{SS}+1	V	T_A = 0°C
V_{IH2}	Input HIGH Voltage	V_{SS}−1	V_{SS}+1	V_{SS}−0.7	V_{SS}+1	V	T_A = 55°C
V_{IL1}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17	V	T_A = 0°C
V_{IL2}*	Input LOW Voltage (A)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17.3	V	T_A = 55°C
V_{IL3}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17	V	T_A = 0°C
V_{IL4}*	Input LOW Voltage (B)	V_{SS}−20	V_{SS}−18	V_{SS}−20	V_{SS}−17.3	V	T_A = 55°C

*See waveforms input type.

DC CHARACTERISITCS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{OH1}	Output HIGH Voltage	115	700	60	700	mV	T_A = +25°C, Note 1
V_{OH2}	Output HIGH Voltage	90	700	50	700	mV	T_A = 55°C, Note 1
V_{OL}	Output LOW Voltage						Note 2
I_{OH1}	Output HIGH Current	1150	7000	600	7000	μA	T_A = 25°C
I_{OH2}	Output HIGH Current	900	7000	500	7000	μA	T_A = 55°C
I_{OL}	Output LOW Current						Note 2
I_{LI}	Input Load Current		10		10	μA	
I_{LO}	Output Leakage Current		10		10	μA	
I_{BB}	V_{BB} Supply Current		100		100	μA	
I_{DD1}	Supply Current During t_{PC}		60		60	mA	T_A = 25°C
I_{DD2}	Supply Current During t_{OV}		68.5		68.5	mA	
I_{DD3}	Supply Current During t_{POV}		11		11	mA	
I_{DD4}	Supply Current During t_{CP}		4.0		4.0	mA	
I_{DDAV}	Average Supply Current		26		24	mA	T_A = 25°C, Note 7

7. t_{RWC} = min; Precharge width at 50%: 1103-1, 105 ns; 1103S, 95 ns.

AC REQUIREMENTS: 1103-1 and 1103S, T_A = 0°C to +55°C

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{REF}	Time Between Refresh		1.0		1.0	ms	
t_{AC}	Address to Chip Enable Set-up Time	30		70		ns	
t_{CA}	Chip Enable to Address Hold Time	10		20		ns	
t_{PC}	Precharge to Chip Enable Delay	60		70		ns	
t_{CP}	Chip Enable to Precharge Delay	40		50		ns	
t_{OVL}	Precharge and Chip Enable Overlap LOW	5.0	30	5.0	45	ns	
t_{OVH}	Precharge and Chip Enable Overlap HIGH		85		105	ns	
t_{OVM}	Precharge and Chip Enable Overlap, 50% Points	25	50			ns	
t_{RC}	Read Cycle	300		345		ns	τ_t = 20 ns
t_{POV}	Precharge to End Chip Enable (Read Cycle)	115	500	140	500	ns	
t_{WC}	Write Cycle	340		390		ns	τ_t = 20 ns
t_{RWC}	Read/Write Cycle	340		390		ns	τ_t = 20 ns
t_{PW}	Precharge to Read/Write Delay	115	500	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		25		ns	
t_W	Read/Write Set-up Time	20		25		ns	
t_{DW}	Data Set-up Time	40		45		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{CW}	Relationship between Chip Enable and Read/Write		0			ns	

AC CHARACTERISTICS: 1103-1 and 1103S, $T_A = 0°C$ to $+55°C$

SYMBOL	PARAMETER	1103-1		1103S		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{PO}	End of Precharge to Output Delay (See Waveforms)		75		105	ns	
t_{ACC1}	Address to Output Access		150		220	ns	Note 5
t_{ACC2}	Precharge to Output Access		180		220	ns	Note 6

CAPACITANCE CHARACTERISTICS (pF): All unused pins at AC ground; $f_o = 1$ MHz; $V_{BB} = +3.0$ Volts

SYMBOL	CAPACITANCE	1103, 1103-1, 1103S, 1103F		CONDITIONS
		TYP	MAX	
C_{AD}	Address	6.0	8.0	$V_{IN} = V_{SS}$
C_{PR}	Precharge	19	23	$V_{IN} = V_{SS}$
C_{CE}	Chip Enable	15	18	$V_{IN} = V_{SS}$
C_{RW}	Read/Write	15	18	$V_{IN} = V_{SS}$
C_{IN}	Data Input	5.0	7.0	Chip Enable = V_{DD} or V_{SS}; $V_{IN} = V_{SS}$
C_{OUT}	Data Output	3.0	4.0	$V_{OUT} = V_{DD}$

21L02

1024×1 STATIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION – The 21L02 is a 1024-word by 1-bit Static Random Access Memory. It requires a single 5 V power supply, is fully TTL compatible on the inputs and outputs and requires no clocking or refresh. The Chip Select ($\overline{CS}$) provides a 3-state output which allows the outputs to be wired-OR. The 21L02 features a power-down mode during standby operation where the device dissipates a maximum of 32 mW.

The 21L02 is manufactured with the n-channel Isoplanar process. It is available in the 16-pin ceramic Dual In-line Package in the commercial temperature range, 0°C to 70°C.

- **FAST ACCESS TIME (400 ns and 500 ns)**
- **SINGLE +5 V POWER SUPPLY**
- **TTL COMPATIBLE ON INPUTS AND OUTPUT**
- **TOTALLY STATIC – NO CLOCKS OR REFRESH**
- **3-STATE OUTPUT**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **16-PIN CERAMIC DUAL IN-LINE PACKAGE**
- **158 mW P_D GUARANTEED**
- **POWER DOWN STANDBY MODE**

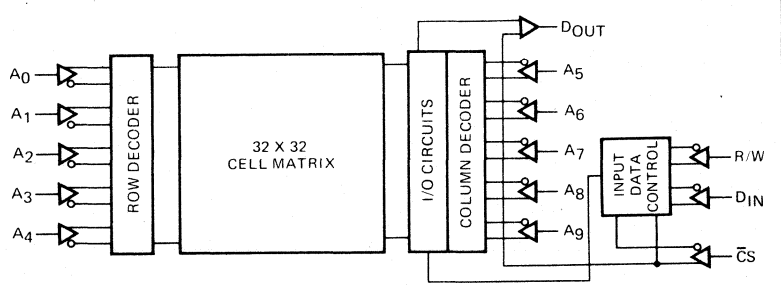
PIN NAMES

A_n	Address Inputs
D_{OUT}	Data Output
D_{IN}	Data Input
$R/\overline{W}$	Read/Write
$\overline{CS}$	Chip Select (active LOW)

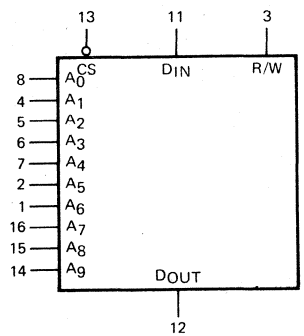
ABSOLUTE MAXIMUM RATINGS

Any Lead with Respect to V_{SS}	-0.5 V to +7.0 V
Storage Temperature	-55°C to +150°C
Operating Temperature	0°C to +70°C

BLOCK DIAGRAM

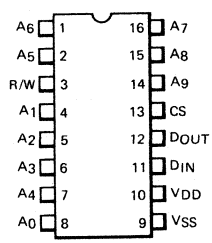


LOGIC SYMBOL



V_{SS} = Pin 8
V_{DD} = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

$\overline{CS}$	$R/\overline{W}$	D_{IN}	D_{OUT}	Comments
H	X	X	*	Chip Deselected
L	L	H	H	Write "1" †
L	L	L	L	Write "0" †
L	H	X	D_n	Read †

X = Don't Care
* = Output High Impedance State
D_n = Data at Addressed Location
† = Chip Selected

FUNCTIONAL DESCRIPTION – The 21L02 is a 1024 x 1 static RAM. When the Chip Select ($\overline{CS}$) goes HIGH, the Read/Write ($R/\overline{W}$) input is disabled and the Data Output (D_{OUT}) is forced into a high impedance state. When Chip Select goes LOW, the Read/Write is enabled.

When $R/\overline{W}$ goes LOW, data from the Data Input (D_{IN}) is written at the location specified by the Address Inputs (A_n). The Data Output will be identical to the Data Input during a write command. When $R/\overline{W}$ goes HIGH, the contents of the addressed location will appear at D_{OUT}. D_{OUT} is not inverted from D_{IN} in the 21L02. (See Truth Table)

DC REQUIREMENTS: $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	21L02B		21L02A		21L02		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	2.0	V_{DD}	2.0	V_{DD}	2.0	V_{DD}	V	V_{DD} = +5 V ± 5%,
V_{IL}	Input LOW Voltage	−0.5	0.8	−0.5	0.8	−0.5	0.8	V	V_{SS} = 0 V
V_{DD}	Power Supply Voltage	4.75	5.25	4.75	5.25	4.75	5.25	V	

DC CHARACTERISTICS: V_{DD} = +5 V ±5%, V_{SS} = 0 V, $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	21L02B		21L02A		21L02		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	2.4		2.4		2.4		V	I_{OH} = −0.2 mA
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	I_{OL} = 3.2 mA
I_{IN}	Input Leakage Current		10		10		10	μA	$V_{IN} = V_{DD}$
I_{OUT}	Output Leakage Current	−10	10	−10	10	−10	10	μA	V_{OUT} = 0 V to V_{DD}, CS = V_{IH}
I_{DD}	Power Supply Current		30		30		30	mA	V_{DD} = 5.25 V, All Inputs HIGH
P_D	Power Dissipation		158		158		158	mW	
POWER DOWN CHARACTERISTICS : $T_A = 0°C$ to $+70°C$									
$I_{DD(PD)}$	Power Supply Current		20		20		20	mA	V_{DD} = 1.6 V
$V_{DD(PD)}$	Power Supply Voltage	1.6		1.6		1.6		V	
t_{CSS}	Chip Select Set-Up Time	100		100		100		ns	See Fig. 3
t_{CSH}	Chip Select Hold Time	100		100		100		ns	See Fig. 3
$V_{\overline{CS}}$	Chip Select Voltage	2.0		2.0		2.0		V	See Fig. 3
V'_{DD}	Power Supply Slew Rate		100		100		100	V/μs	See Fig. 3

AC REQUIREMENTS: $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	21L02B		21L02A		21L02		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{CYC}	Read or Write Cycle Time	400		500		650		ns	V_{DD} = +5 V ± 5%, V_{SS} = 0 V
t_{AW}	Address to Write Time	100		150		200		ns	
t_{WP}	Write Pulse Width	200		250		350		ns	
t_{WR}	Write Recovery Time	50		50		50		ns	
t_{DS}	Data Set-Up Time	150		200		250		ns	
t_{DH}	Data Hold Time	50		50		50		ns	
t_{CW}	Chip Select to Write Time	200		250		350		ns	
t_{WC}	Write to Chip Select Time	50		50		50		ns	

AC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	21L02B		21L02A		21L02		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_A	Read Access Time		400		500		650	ns	V_{DD} = +5 V ± 5%, V_{SS} = 0 V
t_{CO}	Chip Select to Output Time		200		200		250	ns	
t_{OH1}	Data Valid After Address	50		50		50		ns	
t_{OH2}	Previous Data Valid After Chip Deselect	0	150	0	150	0	200	ns	
C_{IN}	Input Capacitance		5		5		5	pF	$T_A = 25°C$, f = 1 MHz
C_{OUT}	Output Capacitance		10		10		10	pF	

WAVEFORMS

READ CYCLE TIMING

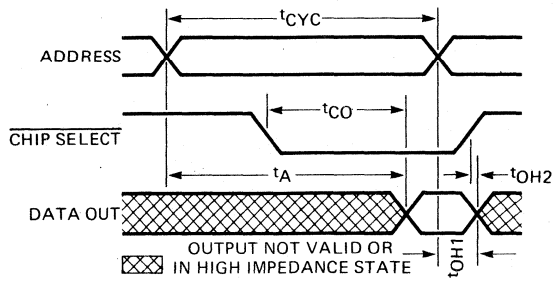


Fig. 1

WRITE CYCLE TIMING

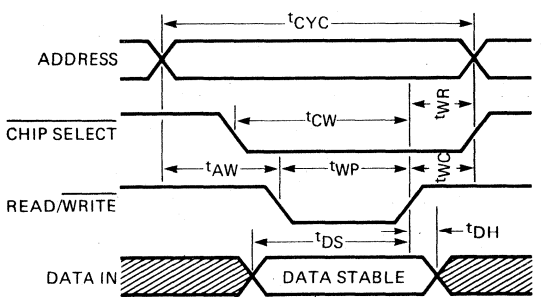


Fig. 2

POWER DOWN MODE TIMING

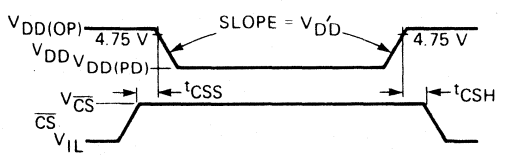


Fig. 3

AC Conditions:
- Input Levels: $V_{IL(MAX)}$ to $V_{IH(MIN)}$
- Input Rise and Fall Times: 10 ns
- Timing Measurement Reference Level: 1.5 V
- Output Load: 2 TTL Gates plus 100 pF

2102

1024×1 STATIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION – The 2102 is a 1024-word by 1-bit Static Random Access Memory. It requires a single 5 V power supply, is fully TTL compatible on the inputs and the output and requires no clocking or refresh. The Chip Select ($\overline{CS}$) provides a 3-state output which allows the outputs to be wired-OR.

The 2102 is manufactured with the n-channel Isoplanar process. It is available in the 16-pin ceramic Dual In-line Package in either commercial, limited military or military temperature ranges.

- **FAST ACCESS TIME (350 ns and 450 ns)**
- **SINGLE +5 V POWER SUPPLY**
- **TTL COMPATIBLE ON INPUTS AND OUTPUT**
- **TOTALLY STATIC – NO CLOCKS OR REFRESH**
- **3-STATE OUTPUT**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **16-PIN CERAMIC DUAL IN-LINE PACKAGE**

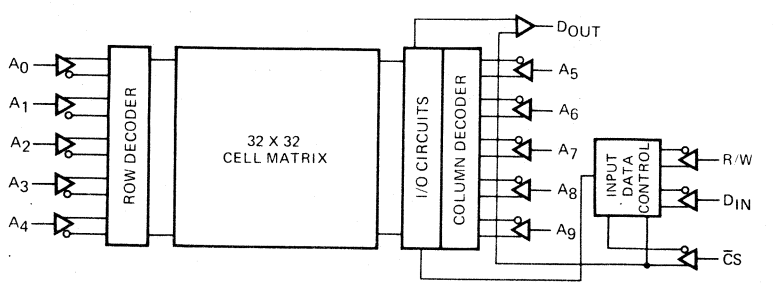
PIN NAMES

A_n	Address Inputs
D_{OUT}	Data Output
D_{IN}	Data Input
$R/\overline{W}$	Read/Write
$\overline{CS}$	Chip Select (active LOW)

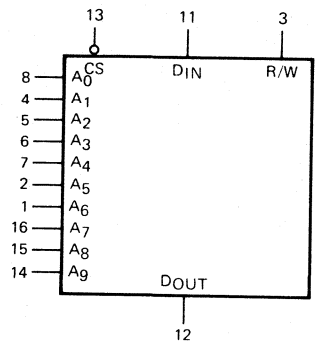
ABSOLUTE MAXIMUM RATINGS

Any Lead with Respect to V_{SS}	−0.5 V to +7.0 V
Storage Temperature	−55°C to +150°C
Operating Temperature DC	0°C to +70°C
DL	−55°C to +85°C
DM	−55°C to +125°C

BLOCK DIAGRAM

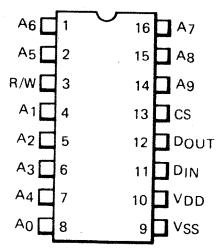


LOGIC SYMBOL



V_{SS} = Pin 9
V_{DD} = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

$\overline{CS}$	$R/\overline{W}$	D_{IN}	D_{OUT}	Comments
H	X	X	*	Chip Deselected
L	L	H	H	Write "1" †
L	L	L	L	Write "0" †
L	H	X	D_n	Read †

X = Don't Care
* = Output High Impedance State
D_n = Data at Addressed Location
† = Chip Selected

FUNCTIONAL DESCRIPTION – The 2102 is a 1024 x 1 static RAM. When the Chip Select ($\overline{CS}$) goes HIGH, the Read/Write ($R/\overline{W}$) input is disabled and the Data Output (D_{OUT}) is forced into a high impedance state. When Chip Select goes LOW, the Read / Write is enabled.

When $R/\overline{W}$ goes LOW, data from the Data Input (D_{IN}) is written at the location specified by the Address Inputs (A_n). The Data Output will be identical to the Data Input during a write command. When $R/\overline{W}$ goes HIGH, the contents of the addressed location will appear at D_{OUT}. D_{OUT} is not inverted from D_{IN} in the 2102. (See Truth Table)

DC REQUIREMENTS: DC: $T_A = 0°C$ to $+70°C$; DL: $T_A = -55°C$ to $+85°C$; DM: $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	DC		DL		DM		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	2.2	V_{DD}	2.0	V_{DD}	2.0	V_{DD}	V	
V_{IL}	Input LOW Voltage	-0.5	0.65	-0.5	0.8	-0.5	0.8	V	
V_{DD}	Power Supply Voltage	4.75	5.25	4.5	5.5	4.5	5.5	V	

DC CHARACTERISTICS: $V_{SS} = 0$ V; DC: $V_{DD} = 5.0$ V ± 5%, $T_A = 0°C$ to $+70°C$; DL: $V_{DD} = 5.0$ V ± 10%, $T_A = -55°C$ to $+85°C$; DM: $V_{DD} = 5.0$ V ± 10%, $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	DC		DL		DM		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	2.2		2.2		2.2		V	$I_{OH} = -100\ \mu A$
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	$I_{OL} = 2.1$ mA
I_{IN}	Input Leakage Current		10		10		10	μA	$V_{IN} = V_{DD}$
I_{OUT}	Output Leakage Current	-10	10	-10	10		10	μA	$V_{OUT} = 0$ V to V_{DD}, $\overline{CS} = V_{IH}$
I_{DD}	Power Supply Current		50		70		70	mA	

AC REQUIREMENTS: DC: $T_A = 0°C$ to $+70°C$; DL: $T_A = -55°C$ to $+85°C$; DM: $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	2102F DC, DL, DM	2102-1 DC, DL, DM	2102-2 DC, DL, DM	2102 DC	UNITS	CONDITIONS
		MIN	MIN	MIN	MIN		
t_{CYC}	Read or Write Cycle Time	350	450	650	1000	ns	$V_{SS} = 0$ V $V_{DD} = +5.0$ V ± 5% For DL, DM: $V_{DD} = 5.0$ V ± 10%
t_{AW}	Address to Write Time	100	150	200	200	ns	
t_{WP}	Write Pulse Width	170	200	350	550	ns	
t_{WR}	Write Recovery Time	50	50	50	50	ns	
t_{DS}	Data Set-up Time	170	200	350	550	ns	
t_{DH}	Data Hold Time	50	50	50	50	ns	
t_{CW}	Chip Select to Write Time	200	250	400	600	ns	
t_{WC}	Write to Chip Select Time	50	50	50	50	ns	

AC CHARACTERISTICS: DC: $T_A = 0°C$ to $+70°C$; DL: $T_A = -55°C$ to $+85°C$; DM: $T_A = -55°C$ to $+125°C$

SYMBOL	PARAMETER	2102F DC, DL, DM		2102-1 DC, DL, DM		2102-2 DC, DL, DM		2102 DC		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_A	Read Access Time		350		450		650		1000	ns	$V_{SS} = 0$ V $V_{DD} = +5.0$ V ± 5%, For DL, DM: $V_{DD} = 5.0$ V ± 10%,
t_{CO}	Chip Select to Output Time		180		200		400		500	ns	
t_{OH1}	Data Valid After Address	50		50		50		50		ns	
t_{OH2}	Previous Data Valid After Chip Deselect	0		0		0		0		ns	
C_{IN}	Input Capacitance		5		5		5		5		$V_{IN} = 0$ V, $V_{SS} = 0$ V, f = 1 MHz, $T_A = 25°C$
C_{OUT}	Output Capacitance		10		10		10		10		

WAVEFORMS

READ CYCLE TIMING

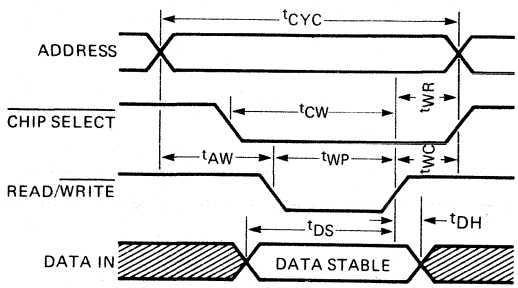


Fig. 1

WRITE CYCLE TIMING

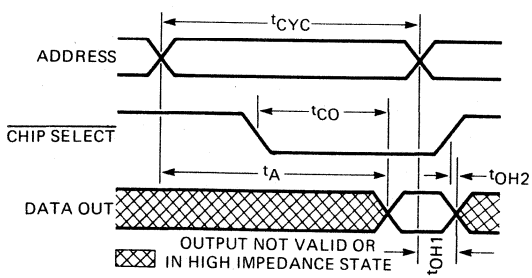


Fig. 2

AC CONDITIONS:

Input Levels: V_{IL} MAX to V_{IH} MIN
Input Rise and Fall Times: 10 ns
Timing Measurement Reference Level: 1.5 V
Output Load: 1 TTL Gate + 100 pF

3257

64 × 5 × 7 CHARACTER GENERATOR

GENERAL DESCRIPTION – The 3257 is a Character Generator designed to display 64 characters in a 5 x 7 font. An on chip column select counter sequences through the five columns of each character. The seven output buffers will each drive one TTL/DTL load directly at a 1 MHz input address rate making the 3257 an ideal device for vertical scan displays. The chip enable allows wired-OR capability if more than 64 characters are required.

- **PROGRAMMABLE WITH A CUSTOM CHARACTER FONT**
- **STANDARD PRODUCT ASCII ENCODED**
- **DIRECT INTERFACING WITH TTL/DTL**
- **WIRED - OR CAPABILITY**

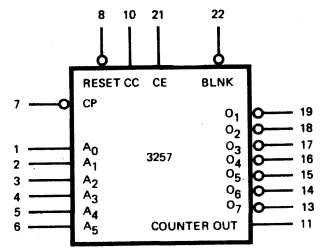
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65° C to +150° C
Operating Temperature	0° C to +70° C
Voltage on any Pin Relative to V_{SS}	−20 V to +0.3 V

APPLICATIONS:

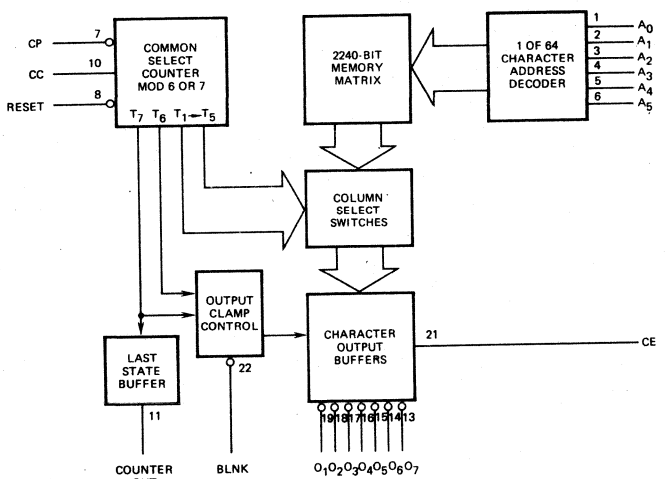
CRT Displays
Billboard Displays
LED Matrix Displays

LOGIC SYMBOL

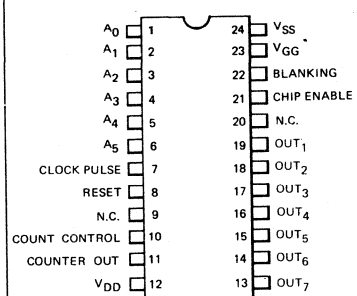


V_{SS} = Pin 24
V_{GG} = Pin 23
V_{DD} = Pin 12

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Connection
A_n = Address Inputs

FUNCTIONAL DESCRIPTION – A Reset pulse (~GND) is required to set the counter to the last state. A 6-bit binary word presented to the character address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the first column of the character is available the next clock time after Reset returns HIGH ($\sim V_{SS}$). The remaining four columns are sequentially selected by the next four states of the counter. The last state of the counter clamps the outputs HIGH ($\sim V_{SS}$) to provide 1 or 2 space blanking between characters (Count Control $\sim V_{SS} \Rightarrow$ MOD 7, Count Control ~ GND $\Rightarrow$ MOD 6). When the last state (6th or 7th) of the counter is reached, the Counter Output goes HIGH ($\sim V_{SS}$). When Chip Enable goes HIGH ($\sim V_{SS}$), the chip is activated while a LOW (~ GND) at this lead floats the outputs to allow common output bussing. A LOW (~ GND) on the Blanking input pulls the outputs HIGH ($\sim V_{SS}$), providing blanking independent of the counter state or the character address.

DC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to +70°C

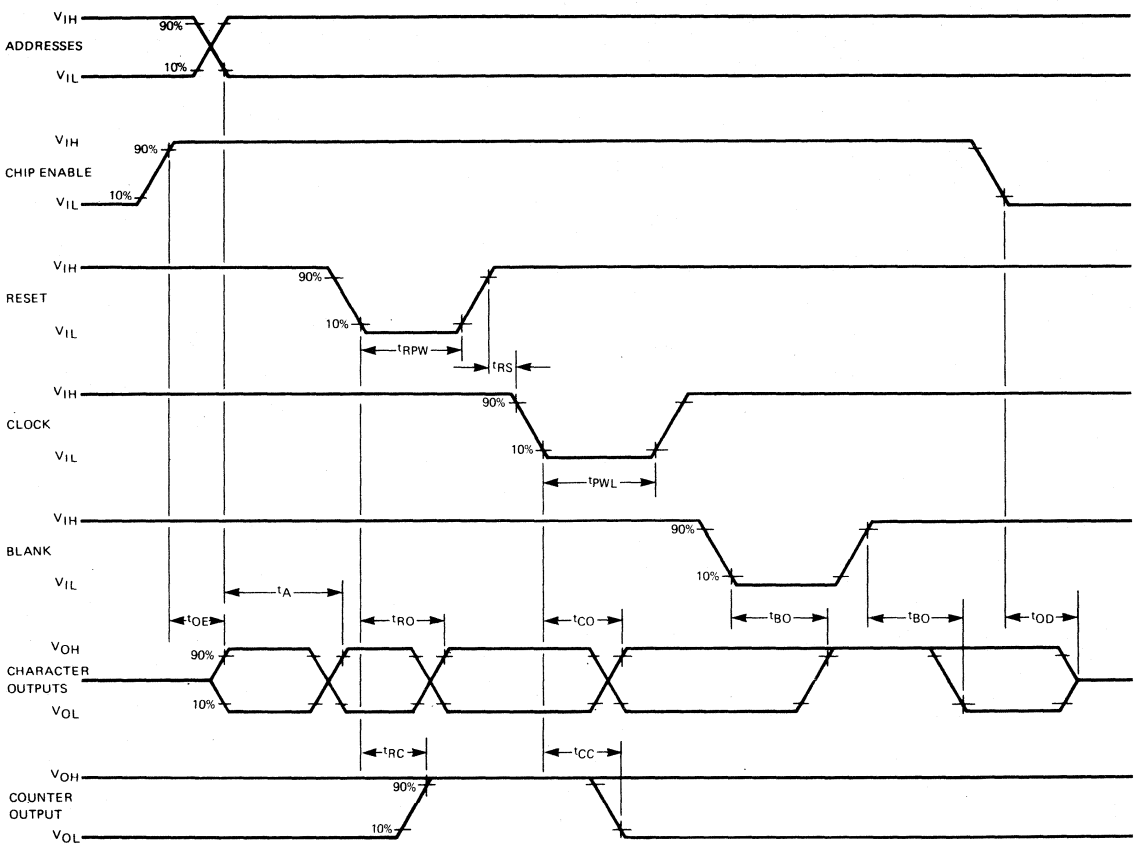
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	$V_{SS}-1$	V_{SS}	V	Note 1
V_{IL}	Input LOW Voltage	V_{GG}	0.8	V	Note 1
V_{OH}	Output HIGH Voltage	$V_{SS}-0.5$	V_{SS}	V	I_{OH} = −10 μA
		2.4	V_{SS}	V	I_{OH} = −0.5 mA
V_{OL}	Output LOW Voltage	0	0.4	V	I_{OL} = 1.6 mA
I_{IN}	Input Leakage Current		−1.0	μA	V_{SS} = 0 V, V_{IN} = −18 V, Note 1
I_{OUT}	Output Leakage Current		1.0	μA	V_{SS} = 0 V, V_{OUT} = −6 V, Note 2
I_{SS}	V_{SS} Current		40	mA	V_{SS} = 5.25 V, V_{GG} = −12.6 V Outputs Open
P_D	Power Dissipation		715	mW	

AC CHARACTERISTICS: V_{SS} = +5 V ±0.25 V, V_{GG} = −12 V ±0.6 V, V_{DD} = 0 V, C_L = 10 pF, T_A = 0°C to +70°C

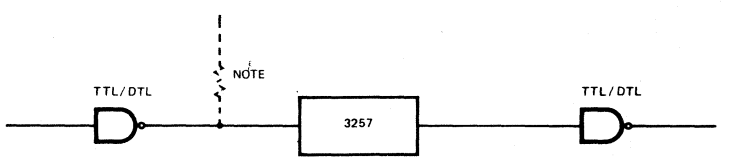
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
f	Clock Frequency	DC	1.0	MHz	
t_{PWL}	Clock Pulse Width LOW	500		ns	
t_r, t_f	Clock Rise & Fall Time (10%-90%)		2.0	μs	
t_{RPW}	Reset Pulse Width	500		ns	
t_{RS}	Reset to Clock Set Up Time	100		ns	
t_A	Character Address to Output Access Time		1000	ns	Notes 4 & 5
t_{CO}	Clock to Output Access Time		1000	ns	Notes 4 & 5
t_{RO}	Reset to Output Time Delay		600	ns	Notes 4 & 5
t_{BO}	Blanking to Output Time Delay		1000	ns	Notes 4 & 5
t_{CC}	Clock to Counter Output Time Delay		500	ns	Notes 4 & 5
t_{RC}	Reset to Counter Output Time Delay		500	ns	Notes 4 & 5
t_{OE}	Output Enable Delay Time		600	ns	Notes 4 & 5
t_{OD}	Output Disable Delay Time		600	ns	Notes 4 & 5
C_{IN}	Input Capacitance		1.0	pF	f = 1.0 MHz, 0 V Bias Note 1

NOTES:
1. Inputs include Addresses, Count Control, Clock and Reset.
2. Chip Enable = LOW.
3. $I_{SS} = -I_{GG}$ (V_{GG} Supply Current).
4. AC Output LOW level is defined as 0.4 V @ 1.6 mA, current sinking (i.e., 1 TTL load).
5. AC Output HIGH level is defined as 2.4 V @ −40 μA, current sourcing (i.e., 1 TTL load).

TIMING DIAGRAM

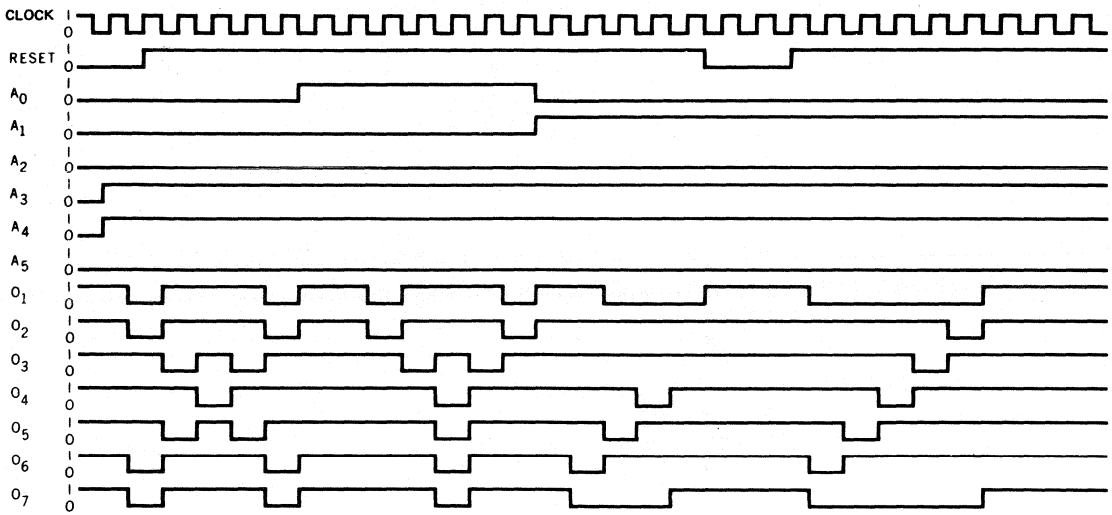


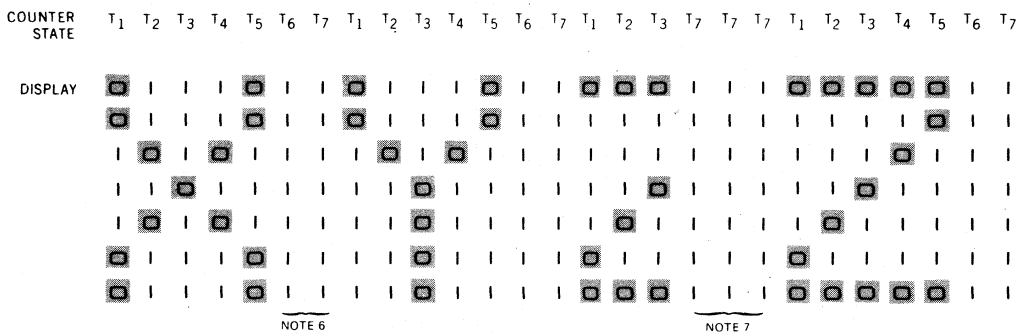
INTERFACING



Note: Directly compatible at outputs with TTL/DTL. Inputs directly compatible with DTL. When being driven by TTL, no pullup resistor needed if TTL output swings to (V_{SS} −1) volts.

TYPICAL FUNCTIONAL TIMING DIAGRAM



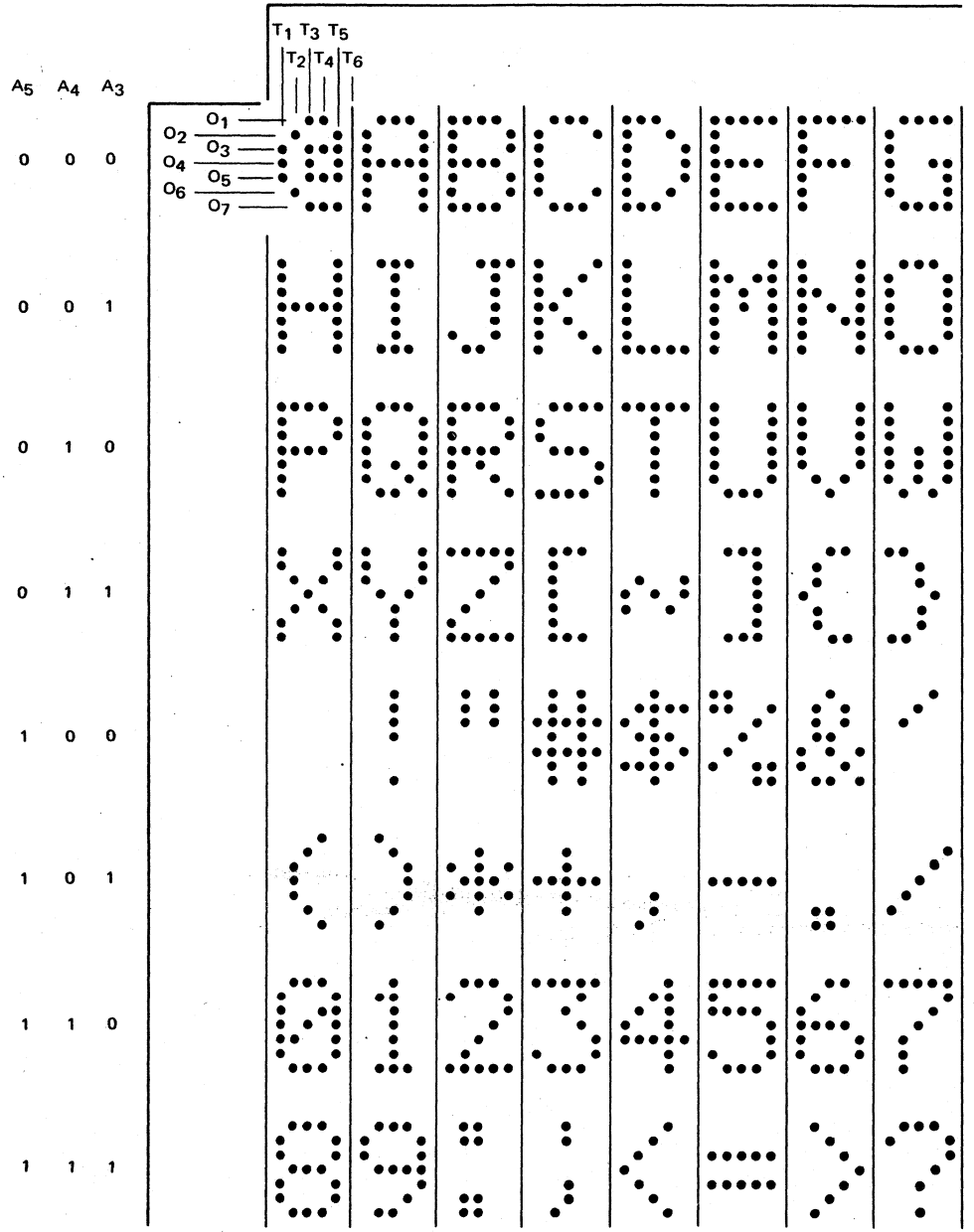


NOTES:
6. Last two counter states (count mode control = HIGH ⇒ MOD 7) provide blanking.
7. Counter is Reset to the last state.

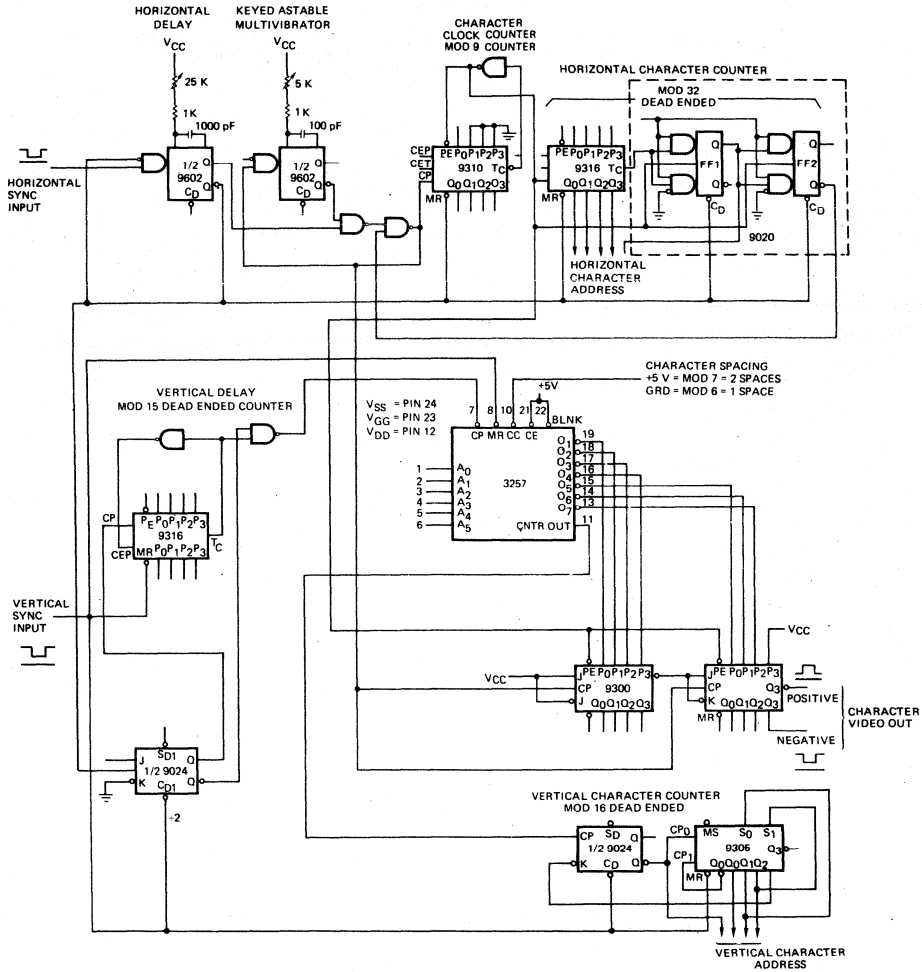
3257A – STANDARD ASCII CHARACTER FONT

COUNT MODE CONTROL ≅ GND ⇒ MOD 6

A_0	0	1	0	1	0	1	0	1
A_1	0	0	1	1	0	0	1	1
A_2	0	0	0	0	1	1	1	1



TYPICAL VERTICAL RASTER SCAN APPLICATION



NOTE:
Horizontal and vertical are referred to as in a standard TV type raster.
16 characters per line, 32 character lines in system.
Each character 10 raster lines wide.

CUSTOM FONT ORDERING INFORMATION

Additional patterns may be made available upon request. The 3257 is programmed on IBM cards or IBM forms in the coding format shown below:

A logic "1" = A more positive voltage nominally +5 V
A logic "0" = A more negative voltage nominally 0 V
The character "dots" are defined as logic "0"

6, 7, 8, 9, 10, 11	Character address input code. The most significant bit (A5) is in column 11.
22, 23, 24, 25, 26, 27, 28	The first column of the character addressed. The most significant bit (07) is in Column 28.
30, 31, 32, 33, 34, 35, 36	The next column of the character addressed. The most significant bit (07) is in Column 36.
38, 39, 40, 41, 42, 43, 44	The next column of the character addressed. The most significant bit (07) is in Column 44.
46, 47, 48, 49, 50, 51, 52	The next column of the character addressed. The most significant bit (07) is in Column 52.
54, 55, 56, 57, 58, 59, 60	The last column of the character addressed. The most significant bit (07) is in Column 60.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential and may be used for card identification purpose.

3258

64 × 7 × 5 CHARACTER GENERATOR

GENERAL DESCRIPTION — The 3258 is a Character Generator designed to display 64 characters in a 5 x 7 dot matrix. An on-chip row select counter sequences through the seven rows of each character. The five output buffers will each drive one TTL/DTL load directly at a 1.6 MHz input address rate making the 3258 an ideal device for CRT displays. Special input amplifiers on the Clock, Master Reset, and Address lines have eliminated the need for pull up resistors and allow direct operation at TTL/DTL logic levels.

- **PROGRAMMABLE WITH A CUSTOM CHARACTER FONT**
- **STANDARD PRODUCT: ASCII FONT**
- **16-PIN DUAL IN-LINE PACKAGE**
- **DIRECT TTL/DTL INTERFACE AT INPUTS AND OUTPUTS**
- **ON-CHIP ROW SELECT COUNTER**

PIN NAMES

A_n	Character Address Inputs
O_n	Character Outputs
$\overline{CP}$	Clock Pulse Input
$\overline{MR}$	Master Reset Input
V_{GG}	−12 V Power Supply
V_{DD}	0 V Power Supply
V_{SS}	+5.0 V Power Supply

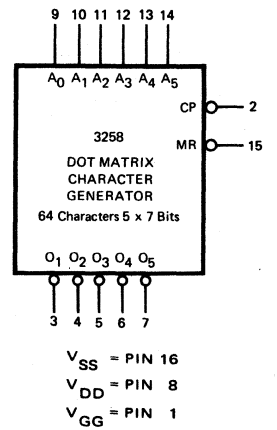
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65° to +150°C
Operating Temperature	0°C to +70°C
Voltage on any Pin Relative to V_{SS}	−20 V to +0.3 V

APPLICATIONS:

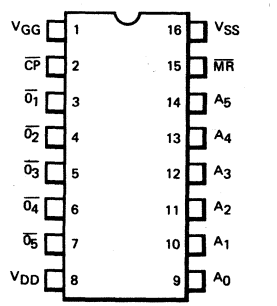
CRT Displays
Billboard Displays
LED Matrix Displays

LOGIC SYMBOL

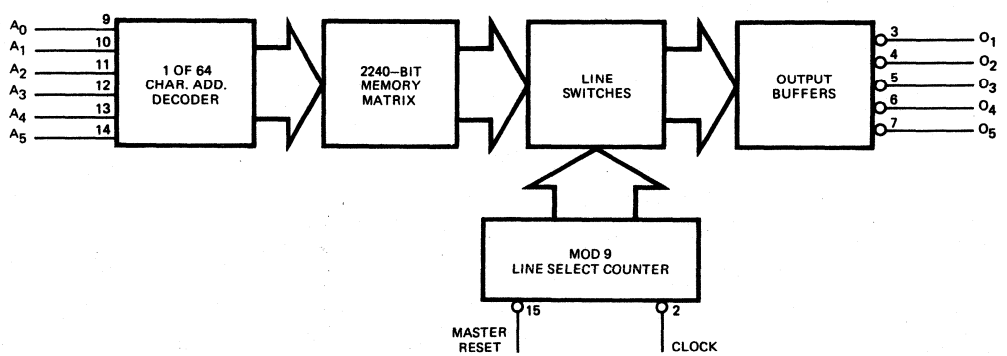


V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – A Master Reset pulse (≅ GND) is required to set the Modulo 9 counter to the first state. A 6-bit binary word present at the address inputs is decoded to select 1 of 64 characters in the memory. Information, representing the first row of the character, will be available at the five outputs the next clock time after the Master Reset goes HIGH (≅ V_{SS}). The next six rows of the character are sequentially selected by the counter. The last state of the counter, like the first state, clamps the outputs HIGH (≅ V_{SS}) which provides 2-space blanking between lines. The counter dead ends at the last state and the outputs will remain HIGH (≅ V_{SS}) providing blanking, until another Master Reset pulse is provided.

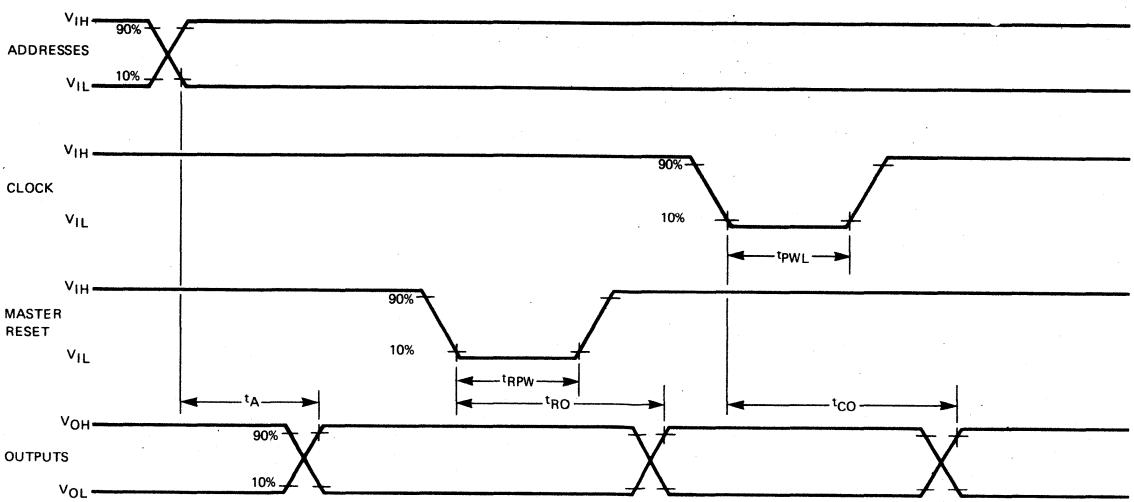
DC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to 70°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS} −2.35	V_{SS}	V	All Inputs
V_{IL}	Input LOW Voltage	V_{GG}	0.55	V	All Inputs
V_{OH}	Output HIGH Voltage	2.4	V_{SS}	V	I_{OH} = −0.5 mA
V_{OL}	Output LOW Voltage	0	0.4	V	I_{OL} = 2.4 mA
I_{IN}	Input Leakage Current		1.0	μA	V_{IN} = −13 V (Note 1)
I_{SS}	V_{SS} Current		28	mA	V_{SS} = +5.25 V, V_{GG} = −12.6 V Outputs Open
I_{GG}	V_{GG} Current		−28	mA	V_{SS} = +5.25 V, V_{GG} = −12.6 V Outputs Open
P_D	Power Dissipation		500	mW	

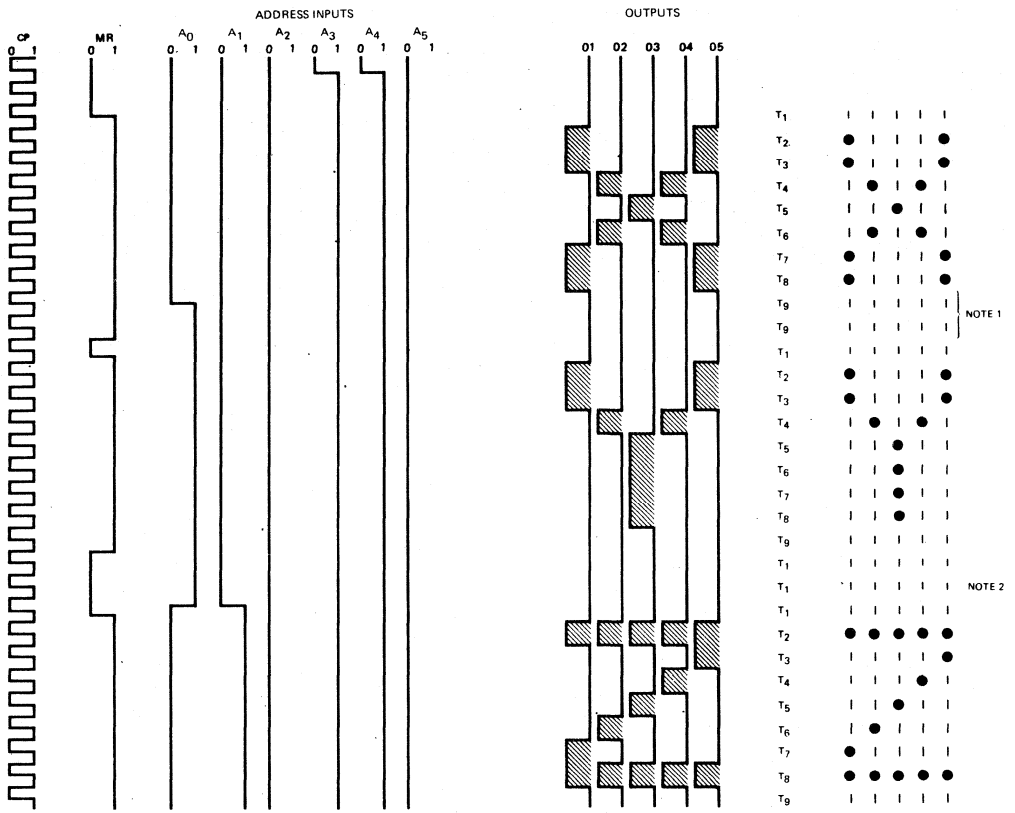
AC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, C_L = 10 pF, T_A = 0°C to +70°C.

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	CONDITIONS
f	Clock Frequency		0	500	kHz	
t_{PWL}	Clock Pulse Width		1.0		μs	
t_r, t_f	Clock Rise and Fall Time			2.0	μs	
t_{RPW}	Reset Pulse Width		500		ns	
t_{RS}	Reset to Clock Set-up		200		ns	
t_A	Character Address to Output Time Delay	3258-1		550	ns	
		3258-2		625	ns	
		3258		800	ns	
t_{CO}	Clock to Output Time Delay			2.0	μs	
t_{RO}	Reset to Output Time Delay			2.0	μs	

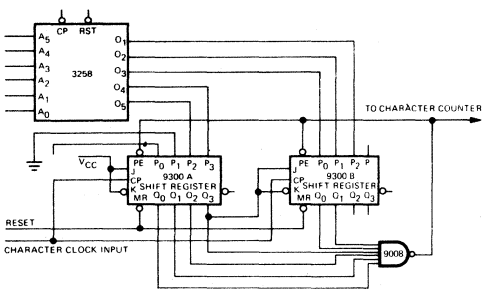
TIMING DIAGRAM

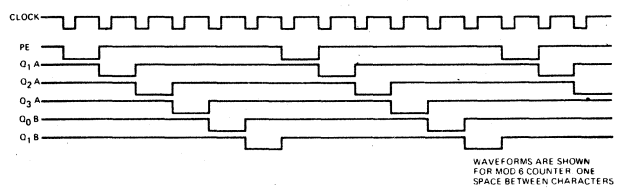


FUNCTIONAL TIMING DIAGRAM



APPLICATIONS





OPERATION:

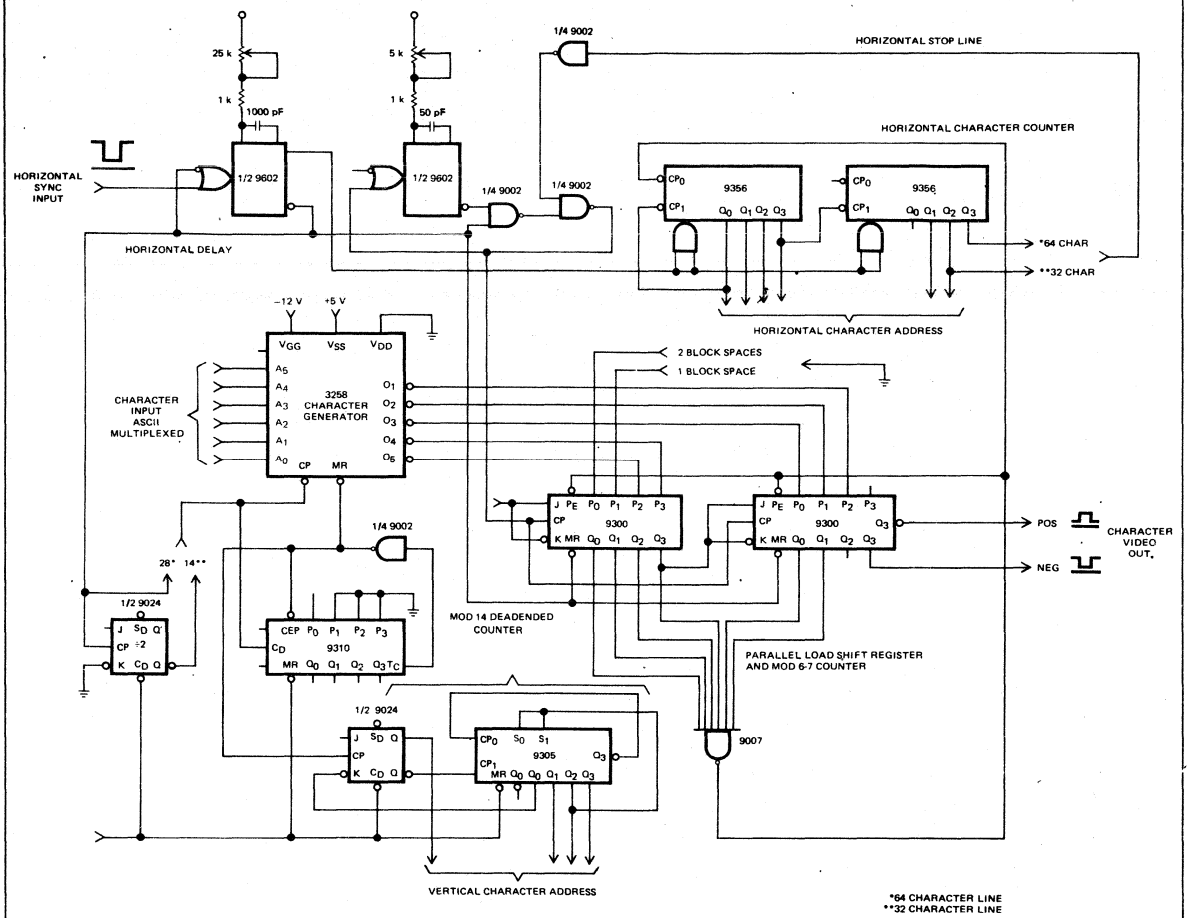
The two 9300 registers and the 9008, eight-input gate combine to form the character clock counter and the parallel to serial converter required for the outputs of the 3258 character generator.

When all the gate inputs are HIGH, the gate output is LOW which enables the parallel load (PE) of the shift registers. On the next clock pulse, positive edge after PE goes LOW, the contents of the 3258 character generator and the LOW on P_0 (A) are transferred into the registers. This LOW is shifted down the registers followed by all HIGH's from the JK input. On reaching Q_2 (B) all the outputs to the gates are once again HIGH, therefore reloading the shift registers again. The modulo count of the system can easily be changed to Modulo 7 by loading in a zero on P_0 (A).

The shift counter is reset at the beginning of each horizontal raster line to ensure that it has the correct time phase.

APPLICATIONS (cont'd)

HORIZONTAL RASTER SCAN CHARACTER GENERATOR



CUSTOM FONT ORDERING INFORMATION

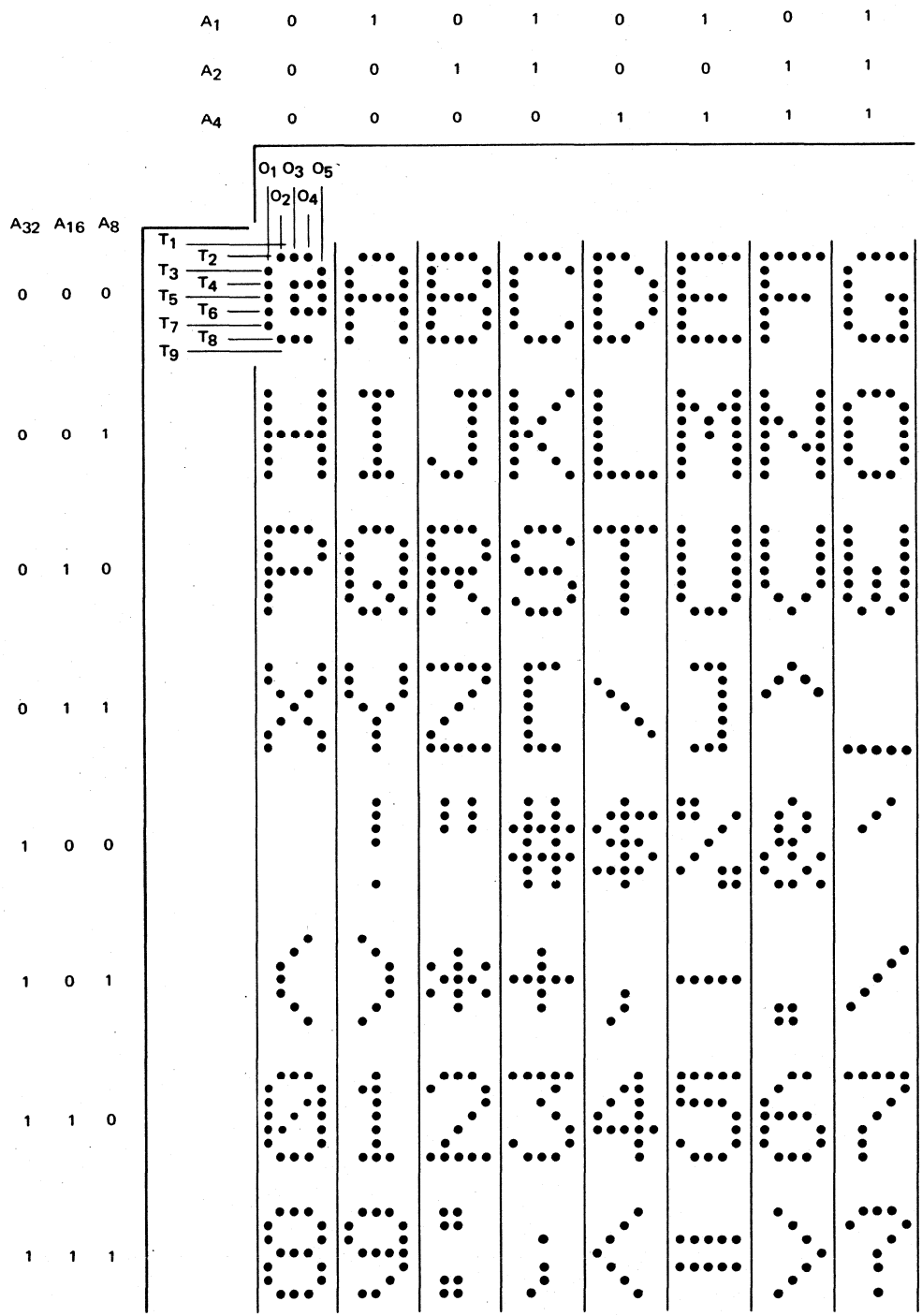
Additional character fonts are available on request. The 3258 is programmed on IBM cards or IBM coding forms in the coding format shown below:

A logic "1" = A more positive voltage nominally +5 V
A logic "0" = A more negative voltage nominally 0 V

The character must be defined by a logic "0". The background by a logic "1". Each character is programmed on one IBM card or a single line on the coding form.

COLUMN NUMBER	DESCRIPTION
6,7,8,9,10,11	Character address input code. The most significant bit (A32) is in Column 11.
22,23,24,25,26	The top line of the character addressed. The most significant bit (05) is in Column 26.
28,29,30,31,32	The next line of the character addressed. The most significant bit (05) is in Column 32.
34,35,36,37,38	The next line of the character addressed. The most significant bit (05) is in Column 38.
40,41,42,43,44	The next line of the character addressed. The most significant bit (05) is in Column 44.
46,47,48,49,50	The next line of the character addressed. The most significant bit (05) is in Column 50.
52,53,54,55,56	The next line of the character addressed. The most significant bit (05) is in Column 56.
58,59,60,61,62	The bottom line of the character addressed. The most significant bit (05) is in Column 62.
73,74,75,76,77,78,79,80	Coding these columns is not essential and may be used for card identification purpose.

STANDARD ASCII CHARACTER FONT



3260

64 × 9 × 7 CHARACTER GENERATOR

ERAL DESCRIPTION — The 3260 is a Character Generator designed to display 64 characters in
‹ 9 dot matrix. An on-chip row select counter sequences through the nine rows of each character.
of the seven output buffers will directly drive one TTL/DTL load. A unique 2-pin programming
re is provided enabling the user (if using a 7 x 16 display matrix) to select one of four display
es: Normal, Normal with Underline, Superscript, and Subscript.

UPERSCRIPT, SUBSCRIPT, & UNDERLINE CAPABILITY
UTPUT INVERSION CONTROL
IRECT TTL/DTL INTERFACING
-STATE OUTPUT CAPABILITY
SCII ENCODED

IAMES

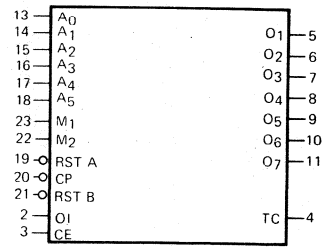
	Character Address Inputs	OI	Output Invert Control Input
	Display Mode Inputs	O_n	Character Outputs
$\overline{A}$	Reset Input "A"	TC	Terminal Count Output
$\overline{B}$	Reset Input "B"	V_{SS}	Substrate Power Supply (≈ 5V)
	Chip Enable Input	V_{DD}	0 V Power Supply
	Clock Input	V_{GG}	Gate Power Supply (≈ −12 V)

LUTE MAXIMUM RATINGS

orage Temperature	−65°C to +150°C
erating Temperature	0°C to +70°C
ltage on Any Input (V_{SS} = GND)	−20 V to +0.3 V
ltage on V_{DD} (V_{SS} = GND)	−7 V to +0.3 V
ltage on Outputs (V_{SS} = GND, Output Current @ +10 mA)	−7 V to +0.3 V

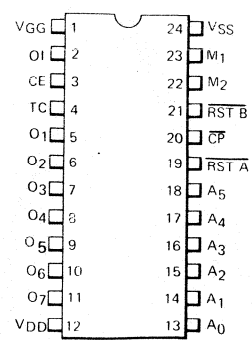
ICATIONS
RT Displays
lboard Displays

LOGIC SYMBOL

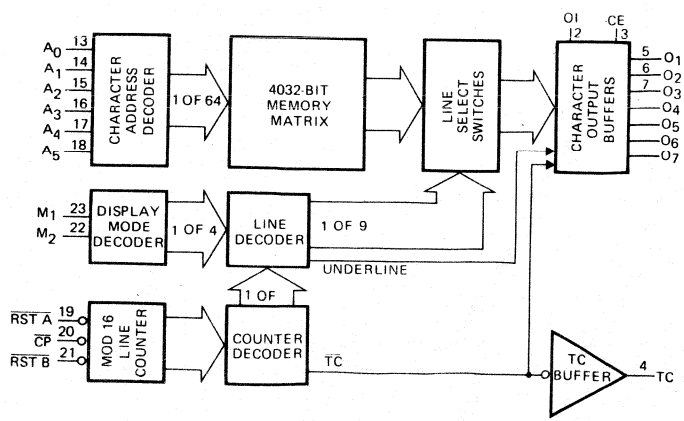


V_{SS} = PIN 24
V_{GG} = PIN 1
V_{DD} = PIN 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



OCK DIAGRAM



FUNCTIONAL DESCRIPTION — A 6-bit binary word present at the address inputs ($A_1 - A_{32}$) is decoded to select one of 64 characters in the memory. Information, representing a horizontal line of the character addressed, will be available at the 7 outputs ($O_1 - O_7$) within t_A after the address is present. The MOD 16 line counter sequences through the rows of the character with the application of a clock pulse (CP). A HIGH ($\sim V_{SS}$) on both RSTA and RSTB allows the counter to be free running. A LOW (~GND) on RSTA will cause the counter to dead end at T_{16} when reached. T_1 will again be reached the next clock time after RSTA returns HIGH. A LOW applied to RSTB sets the counter to T_7 independent of its previous state. This is useful when implementing a 9-line display.

To select the display mode for a specific character (this mode may be changed as often as the character address with no loss in access time), M_1 and M_2 are used. For normal operation (the character displayed during $T_4 - T_{12}$) M_1 and M_2 must both be LOW. For underline operation (character displayed during $T_4 - T_{12}$ underlline displayed during T_{14}), M_1 must be HIGH and M_2 must be LOW. For subscript operation (character displayed during $T_7 - T_{15}$), M_1 must be LOW and M_2 must be HIGH; and for superscript operation (character displayed during $T_1 - T_9$), both M_1 and M_2 must be HIGH (See Figure 1). When the counter reaches T_{16}, the Terminal Count (TC) output will go HIGH and will remain there until another counter state (T_1 or T_7) is reached, at which time TC returns LOW.

If the Output Invert (OI) pin is held HIGH, the resulting display will be a character of "0"s on a field of "1"s. A LOW on OI will produce the opposite effect.

The Chip Enable (CE) pin is provided to enable the user to combine the outputs of two or more 3260's if, for example, a 128-character font is desired.

On chip input pull up circuits will bring a normal TTL output to the desired level (at least $V_{SS}-1$ V) while the output buffers are capable of driving 1.5 TTL loads each.

DC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	$V_{SS}-1$ V	V_{SS}	V	Note 1
V_{IL}	Input LOW Voltage	0	0.8	V	
V_{OH}	Output HIGH Voltage	2.4	V_{SS}	V	I_{OH} = 0.5 mA
		$V_{SS}-1$ V	V_{SS}	V	I_{OH} = 10 μA
V_{OL}	Output LOW Voltage	0	0.4	V	I_{OL} = 2.4 mA
I_{IH}	Input HIGH Pull-up Current	100		μA	$V_{IN} = V_{SS} - 1$ V
I_{IL}	Input LOW Current		615	μA	V_{IN} = 0 V
I_{IN}	Input Leakage Current		1.0	μA	$V_{IN} = V_{SS} - 6$ V, Note 2
I_{OUT}	Character Output Leakage Current		1.0	μA	$V_{OUT} = V_{SS} - 6$ V, Note 3
I_{DD}	V_{DD} Current		36	mW	CE = Disable Code
I_{GG}	V_{GG} Current		24	mA	Outputs disabled
I_{SS}	V_{SS} Current		68	mA	Outputs Open
P_D	Power Dissipation		660	mW	Remaining Inputs = 0 V

NOTES:
1. Input pull up resistors to V_{SS} are provided on all inputs. The minimum V_{IH} is the level the resistors will pull a TTL input high voltage with 100 μA into the TTL output.
2. All pins at V_{SS} except pin under test.
3. Character outputs disabled. TC output is not three state.

DISPLAY MODE TRUTH TABLE

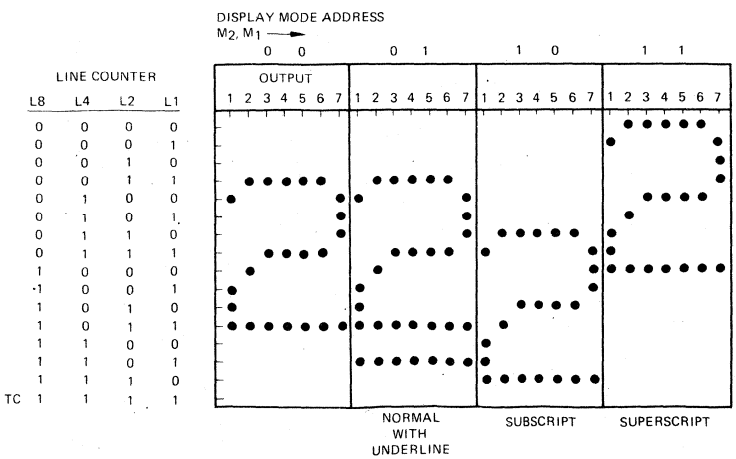
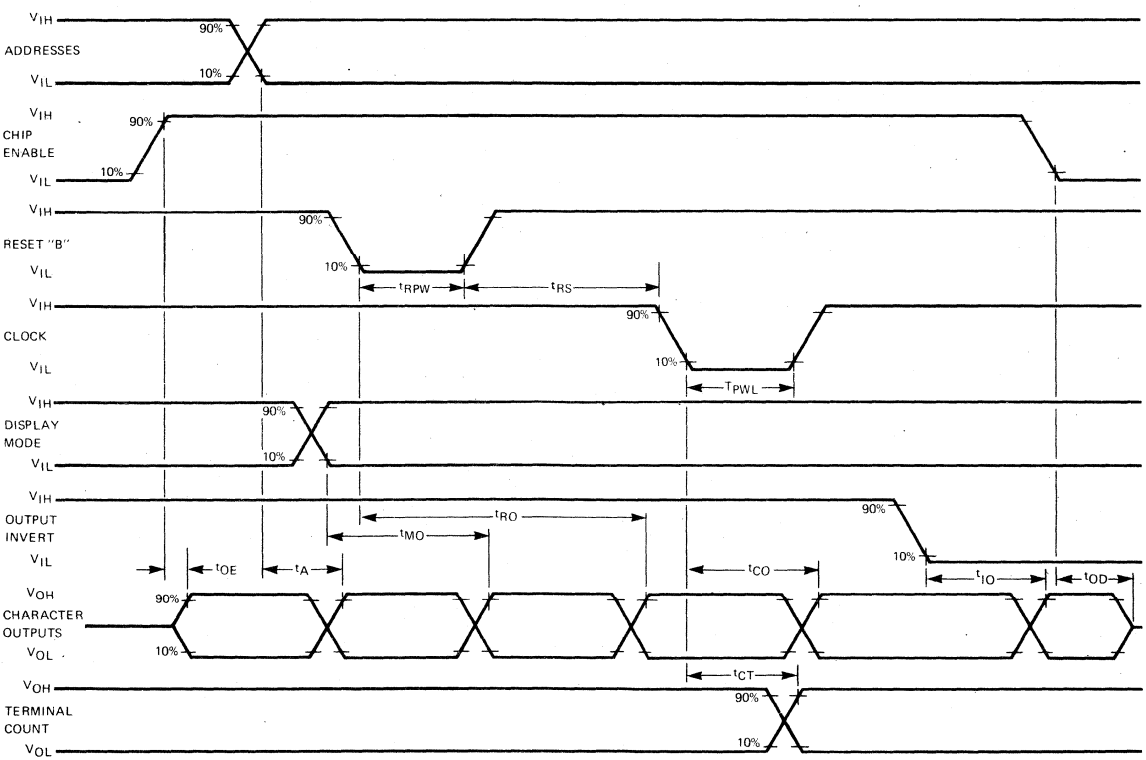


Fig. 1

AC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V; T_A = 0°C to 70°C, C_L = 20 pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
f	Clock Frequency	0		250	kHz	
t_{PWL}	Clock Pulse Width LOW	2.0			μs	
t_r, t_f	Clock Rise and Fall Time			2.0	μs	10% to 90% Points
t_{RPW}	Reset Pulse Width	2.0			μs	
t_{RS}	Reset to Clock Set-up Time Delay	500			ns	
t_A	Character Address to Character Output Time Delay	200		1000	ns	Note 1
t_{MO}	Display Mode Address to Character Output Time Delay	200		1000	ns	Note 1
t_{IO}	Output Invert to Character Output Time Delay	200		1000	ns	Note 1
t_{OE}	Character Output Enable Time Delay			100	ns	Note 1
t_{OD}	Character Output Disable Time Delay			1000	ns	Note 1
t_{CO}	Clock to Output Time Delay			2.5	μs	
t_{CT}	Clock to Terminal Count Output Time Delay			2.5	μs	
t_{RO}	Reset "B" to Character Output Time Delay			2.5	μs	
C_{IN}	Input Capacitance			8.0	pF	f = 1 MHz, 0 V Bias
C_{OUT}	Output Capacitance			10	pF	f = 1 MHz, 0 V Bias

TIMING DIAGRAM



CUSTOM FONT ORDERING INFORMATION

Custom patterns may be made available upon request. The coding format is shown below.
Specify access time desired on Purchase Order.

A Logic "1" = A more positive voltage, nominally + 5 V
A Logic "0" = A more negative voltage, nominally 0 V
Character outline dots must be programmed Logic "0", field Logic "1", for maximum access rate.

FIRST CARD:

COLUMN NUMBER	DESCRIPTION
29	Logic level at chip enable input required to enable chip.

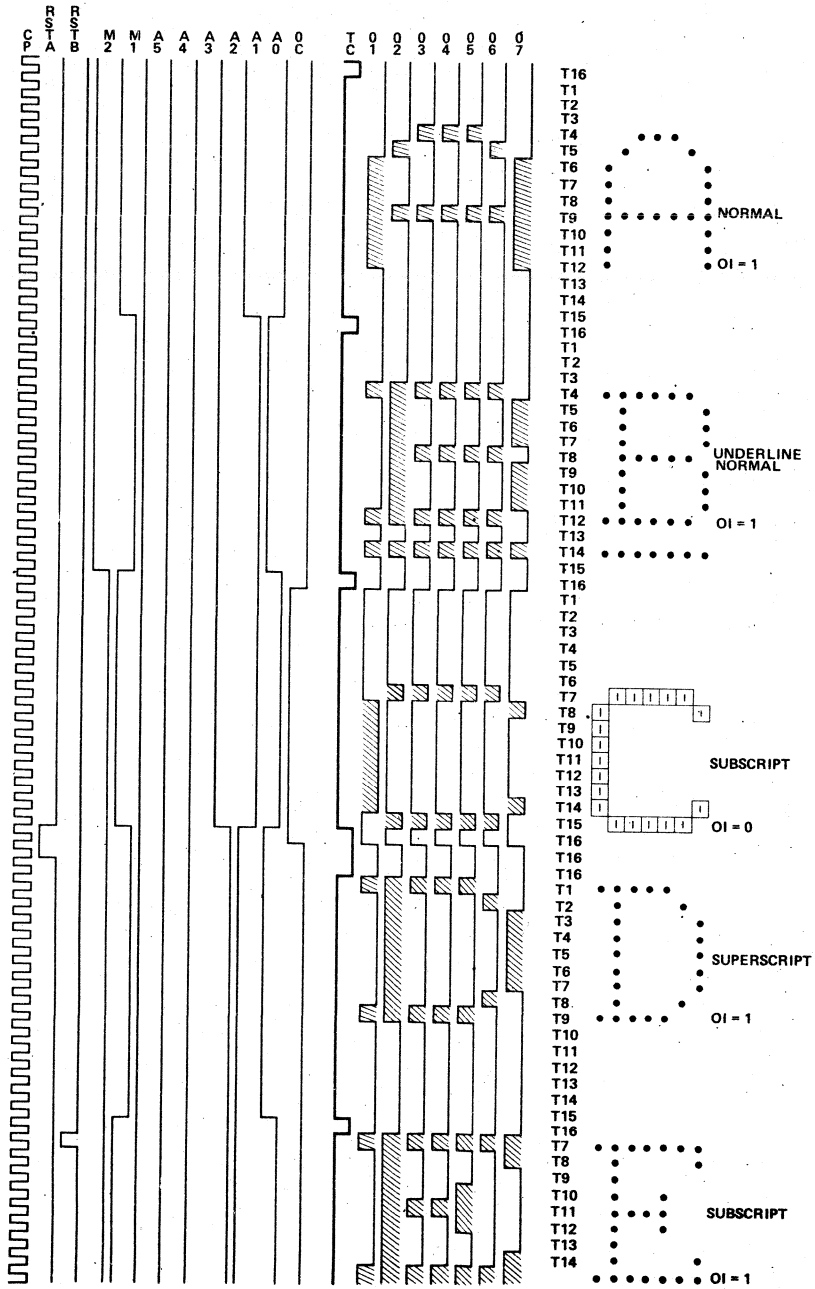
REMAINING 64 CARDS:

COLUMN NUMBER	DESCRIPTION
1, 2, 3, 4, 5, 6	Character address input code, the MSB (A5) is in Column 6.
8, 9, 10, 11, 12, 13, 14	The top line of the character addressed, the MSB O_7 is in Column 14.
15, 16, 17, 18, 19, 20, 21	The next line of the character addressed, the MSB O_7 is in Column 21.
22, 23, 24, 25, 26, 27, 28	The next line of the character addressed, the MSB O_7 is in Column 28.
29, 30, 31, 32, 33, 34, 35	The next line of the character addressed, the MSB O_7 is in Column 35.
36, 37, 38, 39, 40, 41, 42	The next line of the character addressed, the MSB O_7 is in Column 42.
43, 44, 45, 46, 47, 48, 49	The next line of the character addressed, the MSB O_7 is in Column 49.
50, 51, 52, 53, 54, 55, 56	The next line of the character addressed, the MSB O_7 is in Column 56.
57, 58, 59, 60, 61, 62, 63	The next line of the character addressed, the MSB O_7 is in Column 63.
64, 65, 66, 67, 68, 69, 70	The bottom line of the character addressed, the MSB O_7 is in Column 70.
73, 74, 75, 76, 77, 78, 79, 80	Coding these columns is not essential and may be used for card identification purpose.

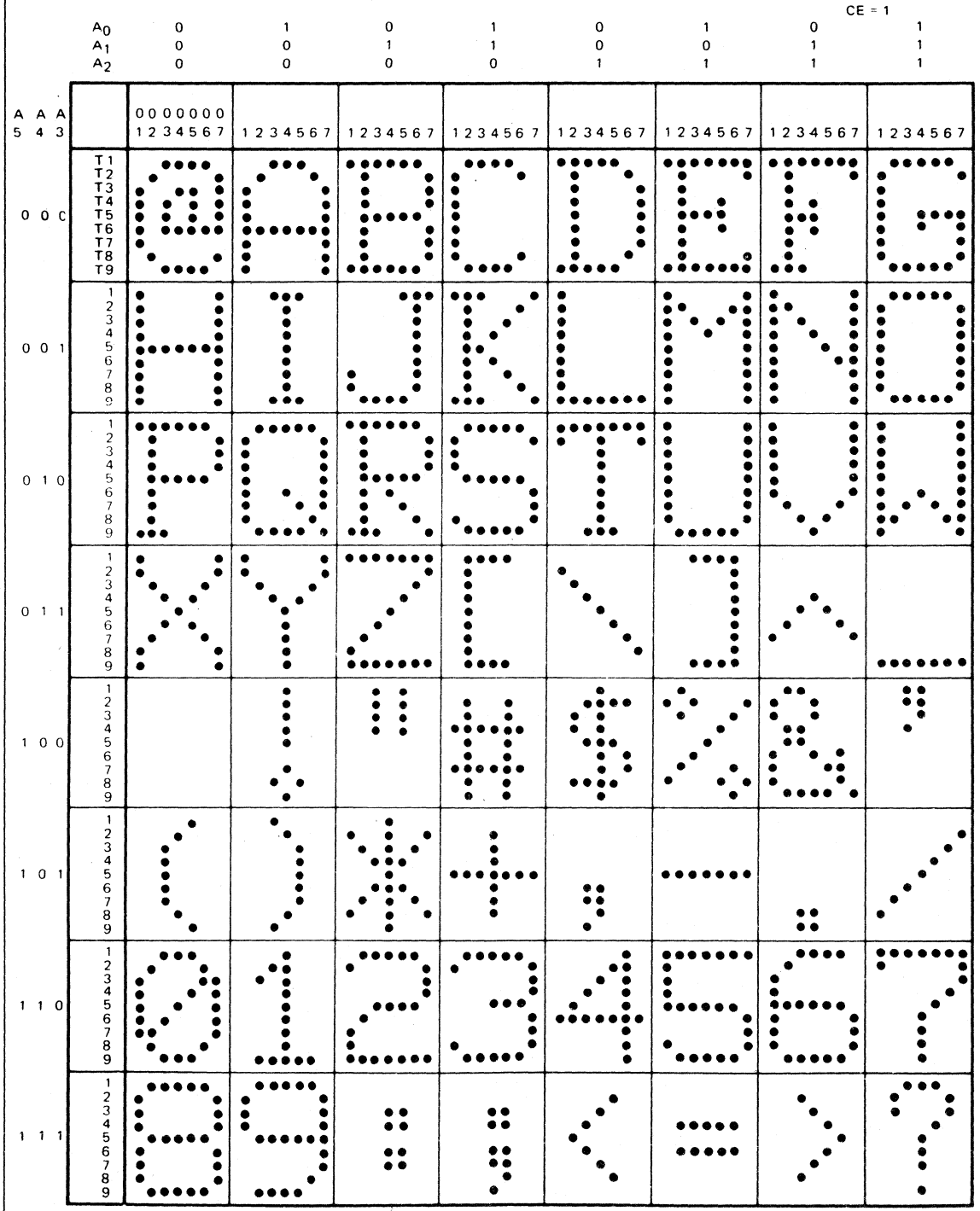
EXAMPLE: Letter G

	L S B						M S B	
	0	0	0	0	0	0	0	
	1	2	3	4	5	6	7	
Top Line	1	0	0	0	0	0	1	T1
	0	1	1	1	1	1	0	T2
	0	1	1	1	1	1	1	T3
	0	1	1	1	1	1	1	T4
	0	1	1	0	0	0	0	T5
	0	1	1	0	1	1	0	T6
	0	1	1	1	1	1	0	T7
	0	1	1	1	1	1	0	T8
Bottom Line	1	0	0	0	0	0	1	T9

FUNCTIONAL TIMING DIAGRAM



CHARACTER FONT



3341/3341A

64-WORD × 4-BIT FIRST-IN FIRST-OUT SERIAL MEMORY

GENERAL DESCRIPTION – The 3341 or 3341A is a 64-word x 4-bit memory that operates in a first-in first-out (FIFO) mode. Inputs and the output are completely independent (no common clocks) making the 3341/3341A ideal for asynchronous buffer applications.

Special on-chip input pull-up circuits and bipolar-compatible output buffers provide direct bipolar interfacing with no external components required. Control signals are provided so that both vertical and horizontal cascading may be easily achieved.

- **1 MHz SHIFT-IN SHIFT-OUT RATE (3341A)**
- **DIRECT TTL/DTL INTERFACE AT INPUTS AND OUTPUTS**
- **16-PIN DUAL IN-LINE PACKAGE**
- **READILY EXPANDABLE IN EITHER DIRECTION**
- **ASYNCHRONOUS OR SYNCHRONOUS OPERATION**
- **CONVENIENT PIN ORIENTATION FOR EASY BREADBOARDING**
- **UNIQUE TTL INPUT STAGE**

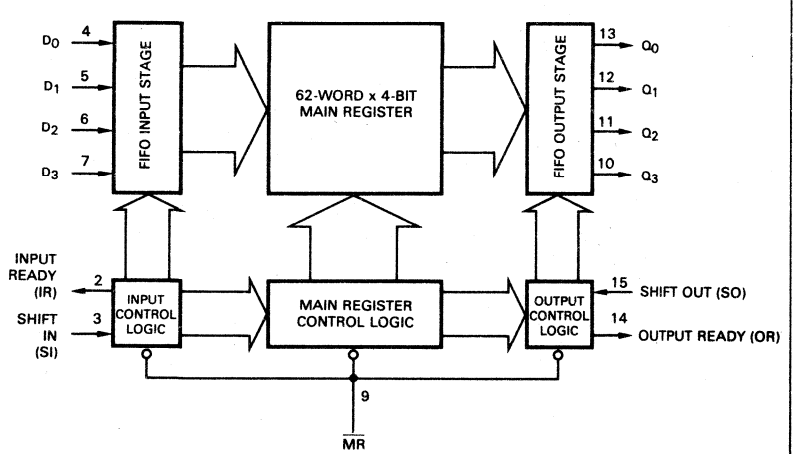
PIN NAMES

IR	Input Ready
SI	Shift In
Dn	Data Inputs
Qn	Data Outputs
$\overline{MR}$	Master Reset
OR	Output Ready
SO	Shift Out
V_{SS}	+5 Volt Power Supply
V_{DD}	0 Volt Power Supply
V_{GG}	−12 Volt Power Supply

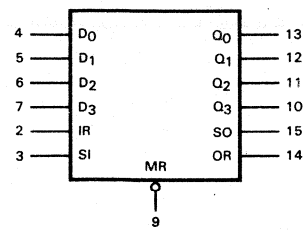
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	
3341ADC, 3341DC	0°C to +70°C
3341DL	−55°C to +85°C
3341DM	−55°C to +125°C
Voltage on all pins except V_{DD} with respect to V_{SS}	−20 V to +0.3 V
Voltage on V_{DD}	−7.0 V to +0.3 V

BLOCK DIAGRAM

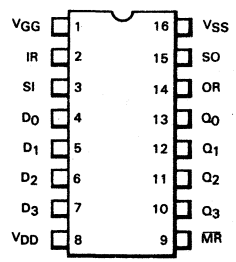


LOGIC SYMBOL



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 1

CONNECTION DIAGRAM DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION:

INPUT:

4 four bits of data on the D_0 through D_3 inputs are entered into the first bit location when both Input Ready (IR) and Shift In (SI) are HIGH ($\approx V_{SS}$). This causes IR to go LOW ($\approx V_{DD}$), but data will stay locked in the first bit location until both IR and SI are LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

DATA TRANSFER:

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{BT} defines the time required for the first data to travel from input to the output of a previously empty device, or for the first empty space to travel from the output to the input of a previously full device.

DATA OUTPUT:

When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of a valid data at the output pins Q_0 through Q_3. The transfer of data is initiated when both the Output Ready output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BT}) or completely empty (Output Ready stays LOW for at least t_{BT}).

RESET:

When Master Reset ($\overline{MR}$) goes LOW, the control logic is cleared. When $\overline{MR}$ returns HIGH, Output Ready (OR) stays LOW, and Input Ready (IR) goes HIGH if Shift In (SI) was LOW. Since the Data Outputs (Q_0 through Q_3) are unaffected by $\overline{MR}$, Data on Q_0 through Q_3 should be considered valid only while OR is HIGH.

SPECIAL INPUT CHARACTERISTICS:

The 3341 and 3341A use a TTL-compatible input pull-up circuit. When going HIGH, the TTL driver need only provide 2.2 V minimum. The input is then internally pulled up to V_{SS}.

When going LOW, the TTL driver must overcome a maximum current barrier of 1.6 mA at 2 V. Once this current is reached, the input current drops to I_{IL}.

All inputs are returned to V_{SS} internally through a switched pull-up resistor.

DC CHARACTERISTICS: DC, DL, DM: V_{SS} = +5 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V. (Note 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS}−1.0			V	Notes 2 and 3
V_{IL}	Input LOW Voltage			0.8	V	Note 2
V_{OH}	Output HIGH Voltage	V_{SS}−1.0			V	I_{OH} = 0.3 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{II}	Input Pull-up			2.0	V	V_{SS} = 4.75 V
	Initiation Voltage			2.2	V	V_{SS} = 5.25 V
V_{IP}	Peak Input Current Voltage Point			V_{SS}−1.5	V	
I_{IH}	Input HIGH Current	250			μA	Note 2, V_{IN} = V_{SS}−1.0 V
I_{IL}	Input Leakage Current			30	μA	Note 2, V_{IN} = 0 V
I_{IP}	Input Barrier Current			1.6	mA	Note 2
I_{GG}	V_{GG} Current			12	mA	3341DC, 3341ADC
				16	mA	3341DL, 3341DM
I_{DD}	V_{DD} Current			45	mA	3341DC, 3341ADC
				60	mA	3341DL, 3341DM
P_D	Power Dissipation			450	mW	3341DC, 3341ADC
				600	mW	3341DL, 3341DM

NOTES:
1. See Operating Temperatures on preceeding page.
2. Inputs include D_0 – D_3, $\overline{\text{Master Reset}}$, Shift In, and Shift Out.
3. Internal pull up circuits are provided on all inputs to insure proper HIGH level.

AC CHARACTERISTICS: V_{SS} = +5 V ±5%, V_{DD} = 0 V, V_{GG} = 12 V ±5% (Note 1)

SYMBOL	PARAMETER	3341A DC			3341 DC, DL, DM			UNITS	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
t_{IRH}	Input Ready HIGH Time	50		400	90	300	550	ns	Fig. 1, Note A, Note F
t_{IRL}	Input Ready LOW Time	100		550	138	300	550	ns	Fig. 1, Note B
t_{OVH}	Control Overlap HIGH Time	80			100			ns	Figs. 1 and 2, Note 4, Note K
t_{OVL}	Control Overlap LOW Time	80			100			ns	Figs. 1 and 2, Note 4, Note L
t_{DH}	Data Input Stable Time	200			400			ns	Fig. 1
t_{DD}	Data Input Delay Time			0			25	ns	Fig. 1, Note C
t_{ORH}	Output Ready HIGH Time	70		450	90	300	500	ns	Fig. 2, Note G
t_{ORL}	Output Ready LOW Time	70		550	170	450	850	ns	Fig. 2, Note H
t_{BT}	Data Bubble-through Time			16			32	µs	Note 5
t_{DV}	Data Valid After SI or OR	75			75			ns	Fig. 2, Note J
t_{MRW}	Master Reset Pulse Width	400			400			ns	Note 7
t_{DA}	Data Output Available Time	0			0			ns	Fig. 2
C_{IN}	Input Cap. of Data and Control Lines			7.0			7.0	pF	f = 1 MHz, $V_{IN} = V_{SS}$
C_{MR}	Input Cap. of $\overline{MR}$			7.0			15	pF	f = 1 MHz, $V_{MR} = V_{SS}$

NOTES:
4. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.
5. This parameter defines total time from the time data is loaded into the first word location to the time it is available at $O_0 - O_3$ with FIFO initially empty. Conversely, t_{BT} also defines the time required for an empty space to propagate from the last word location back to the first word location. When the FIFO is full, this is the time from the HIGH to LOW transition of OR to the LOW to HIGH transition of IR.
6. 1 TTL load +20 pF.
7. The $\overline{MR}$ input overrides all other control functions. It resets the control register and the input-and output control logic while disabling any SI or SO inputs.

TIMING DIAGRAMS

INPUT TIMING

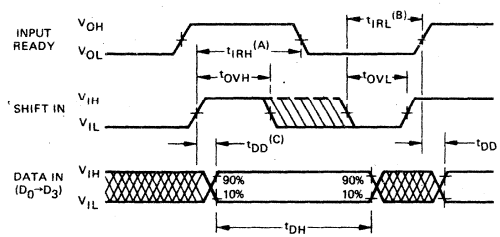


Figure 1

OUTPUT TIMING

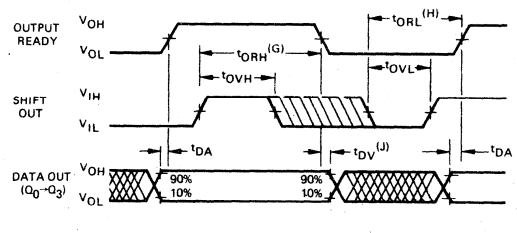


Figure 2

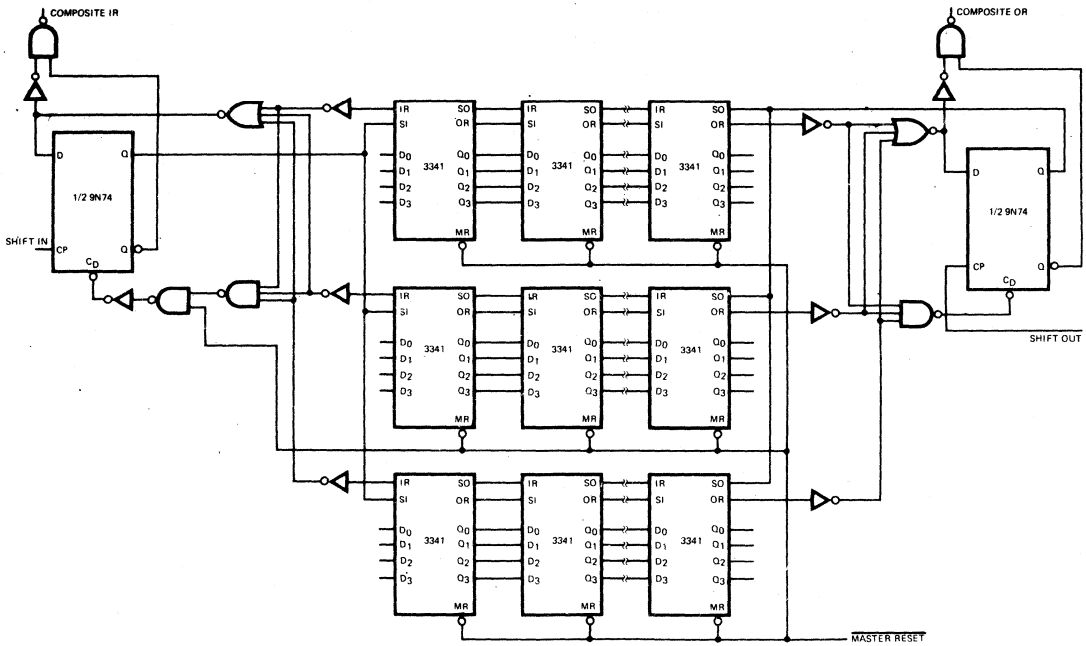
Input data must remain stable during timing window t_{DH}. Both SI and IR must be HIGH for t_{OVH}. Similarly, both SI and IR must be LOW for t_{OVL}.

Both SO and OR must be HIGH for t_{OVH}. Similarly both SO and OR must be LOW for t_{OVL}. Data will remain stable for t_{DV} after both SO and OR are LOW.

NOTES:
A. t_{IRH} is referenced to the positive going edge of IR or SI, whichever occurs later.
B. t_{IRL} is referenced to the negative going edge of IR or SI, whichever occurs later.
C. t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.
D. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
E. t_{OVL} is referenced to the negative going edge of IR or SI whichever occurs later.
F. Data must be stable for t_{DH} or t_{IRH}, whichever is shorter.

NOTES:
G. t_{ORH} is referenced to the positive going edge of OR or SO, whichever occurs later.
H. t_{ORL} is referenced to the negative going edge of OR or SO, whichever occurs later.
J. t_{DV} is referenced to the negative going edge of OR or SO, whichever occurs later.
K. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
L. t_{OVL} is referenced to the negative going edge of IR or SI, whichever occurs later.

EXPANSION OF 3341 TO N-WORD BY 12-BIT FIFO



NOTE: Composite Shift In should be LOW when Master Reset goes HIGH. Input data may be changed after Composite IR goes LOW. Composite IR will not go HIGH until Composite Shift In goes LOW. When Composite IR goes HIGH, FIFO's will accept new data. 3341's will operate at full speed if these rules are followed.

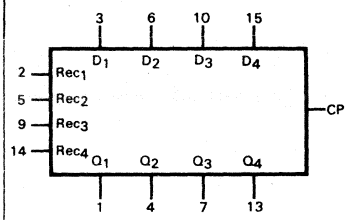
3342/3347

QUAD 64-QUAD/80-BIT STATIC SHIFT REGISTERS

GENERAL DESCRIPTION – The 3342 and 3347 are Static Shift Registers in Quad 64-bit and Quad 80-bit organizations, respectively. An on-chip clock generator provides appropriate internal clock phases from a single external TTL-level clock input. Passive on-chip input pull-up resistors allow direct TTL compatibility on all inputs. The outputs are capable of driving a single TTL load directly without the need for external components. Both the 3342 and 3347 are manufactured with the p-channel silicon gate technology. They are available in ceramic or plastic 16-pin Dual In-line Packages in the commercial temperature range, 0°C to +70°C.

- **SINGLE TTL COMPATIBLE EXTERNAL CLOCK**
- **DIRECT TTL COMPATIBILITY**
- **1.5 MHz OPERATION GUARANTEED**
- **LOW CLOCK CAPACITANCE**
- **INPUT OVERVOLTAGE PROTECTION**
- **EXTERNAL RECIRCULATE CONTROL**
- **16-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE**

LOGIC SYMBOL

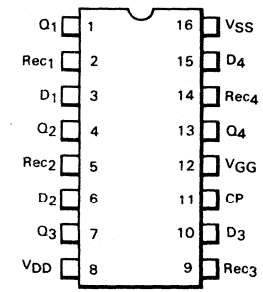


V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 12

PIN NAMES

Q_n	Data Outputs	V_{SS}	+5-volt Power Supply
D_n	Data Inputs	V_{DD}	0-volt Power Supply
Rec_n	Recirculate Inputs	V_{GG}	−12-volt Power Supply
CP	Clock Pulse Input		

CONNECTION DIAGRAM
DIP (TOP VIEW)

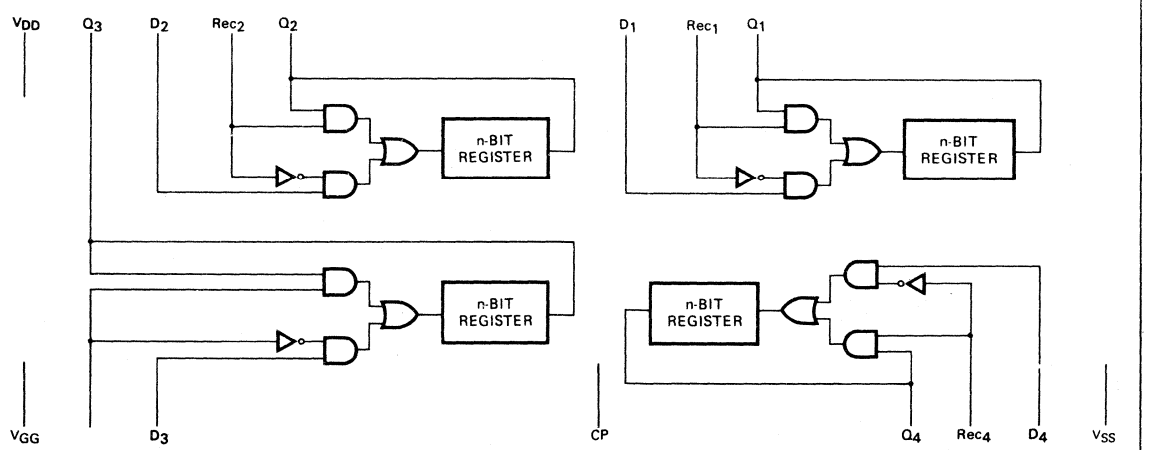


ABSOLUTE MAXIMUM RATINGS

All Inputs Including Clock (Note 1)	−20 V to +0.3 V
V_{GG} (Note 1)	−20 V to +0.3 V
V_{DD} and Outputs (Note 1)	−7.0 V to +0.3 V
Output Current when Output is LOW (Note 2)	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

NOTES:
1. All voltages with respect to V_{SS}.
2. LOW logic level is most negative level and HIGH logic level is most positive.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 3342 and 3347 are Single Phase Static Shift Registers. Data is accepted at the inputs when the external clock is HIGH. Data is available at the outputs after the negative clock transition as illustrated in *Figure 1.* All inputs are connected by an MOS transistor to V_{SS} allowing complete TTL compatibility. The recirculate inputs allow data to be entered externally (LOW logic level) or internally recirculated in the registers (HIGH logic level). The output stages are push/pull amplifiers and can drive one TTL load.

DC REQUIREMENTS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS} -1.0			V	Notes 1 and 2
V_{IL}	Input LOW Voltage	V_{GG}		0.80	V	Note 1

DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4		V_{SS}	V	I_{OH} = -0.5 mA
V_{OL}	Output LOW Voltage	0		0.4	V	I_{OL} = -1.6 mA
I_{IH}	Input HIGH Current	-0.10			mA	V_{IN} = V_{SS} -1.0 V, Note 1
I_{IL}	Input LOW Current			-1.6	mA	V_{IN} = 0.4 V, Note 1
I_{IN}	Input Leakage Current			1.0	μA	V_{IN} = -5.0 V, Note 1 V_{GG} = V_{SS}
I_{DD}	V_{DD} Current			28	mA	
I_{GG}	V_{GG} Current			12	mA	
I_{SS}	V_{SS} Current			40	mA	
P_D	Power Dissipation			380	mW	t_{PWH} = 265 ns, f = 1.5 MHz

NOTES:

1. These parameters apply to all data, recirculate, and clock inputs.
2. On-chip pull-up resistors are provided on all inputs to effect the proper logic level when driving with TTL/DTL.

AC REQUIREMENTS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C. (Note 4)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
f	Operating Frequency	0		1.5	MHz	Note 4
t_{PWH}	Clock Pulse Width HIGH	.265		10	µs	Note 3
t_{PWL}	Clock Pulse Width LOW	.320			µs	
t_r, t_f	Clock Rise and Fall Times (10% to 90%)			1.0	µs	
t_{DS}	Data Input Set-up Time	200			ns	
t_{DH}	Data Input Hold Time	100			ns	
t_{RS}	Recirculate Set-up Time	200			ns	
t_{RH}	Recirculate Hold Time	130			ns	

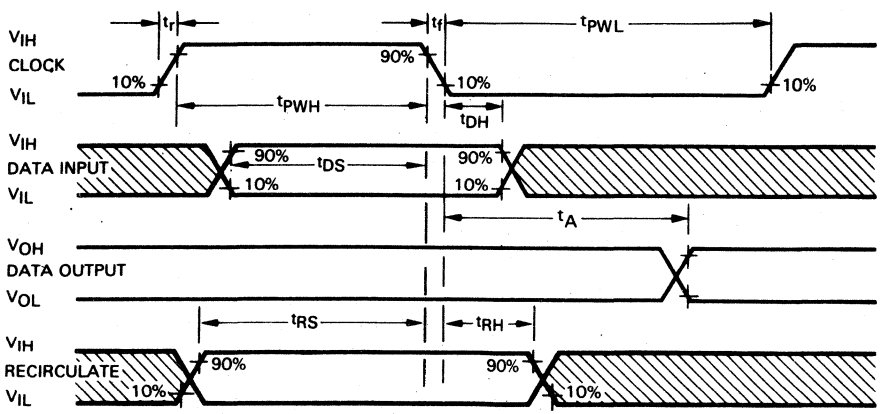
NOTES:

3. Outputs remain valid until negative-going edge of next clock pulse.
4. $1/f = t_{PWH} + t_{PW} + tr + tf$.

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_A	Clock to Output Delay			265	ns	C_L = 10 pF Load = 1 TTL Input
C_{IN}	Capacitance (All Inputs Including Clock)			5.0	pF	V_{IN} = V_{SS}, f = 1.0 MHz

WAVEFORM



3348/3349
HEX 32-BIT STATIC SHIFT REGISTER

GENERAL DESCRIPTION — The 3348/3349 contains six separate 32-Bit Static Shift Registers constructed in a single chip using P-channel enhancement mode silicon gate MOS technology. Only two power pins, V_{SS} and V_{GG}, are needed for circuit operation. An on-chip clock generator provides all internal clock phases from a single TTL clock pulse. Each output is a bare drain, and therefore requires a 7.5 kΩ load resistor to V_{GG}. A recirculate data input allows the user to either enter data from the outside (LOW logic level) or to internally recirculate the contents of the registers (HIGH logic level).

The 3348 is available in a 24-pin ceramic Dual In-line Package and the 3349 is available in a 16-pin plastic or ceramic Dual In-line Package. The 3348 option provides an output disable pin for wired-OR operation. The outputs are disabled when Output Enable is HIGH.

- **SINGLE TTL EXTERNAL CLOCK**
- **INPUT OVERVOLTAGE PROTECTION**
- **LOW CLOCKLINE CAPACITANCE**
- **TTL COMPATIBLE INPUTS**
- **CASCADE CAPABILITY**
- **SINGLE POWER SUPPLY OPERATION**
- **INTERNAL RECIRCULATION CONTROL**
- **DC TO 1 MHz OPERATION GUARANTEED**
- **OUTPUT DISABLE CONTROL (3348 ONLY)**
- **SINGLE ENDED (BARE DRAIN) BUFFERS**

PIN NAMES

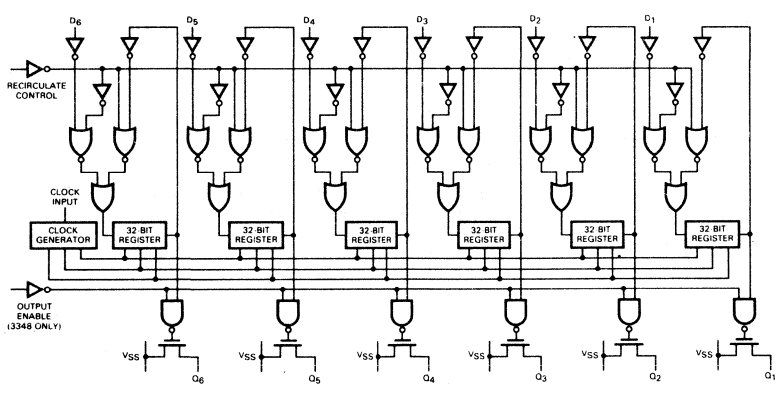
D_n	Data Inputs
Q_n	Data Outputs
R	Recirculate Input
$\overline{CP}$	Clock Pulse
OE	Output Enable

ABSOLUTE MAXIMUM RATINGS

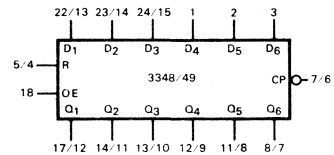
All Inputs, V_{GG}	−22 V to +0.3 V
All Outputs	−19 V to +0.3 V
Output Current	+10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

Note: All voltages with respect to V_{SS}.

BLOCK DIAGRAM

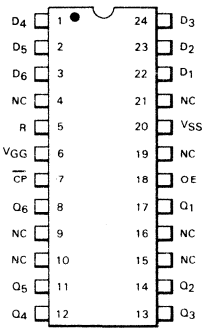


LOGIC SYMBOL

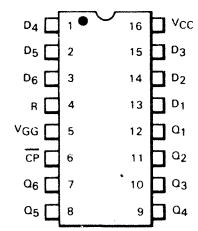


CONNECTION DIAGRAMS
DIP (TOP VIEW)

3348



3349



FUNCTIONAL DESCRIPTION – The 3348/3349 is a two-phase static shift register. The single external clock phase generates two shift phases as well as a static operation phase via the on-chip clock generator. Data is accepted at the inputs after the negative-going transition of the external clock. Output information is available after the positive clock transition as illustrated in *Figure 1*. For long-term storage, the external clock should be held HIGH.

DC REQUIREMENTS: V_{SS} = 5 V ±5%, V_{GG} = −12 ±1 V, T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	$V_{SS}-1.5$			V	All Inputs Including Clocks
V_{IL}	Input LOW Voltage			0.6	V	All Inputs Including Clocks
R_L	Output Load Resistor to V_{GG}	7.5			kΩ	

DC CHARACTERISTICS: V_{SS} = 5 V ±5%, V_{GG} = −12 ±1 V, T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	$V_{SS}-1.2$			V	7500 Ω Load to V_{GG} V_{SS} = 4.75 V, V_{GG} = −11 V
I_{IN}	Input Leakage Current			1.0	μA	V_{IN} = 0 V
I_{GG}	V_{GG} Current			27	mA	V_{GG} = −12 V, V_{SS} = 5.0 V

AC REQUIREMENTS: V_{SS} = 5 V ±5%, V_{GG} = −12 ±1V, T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
f	Operating Frequency			1.0	MHz	
t_{PWL}	Clock Pulse Width LOW	0.35		50	μs	
t_{PWH}	Clock Pulse Width HIGH	0.6			μs	
t_r, t_f	Clock Rise Time and Fall Time			0.5	μs	
t_{DS}	Input Data Set-Up Time	180			ns	
t_{DH}	Input Data Hold Time	40			ns	
t_{RPW}	Recirculate Pulse Width	350			ns	
t_{RS}	Recirculate Set-Up Time	225			ns	
t_{RH}	Recirculate Hold Time	100			ns	

AC CHARACTERISTICS: V_{SS} = 5 V ±5%, V_{GG} = −12 ±1 V, T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_A	Clock to Data Out Delay Time	125		520	ns	C_L = 0 to 20 pF, R_L = 7.5 kΩ
t_{EO}	Output Enable Time Delay (3348 Only)			350	ns	C_L = 20 pF, R_L = 7.5 kΩ to V_{GG}
t_{DO}	Output Disable Time Delay (3348 Only)			350	ns	

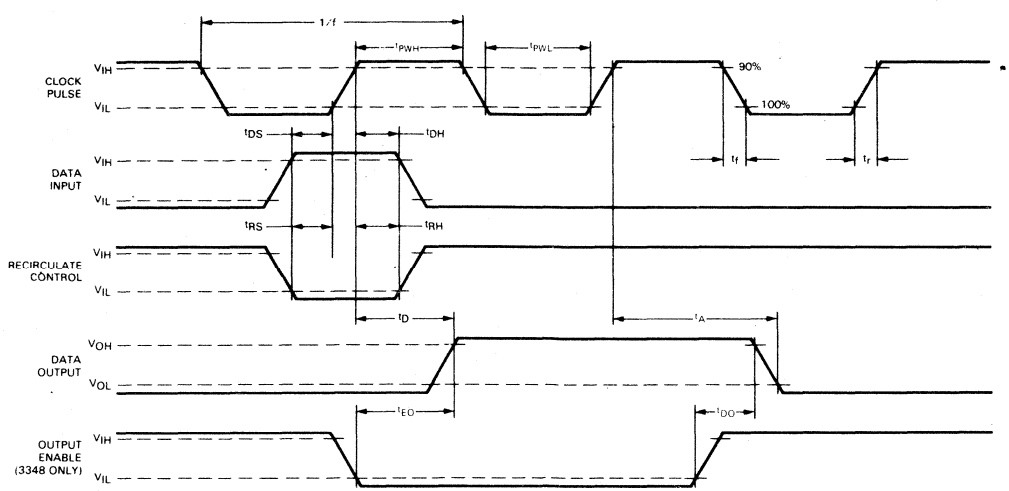


Fig. 1. 3348/3349 Timing Diagram and Voltage Waveforms

3351
40×9 FIRST-IN FIRST-OUT MEMORY

GENERAL DESCRIPTION – The 3351 is a First-In First-Out (FIFO) Memory used in data rate buffering applications. The 3351 has a capacity of 40 nine-bit words. The words are accepted at the input, automatically shifted toward the output, and removed at any rate in the same sequence in which they were entered.

The 3351 has status indicators on both the input and output to signal an available empty input or a valid data word at the output. It also has separate input and output enable lines, in addition to a master reset line. A unique input stage interfaces to TTL without external components. The 3351 is manufactured using the p-channel Isoplanar silicon gate process with ion-implantation.

- **2 MHz (3351-1) AND 1 MHz (3351-2) DATA RATES**
- **INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS**
- **FULLY TTL COMPATIBLE**
- **3-STATE OUTPUTS**
- **INPUT AND OUTPUT ENABLES**
- **EXPANDABLE IN EITHER DIRECTION**
- **STATUS INDICATORS ON INPUT AND OUTPUT**
- **28-PIN CERAMIC DUAL IN-LINE PACKAGE**

PIN NAMES

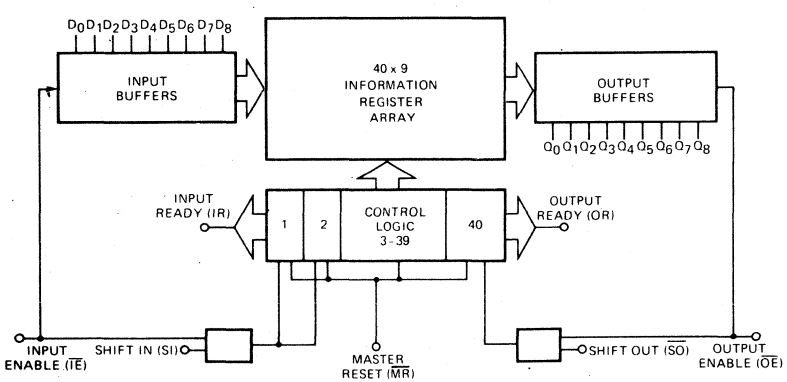
Q_n	Outputs	IR	Input Ready
D_n	Data Inputs	OR	Output Ready
$\overline{MR}$	Master Reset	$\overline{IE}$	Input Enable
SI	Shift In	$\overline{OE}$	Output Enable
SO	Shift Out		

ABSOLUTE MAXIMUM RATINGS

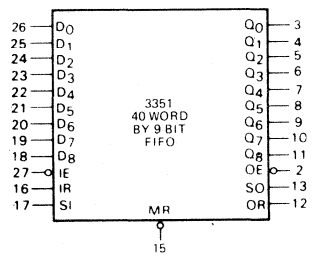
V_{GG} and Inputs	−20 V to +0.3 V
V_{DD} and Outputs	−7.0 V to +0.3 V
Output Sink Current	5.0 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

NOTE: All Voltages with respect to V_{SS}.

BLOCK DIAGRAM

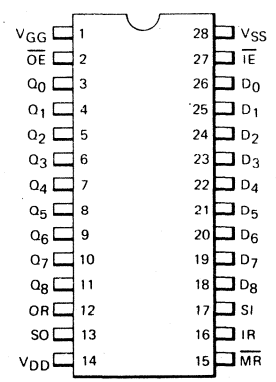


LOGIC SYMBOL



V_{SS} = Pin 28
V_{DD} = Pin 14
V_{GG} = Pin 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 40 by 9 memory array is under the constant control of a control logic network (See Fig. 1). Each word position in the array is clocked by a control register, which also stores a marker bit; a "1" signifies that that position's data is filled and a "0" indicates a vacancy at that location. Each control register clocks data from the preceding nine data flip-flops to its own set of nine data flip-flops. The register logic detects the status of the preceding and succeeding registers' marker bits to determine when to clock its data flip-flops. When data has been transferred from location "n" to location "n+1", the n+1 control circuitry changes the marker bit at control register "n" from a "1" to a "0", indicating that the data at location "n" has been transferred elsewhere in the array. This "0" will then propagate back to the first control register signifying that the FIFO is capable of accepting more data.

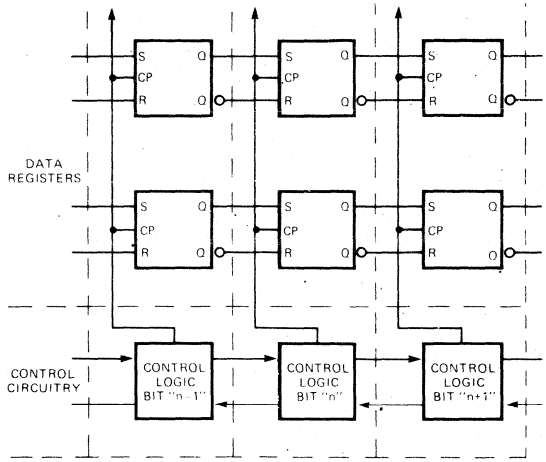


Fig. 1

The 3351 buffers the first and last control registers and uses them as input/output status indicators. Since all status marker "0"s propagate toward the first control register, a "0" at the first register indicates the FIFO is ready to clock in more data. Likewise, all "1"s propagate towards the last control register, and a "1" here means that data is valid at the outputs.

A Master Reset control is provided to set all the control registers' status markers to "0". Note that the data registers are not reset by $\overline{MR}$.

SHIFT IN (SI), INPUT READY (IR) – A LOW to HIGH transition of the Shift In command does two things: 1) the first control register is enabled, permitting input data to be loaded into the first set of data registers and setting the first marker bit to a "1", and 2) the second control register is locked out by means of an inverted SI command. At this point, data from the first data register cannot be transferred to the second data register. The Input Ready signal indicates the status of the first marker bit and accordingly goes LOW(not ready).

The HIGH to LOW transition of the SI locks out the first control register and causes data from the first data registers to propagate down the FIFO under the control of the control logic. This action sets the first marker bit to a "0" and the Input Ready returns HIGH (input ready). When the FIFO becomes full, the IR will stay LOW after SI returns LOW and any further SI commands will be ignored by the circuit. When a "0" ripples back from the last to the first control register the Input Ready (IR) will return to HIGH (if SI is LOW).

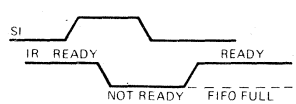


Fig. 2

INPUT ENABLE ($\overline{IE}$) – A HIGH on the Input Enable disables the SI input and the current-sourcing capability of the special TTL pull-up networks of the data inputs and the SI. A LOW enables these inputs.

SHIFT OUT (SO), OUTPUT READY (OR) – The HIGH to LOW transition of Shift Out command disables the clocking line of the last control register and changes the 40th bit marker to a "0". The Output Ready is then forced LOW. Note that data is not transferred from the 39th position to the 40th position on this edge. When SO makes the LOW to HIGH transition, the FIFO is again under control of its control logic circuitry, new data is transferred to the 40th location and the 40th marker bit is reset to a "1". The Output Ready returns to HIGH, signifying the new data at the output leads is now valid.

When the FIFO is empty, the OR remains LOW after SO goes HIGH. SO commands will be ignored until a "1"marker ripples down to the last control register, after which the OR goes HIGH (if SO is HIGH).

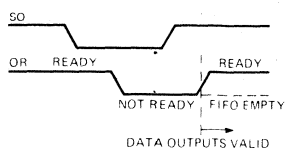


Fig. 3

OUTPUT ENABLE ($\overline{OE}$) – A HIGH on Output Enable forces the nine outputs to a high impedance state, disables the shift out command, and disables the current-sourcing capability of the special TTL pull-up network of SO. A LOW again enables SO, and the outputs revert back to their normal TTL states.

MASTER RESET ($\overline{MR}$) – A LOW on Master Reset sets all the control logic marker bits to "0". Consequently, IR will go HIGH (if SI is LOW) and OR will go LOW, indicating that the FIFO is now empty.

DC REQUIREMENTS: V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	33511 LIMITS		33512 LIMITS		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	V_{SS}−1.0	V_{SS}+0.3	V_{SS}−1.0	V_{SS}+0.3	V	Note 1
V_{IL}	Input LOW Voltage	V_{GG}	0.8	V_{GG}	0.8	V	Note 1

DC CHARACTERISTICS: V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	33511 LIMITS		33512 LIMITS		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{OH1}	Output HIGH Voltage	V_{SS}−0.5		V_{SS}−0.5		V	I_{OH} = 50 μA
V_{OH2}	Output HIGH Voltage	2.4		2.4		V	I_{OH} = −0.2 mA
V_{OL}	Output LOW Voltage		0.4		0.4	V	I_{OL} = 1.6 mA
V_{II}	Pull Up Initiation Voltage		2.2		2.2	V	Fig. 2, Note 1 I_{IN} = −0.12 mA
V_{IP}	Peak Current Voltage		V_{SS}−1.5		V_{SS}−1.5	V	Fig. 6, Note 1
I_{IP}	Peak Current		1.6		1.6	mA	Fig. 6, Note 1
I_{IH}	Input HIGH Current	0.22		0.22		mA	Fig. 6, Note 1 V_{IN} = V_{SS}−1.0 V
I_{IL}	Input LOW Current		50		50	μA	Fig. 6, Note 1 V_{IN} = 0.4 V
I_{DD}	V_{DD} Current		65		50	mA	
I_{GG}	V_{GG} Current		10		8.0	mA	
P_D	Power Dissipation		520		420	mA	

AC REQUIREMENTS: V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	33511 LIMITS		33512 LIMITS		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{IDS}	$\overline{IE}$ Disable Set-Up Time	20		20		ns	Fig. 6
t_{IDH}	$\overline{IE}$ Disable Hold Time	20		20		ns	Fig. 6
t_{IES}	$\overline{IE}$ Enable Set-Up Time	0		0		ns	Fig. 6
t_{IEH}	$\overline{IE}$ Enable Hold Time	0		0		ns	Fig. 6
t_{DS}	Input Data Set-Up Time	0		0		ns	Fig. 6
t_{DH}	Input Data Hold Time	220		440		ns	Fig. 6
t_{SIH}	SI HIGH Time	220		440		ns	Fig. 6
t_{SIL}	SI LOW Time	280		560		ns	Fig. 6
t_{ODS}	$\overline{OE}$ Disable Set-Up Time	20		20		ns	Fig. 8
t_{ODH}	$\overline{OE}$ Disable Hold Time	20		20		ns	Fig. 8
t_{OES}	$\overline{OE}$ Enable Set-Up Time	0		0		ns	Fig. 8
t_{OEH}	$\overline{OE}$ Enable Hold Time	0		0		ns	Fig. 8
t_{SOL}	SO LOW Time	200		400		ns	Fig. 8
t_{SOH}	SO HIGH Time	300		600		ns	Fig. 8
t_{RPW}	$\overline{MR}$ Pulse Width	100		200		ns	Fig. 8
t_{RS}	$\overline{MR}$ to SI Set-Up Time	0		0		ns	Fig. 8

AC CHARACTERISTICS: V_{SS} = 5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C.

SYMBOL	PARAMETER	33511 LIMITS		33512 LIMITS		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
$t_{SI-IRHL}$	SI to IR Delay Time		220		440	ns	Fig. 6, Note 2
$t_{SI-IRLH}$	SI to IR Delay Time		280		560	ns	Fig. 6, Note 2
$t_{SO-ORLL}$	SO to OR Delay Time		200		400	ns	Fig. 7, Note 2
$t_{SO-ORHH}$	SO to OR Delay Time		300		600	ns	Fig. 7, Note 2
t_{MR-IR}	$\overline{MR}$ to IR Delay Time		300		480	ns	Fig. 8
t_{MR-OR}	$\overline{MR}$ to OR Delay Time		240		480	ns	Fig. 8
t_{BT}	Bubble-Through Time		9.0		15	μs	Fig. 7, Note 3
t_E	Output Enable Time		300		600	ns	Fig. 7
t_D	Output Disable Time		300		600	ns	Fig. 7

NOTES: 1. Includes all Data Inputs, $\overline{IE}$, $\overline{OE}$, SI, SO and $\overline{MR}$. (See Feedback Resistor, Figure 2).
2. HL means positive-going edge of first signal to negative-going edge of second signal, etc.
3. Forward and reverse.

TYPICAL INPUT CHARACTERISTICS

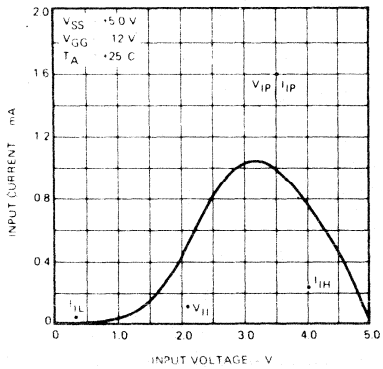


Fig. 4

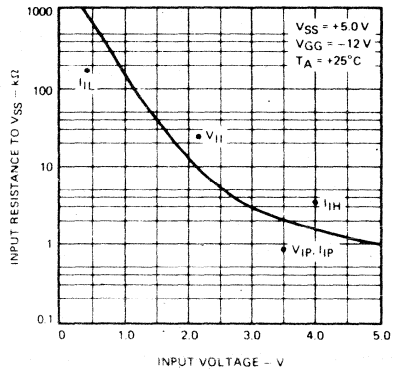


Fig. 5

TIMING DIAGRAMS

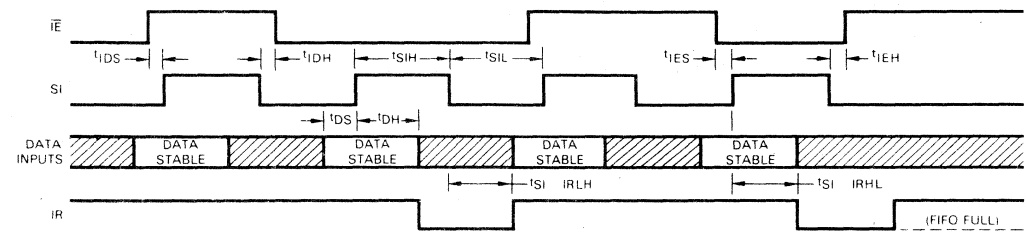


Fig. 6 INPUT TIMING

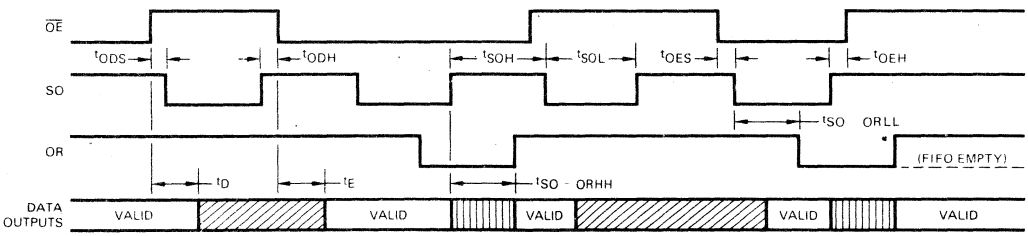


Fig. 7 BUBBLE-THROUGH

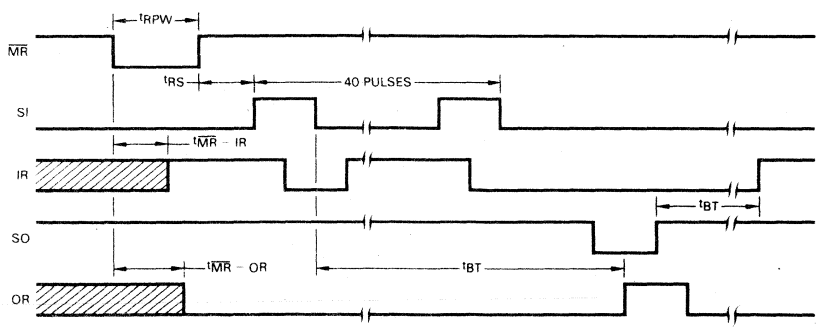


Fig. 8 OUTPUT TIMING

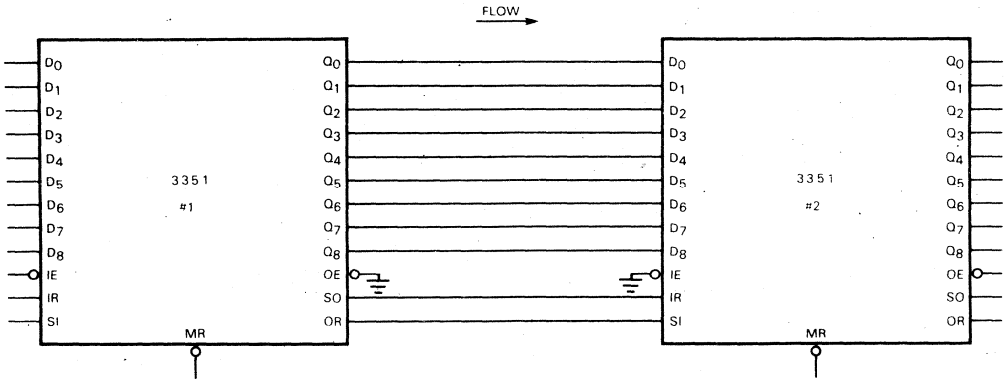


Fig. 9 SIMPLE WORD EXPANSION

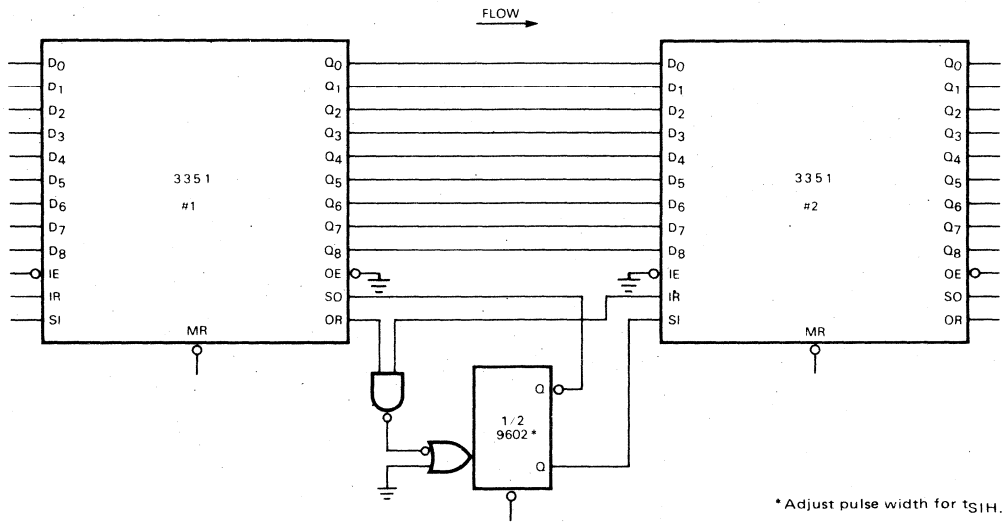
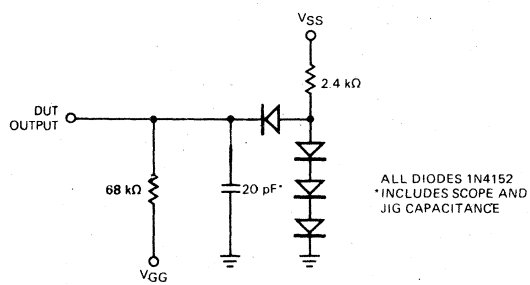


Fig. 10 HIGH SPEED WORD EXPANSION



NOTES:
A. All input t_r and t_f: 10 ns.
B. All times measurements referenced to 1.5 level.

Fig. 11 OUTPUT LOADING

3355/2533

1024-BIT STATIC SHIFT REGISTER

GENERAL DESCRIPTION — The 3355/2533 is a single phase 1024-Bit Static Shift Register with an on-chip clock generator that is driven by a single phase TTL clock. A multiplexer is provided to select from two input sources. A unique on-chip input pull up circuit allows interfacing directly from TTL to all inputs without external components.

The 3355/2533 is manufactured with the P-channel Isoplanar process and is available in 8-pin ceramic or plastic Dual In-line Packages in the commercial temperature range.

- **4.0 MHz (3355) AND 1.5 MHz (2533) GUARANTEED OPERATION**
- **TTL COMPATIBILITY.**
- **SINGLE PHASE TTL CLOCK**
- **LOW CLOCK CAPACITANCE**
- **OPEN RECIRCULATE LOOP**
- **8-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE**

PIN NAMES

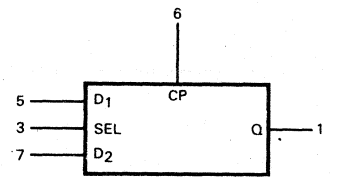
D_n	Data Inputs
Q_n	Data Output
SEL	Data Input Select
CP	Clock Input

ABSOLUTE MAXIMUM RATINGS

V_{GG} and Inputs	-20 V to +0.3 V
V_{DD} and Outputs	-7.0 V to +0.3 V
Output Sink Current	10 mA
Storage Temperature	-55°C to +150°C
Operating Temperature	0°C to +70°C

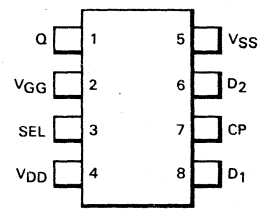
Note: All voltages with respect to V_{SS}.

LOGIC SYMBOL

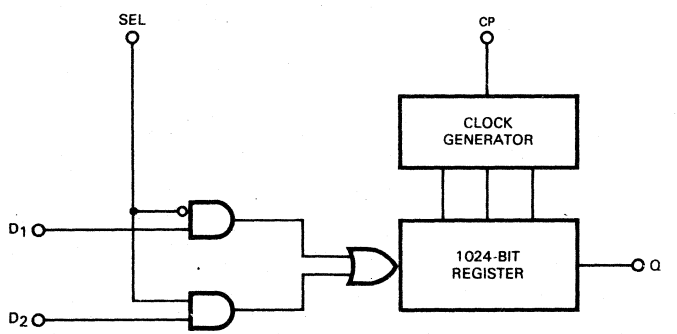


V_{SS} = Pin 8
V_{DD} = Pin 4
V_{GG} = Pin 2

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 3355/2533 is a single phase 1024-Bit Static Shift Register. Data is loaded into the register on the negative transition of the external clock.

The Select Input allows data to enter the register from either D_1 or D_2. D_1 is selected with a LOW on Select and D_2 is selected with a HIGH on Select. This feature allows recirculating of data around all of a cascaded bit string without external logic.

Input Characteristics – The 3355/2533 has a unique pull-up circuit on each input, including the clock, to ensure TTL compatibility. P-channel MOS requires a resistor to pull a TTL output from the HIGH state of 2.4 V toward the +5.0 V power supply (to a minimum of V_{SS}–1). A voltage controlled resistor performs this pull-up function but does not load the TTL output in the LOW state (see Figures 3 and 4).

Output Characteristics – Each output will drive one unit TTL load (1.6 mA at 0.4 V) directly or another unit Shift Register load without any external components.

DC REQUIREMENTS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = –12 V ±5%

SYMBOL	PARAMETER	3355		2533		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	V_{SS} –1	V_{SS} +0.3	V_{SS} –1	V_{SS} +0.3	V	Note 1, Note 2
V_{IL}	Input LOW Voltage	V_{GG}	+0.8	V_{GG}	+0.8	V	Note 1

DC CHARACTERISTICS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = –12 V ±5%

SYMBOL	PARAMETER	3355		2533		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	V_{SS} –1		V_{SS} –1		V	I_{OH} = –0.1 mA, Note 2
V_{OL}	Output LOW Voltage		0.4		0.4	V	I_{OL} = 1.6 mA
V_{II}	Pull-up Initiation Voltage		2.2		2.2	V	Note 1, Figs. 3 and 4
V_{IP}	Peak Current Voltage		V_{SS} –1.5		V_{SS} –1.5	V	Note 1, Figs. 3 and 4
I_{IP}	Peak Input Current		1.6		1.6	mA	Note 1, Figs. 3 and 4
I_{IH}	Input HIGH Current	0.22		0.22		mA	Note 1, V_{IN} = V_{SS} –1.0 V
I_{IL}	Input LOW Current		30		30	μA	Note 1, V_{IN} = 0.4 V
I_{DD}	V_{DD} Current		34		35	mA	Max Operating Frequency
I_{GG}	V_{GG} Current		15		12	mA	
P_D	Power Dissipation		446		398	mW	

AC REQUIREMENTS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = –12 V ±5%

SYMBOL	PARAMETER	3355		2533		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
f	Operating Frequency	0	4.0	0	1.5	MHz	
t_{PWH}	Clock Pulse Width HIGH	0.095	100	0.35	100	μs	Fig. 1, Note 3
t_{PWL}	Clock Pulse Width LOW	0.135	∞	0.25	∞	μs	
t_{DS}	Data Set-Up Time	25		40		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{SS}	Select Set-Up Time	40		70		ns	
t_{SH}	Select Hold Time	10		10		ns	

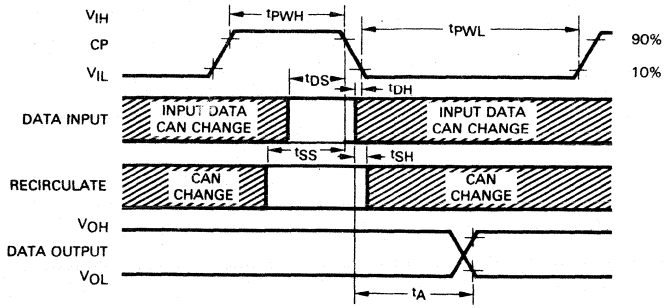
AC CHARACTERISTICS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = –12 V ±5%

SYMBOL	PARAMETER	3355		2533		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_A	Clock to Output Delay		215		300	ns	Fig. 2
C_{IN}	Input Capacitance		5		5	pF	Note 1
C_{OUT}	Output Capacitance		5		5	pF	

NOTES:
1. Applies to inputs D_1, D_2, Clock and Select.
2. See Input Characteristics.
3. t_r, t_f = Clock Transition Time = 0.5 μs maximum. $1/f = t_{PWH} + t_{PWL} + t_r + t_f$.

TIMING DIAGRAM AND AC LOAD

TIMING DIAGRAM



NOTE: Data inputs and Select must be above 90 % or below 10 % during valid time.

Fig. 1

AC LOAD

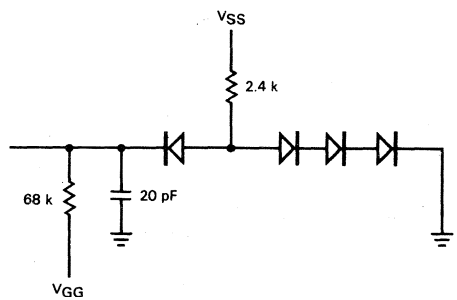


Fig. 2

TYPICAL INPUT CHARACTERISTICS

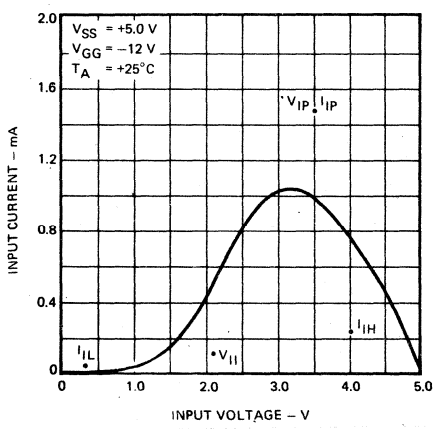


Fig. 3

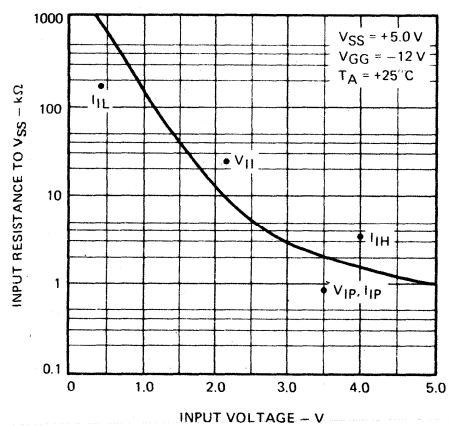


Fig. 4

3357

QUAD 80-BIT STATIC SHIFT REGISTER

GENERAL DESCRIPTION — The 3357 is a single phase Quad 80-Bit Static Shift Register with an on-chip clock generator that is driven by a single phase TTL clock. A multiplexer is provided to allow data to be entered from the input or recirculated from the output. A unique on-chip input pull-up circuit allows interfacing directly from TTL to all inputs without external components.

The 3357 is manufactured with the p-channel Isoplanar process and is available in 16-pin ceramic or plastic Dual In-line Packages in the commercial temperature range.

- **4.0 MHz (33571) AND 2.0 MHz (33572) GUARANTEED OPERATION**
- **ZERO DATA HOLD TIME**
- **TTL COMPATIBILITY**
- **SINGLE PHASE TTL CLOCK**
- **LOW CLOCK CAPACITANCE**
- **INPUT MULTIPLEXER**
- **16-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE**

PIN NAMES

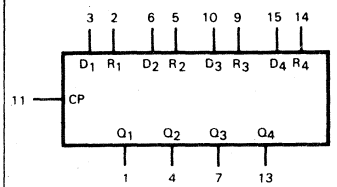
D_n	Data Inputs
Q_n	Data Outputs
R_n	Recirculate Inputs
CP	Clock Input

ABSOLUTE MAXIMUM RATINGS

V_{GG} and Inputs	-20 V to +0.3 V
V_{DD} and Outputs	-7.0 V to +0.3 V
Output Sink Current	10 mA
Storage Temperature	-55°C to +150°C
Operating Temperature	0°C to +70°C

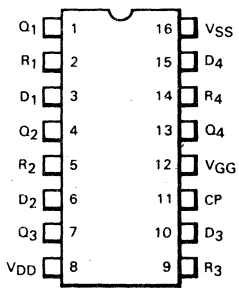
Note: All voltages with respect to V_{SS}

LOGIC SYMBOL

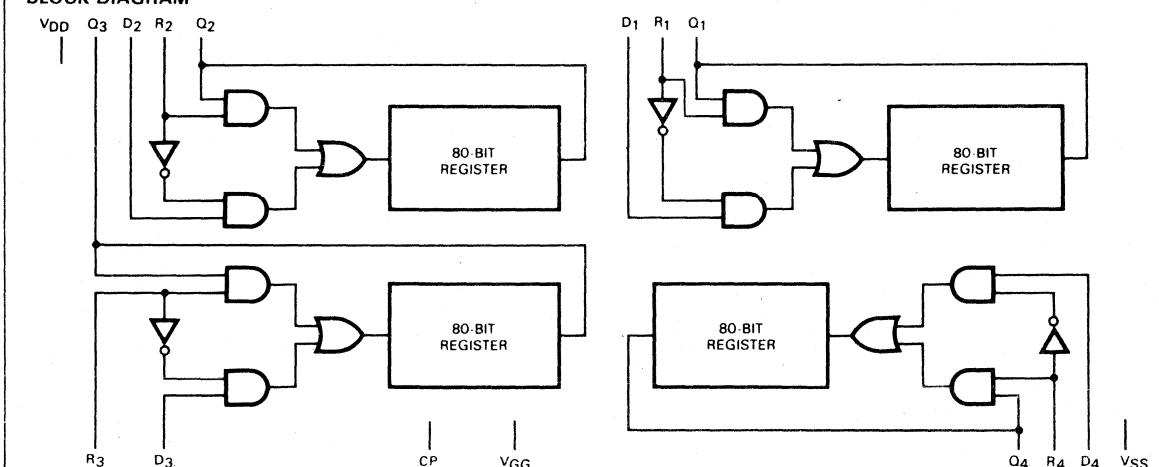


V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION — The 3357 is a single phase Quad 80-Bit Static Shift Register. Data is loaded into the register on the negative transition of the external clock. The Recirculate input choose- between loading new data from the input or recirculating old data from the output. A LOW on Recirculate loads data from the input, and a HIGH loads data from the output.

Input Characteristics — The 3357 has a unique pull-up circuit on each input, including the clock, to ensure TTL compatibility. P-channel MOS requires a resistor to pull a TTL output from the HIGH state of 2.4 V toward the +5.0 V power supply (to a minimum of $V_{SS}-1$). A voltage controlled resistor performs this pull-up function but does not load the TTL output in the LOW state (see Figures 3 and 4).

Output Characteristics — Each output will drive one unit TTL load (1.6 mA at 0.4 V) directly or another unit Shift Register load without any external components.

DC REQUIREMENTS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%

SYMBOL	PARAMETER	33571		33572		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	V_{SS} -1	V_{SS} +0.3	V_{SS} -1	V_{SS} +0.3	V	Note 1
V_{IL}	Input LOW Voltage	V_{GG}	+0.8	V_{GG}	+0.8	V	Note 1

DC CHARACTERISTICS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%

SYMBOL	PARAMETER	33571		33572		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	V_{SS} -1		V_{SS} -1		V	I_{OH} = -0.1 mA,
V_{OL}	Output LOW Voltage		0.4		0.4	V	I_{OL} = 1.6 mA
V_{II}	Input Pull-up Initiation Volt.		2.2		2.2	V	Note 1, $I_{IN} < -0.12$ mA
V_{IP}	Input Peak Current Voltage		V_{SS} -1.5		V_{SS} -1.5	V	Note 1
I_{IP}	Input Peak Current		1.6		1.6	mA	Note 1
I_{IH}	Input HIGH Current	0.22		0.22		mA	Note 1, $V_{IN} = V_{SS} - 1.0$ V
I_{IL}	Input LOW Current		30		30	µA	Note 1, V_{IN} = 0.4 V
I_{DD}	V_{DD} Current		20		18	mA	Max Operating Frequency
I_{GG}	V_{GG} Current		15		10.5	mA	
P_D	Power Dissipation		375		285	mW	

AC REQUIREMENTS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%

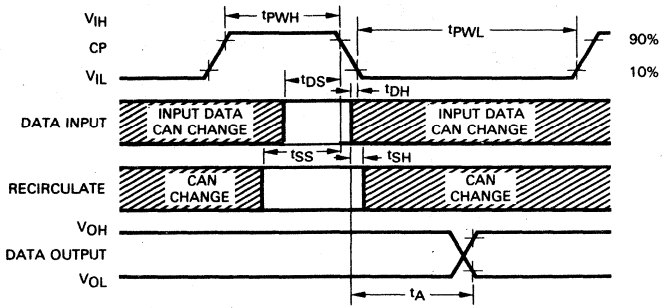
SYMBOL	PARAMETER	33571		33572		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
f	Operating Frequency	0	4.0	0	2.0	MHz	
t_{PWH}	Clock Pulse Width HIGH	0.095	100	0.25	100	µs	Fig. 1, Note 2
t_{PWL}	Clock Pulse Width LOW	0.135		0.25		µs	
t_{DS}	Data Set-Up Time	25		40		ns	
t_{DH}	Data Hold Time	0		0		ns	
t_{SS}	Select Set-Up Time	40		70		ns	
t_{SH}	Select Hold Time	10		10		ns	

AC CHARACTERISTICS: T_A = 0°C to +70°C, V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = -12 V ±5%

SYMBOL	PARAMETER	33571		33572		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_A	Clock to Output Delay		215		260	ns	Fig. 2
C_{IN}	Input Capacitance		5		5	pF	Note 1
C_{OUT}	Output Capacitance		5		5	pF	

NOTES:
1. Applies to all inputs including Clock.
2. t_r, t_f = Clock Transition Time = 0.5 µs.

TIMING DIAGRAM



NOTE: Data Inputs and Select must be above 90% or below 10% during valid time.

Fig. 1

AC LOAD

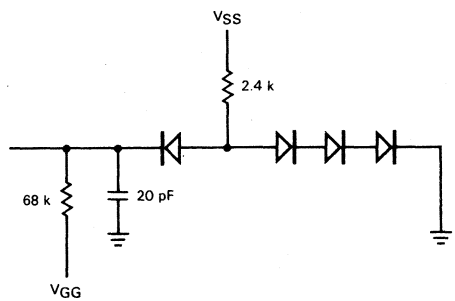


Fig. 2

TYPICAL INPUT CHARACTERISTICS

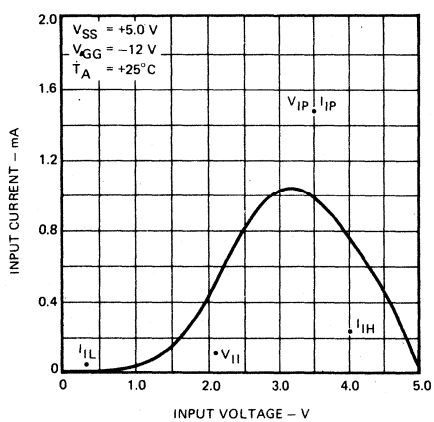


Fig. 3

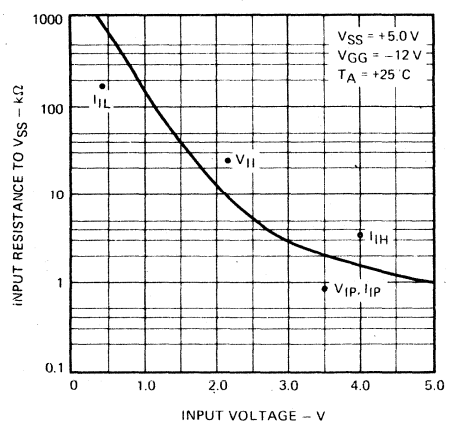


Fig. 4

3515
4096-BIT READ ONLY MEMORY

GENERAL DESCRIPTION – The 3515 is a 4096-Bit Last Mask Programmable Read Only Memory. It is organized in a 512-word by 8-bit format. There are four programmable Chip Selects to allow up to 16 chips to be wired-OR. The 3515 is manufactured with the p-channel Isoplanar Silicon Gate process and is available in the 24-pin ceramic Dual In-line Package in the commercial temperature range, 0°C to 70°C.

- **FAST CODE TURNAROUND (LAST MASK PROGRAMMABLE)**
- **INTERFACES DIRECTLY WITH TTL – NO EXTERNAL COMPONENTS**
- **600 ns ACCESS TIME (MAX)**
- **4-BIT PROGRAMMABLE CHIP SELECT CODE**
- **3-STATE OUTPUTS FOR WIRED-OR CAPABILITY**
- **STATIC LOGIC – NO CLOCKS REQUIRED**
- **24-PIN CERAMIC DUAL IN-LINE PACKAGE**
- **APPLICATIONS – CODE CONVERSION, TABLE LOOK-UP, CONTROL LOGIC, PROGRAM STORAGE**

ABSOLUTE MAXIMUM RATINGS

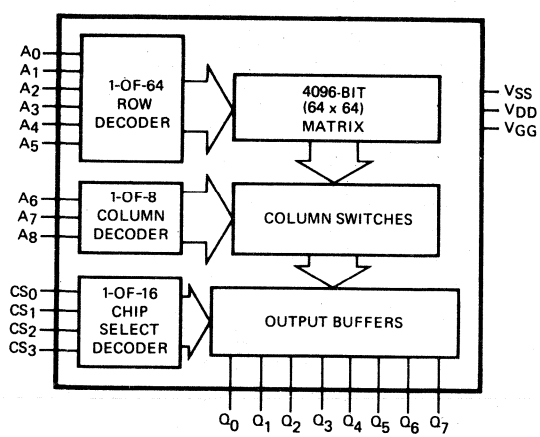
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C
Voltage on Any Input Pin	-20 V to +0.3 V
Voltage on V_{DD}	-7 V to +0.3 V
Voltage on Output Pin (Output Current @ ± 10 mA)	-7 V to +0.3 V

Note: All voltages with respect to V_{SS}

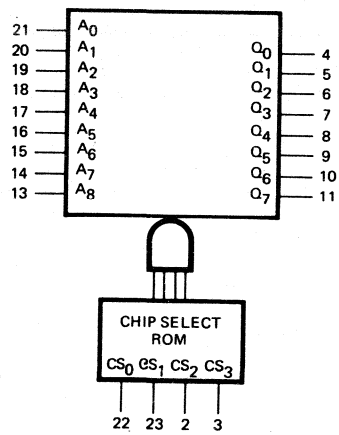
PIN NAMES

A_n	Address Inputs
Q_n	Data Outputs
CS_n	Chip Selects

LOGIC BLOCK DIAGRAM

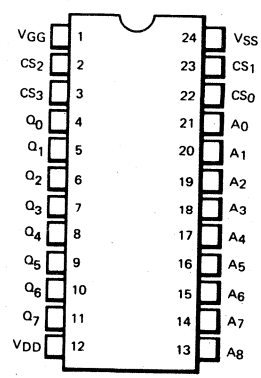


LOGIC SYMBOL



V_{SS} = Pin 24
V_{DD} = Pin 12
V_{GG} = Pin 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – A 9-bit binary address applied to the address ($A_0 - A_8$) will cause a corresponding 8-bit word to appear on the outputs ($Q_0 - Q_7$). A 4-bit programmable Chip Select (CS_{0-3}) allows selection of 1 of 16 memories without external gating. When a chip is not selected, its outputs are turned off, *i.e.*, a high impedance to both V_{SS} and V_{DD}. This feature allows expansion of up to 16 memories without external components, either for chip select decoding or for output gating. Each output of the device will drive 1.5 unit TTL loads.

Each input to the 3515 drives a special input amplifier stage which eliminates the need for pull-up resistors.

Two types of information must be supplied when ordering the 3515: first, the bit pattern to be stored in the 512 word locations of the memory; and second, the 4-bit chip enable code which will activate the chip.

DC CHARACTERISTICS: V_{GG} = -12 V ±5%, V_{DD} = 0 V, V_{SS} = +5.0V ±5%, T_A = 0°C to +70°C

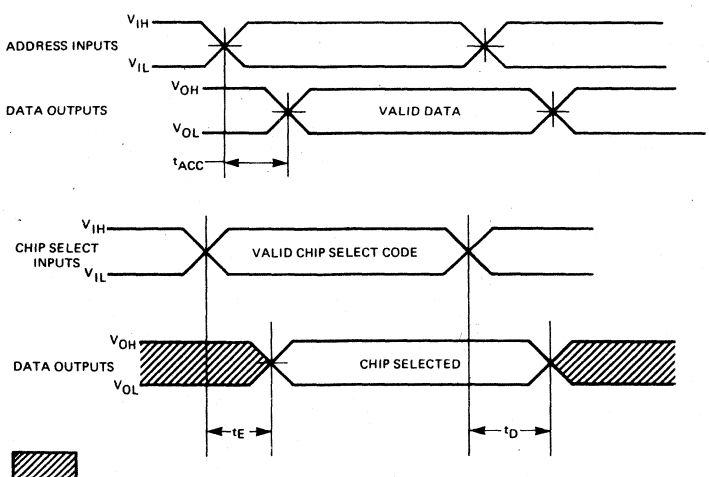
SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS} -2.75 V	V_{SS}	V	
V_{IL}	Input LOW Voltage	V_{GG}	0.55	V	
V_{OH}	Output HIGH Voltage	2.4	V_{SS}	V	I_{OH} = -0.5 mA
V_{OL}	Output LOW Voltage	0	0.4	V	I_{OL} = 2.4 mA
I_{IN}	Input Leakage Current		1.0	μA	V_{IN} = V_{SS} -6 V, Note 1
I_{OUT}	Output Leakage Current		1.0	μA	V_{OUT} = V_{SS} -6 V, Note 2
I_{DD}	V_{DD} Current		35	mA	
I_{GG}	V_{GG} Current		19	mA	
P_D	Power Dissipation		510	mW	

AC CHARACTERISTICS: V_{GG} = -12 V ±5%, V_{DD} = 0 V, V_{SS} = +5.0 V ±5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
t_{ACC}	Access Time Address to Output		600	ns	Note 3
t_E	Access Time Chip Select Enable to Output		600	ns	
t_D	Access Time Chip Select Disable to Output		600	ns	
C_{IN}	Input Capacitance		8.0	pF	f = 1 MHz; V_{IN} = V_{SS}
C_{OUT}	Output Capacitance		12	pF	Note 2, f = 1 MHz, V_{OUT} = V_{SS}

NOTES:
1. All pins at 0 V except those under test.
2. Output floating (chip not selected).
3. 1.5 TTL load.

TIMING DIAGRAM



ORDERING INFORMATION – The 3515 is programmed from punched cards or a coding form in the format shown below.

Logic "1" = a more positive voltage ($\approx V_{SS}$)
Logic "0" = a more negative voltage ($\approx V_{DD}$)

FIRST CARD

CUSTOMER INFORMATION

Column Number	Description
10 thru 29	Customer Name
35 thru 39	Blank
50 thru 62	3515
65 thru 80	Customer Comment Field

SECOND CARD

Column Number	Description
29	CS_3 input required to select chip
31	CS_2 input required to select chip
33	CS_1 input required to select chip
35	CS_0 input required to select chip

REMAINING 512 CARDS

Column Number	Description
10, 12, 14, 16, 18, 20, 22, 24, 26	Address input pattern. The most significant bit (A_8) is in column 10
40, 42, 44, 46, 48, 50, 42, 54	Output pattern. The most significant bit (O_7) is in column 40
73 thru 80	Coding these columns is not essential and may be used for card identification purposes

35L38
256 × 4 STATIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION – The 35L38 is a 256-word by 4-bit Static Random Access Memory. It requires a single 5 V power supply, is fully TTL compatible on the inputs and outputs and requires no clocking or refresh. The Chip Select ($\overline{CS}$) controls a 3-state output which allows the outputs to be wired-OR. The 35L38 features a power-down mode during standby operation where the device dissipates a maximum of 37 mW.

The 35L38 is manufactured with the n-channel Isoplanar process. It is available in the 22-pin ceramic Dual In-line Package in the commercial temperature range, 0°C to 70°C.

- **FAST ACCESS TIME (400 ns and 500 ns)**
- **SINGLE 5 V POWER SUPPLY**
- **TTL COMPATIBLE ON INPUTS AND OUTPUTS**
- **TOTALLY STATIC – NO CLOCKS OR REFRESH**
- **3-STATE OUTPUTS**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **22-PIN CERAMIC DUAL IN-LINE PACKAGE**
- **184 mW P_D GUARANTEED**
- **POWER DOWN STANDBY MODE**

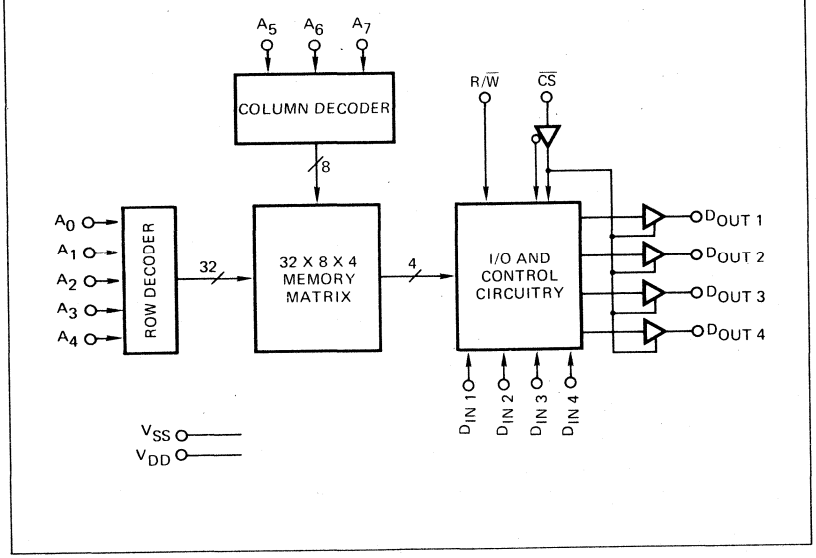
PIN NAMES

A_n	Address Inputs
D_{OUTX}	Data Outputs
D_{INX}	Data Inputs
$R/\overline{W}$	Read/Write Control Input
$\overline{CS}$	Chip Select

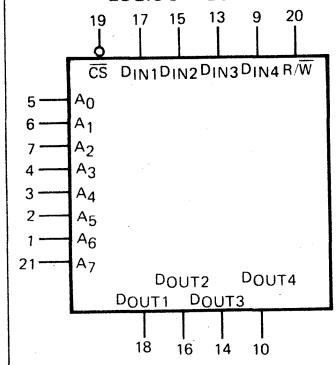
ABSOLUTE MAXIMUM RATINGS

Any Pin with Respect to V_{SS}	−0.5 V to +7.0 V
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

BLOCK DIAGRAM

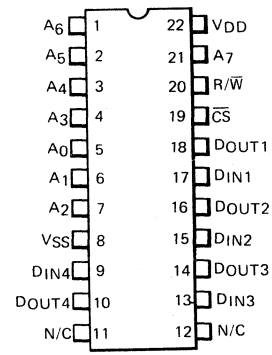


LOGIC SYMBOL



V_{SS} = Pin 8
V_{DD} = Pin 22
N/C = Pins 11, 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



N/C = No Connection

TRUTH TABLE

$\overline{CS}$	$R/\overline{W}$	D_{INX}	D_{OUTX}	Comments
H	X	X	*	Chip Deselected
L	L	H	H	Write "1"†
L	L	L	L	Write "0"†
L	H	X	D_n	Read †

X = Don't Care
* = Output HIGH Impedance State
D_n = Data at Addressed Location
† = Chip Selected

FUNCTIONAL DESCRIPTION — The 35L38 is a 256 x 4 static RAM. When the Chip Select ($\overline{CS}$) goes HIGH, the Read/Write (R/$\overline{W}$) input is disabled and the Data Outputs (D_{OUT}) are forced into a high impedance state. When Chip Select goes LOW, the Read/Write is enabled.

When R/$\overline{W}$ goes LOW, data from the Data Inputs (D_{IN}) is written at the location specified by the Address Inputs (A_n). The Data Outputs will be identical to the Data Inputs during a write command. When R/$\overline{W}$ goes HIGH, the contents of the addressed location will appear at D_{OUT}. D_{OUT} is not inverted from D_{IN} in the 35L38.

DC REQUIREMENTS: T_A = 0°C to +70°C

SYMBOL	PARAMETER	35L38BDC		35L38ADC		35L38DC		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	2.0	V_{DD}	2.0	V_{DD}	2.0	V_{DD}	V	V_{DD} = +5.0 V ± 5%,
V_{IL}	Input LOW Voltage	−0.5	0.8	−0.5	0.8	−0.5	0.8	V	V_{SS} = 0 V

DC CHARACTERISTICS: T_A = 0°C to +70°C, V_{DD} = +5.0 V ±5%, V_{SS} = 0 V

SYMBOL	PARAMETER	35L38BDC		35L38ADC		35L38DC		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	2.4		2.4		2.4		V	I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	I_{OL} = 3.2 mA
I_{IN}	Input Leakage Current		10		10		10	μA	V_{IN} = $V_{DD(Max)}$
I_{OUT}	Output Leakage Current	−10	10	−10	10	−10	10	μA	V_{OUT} = 0 V to $V_{DD(Max)}$
I_{DD}	Power Supply Current		35		35		35	mA	
P_D	Power Dissipation		184		184		184	mW	

POWER DOWN CHARACTERISTICS: T_A = 0°C to +70°C

SYMBOL	PARAMETER	35L38B, 35L38A, 35L38		UNITS	CONDITIONS
		MIN	MAX		
I_{DD} (P.D.)	Power Supply Current		23	mA	V_{DD} = 1.6 V
V_{DD} (P.D.)	Power Supply Voltage	1.6		V	
t_{CSS}	Chip Select Set-Up Time	100		ns	See Fig. 2
t_{CSH}	Chip Select Hold Time	100		ns	
$V_{\overline{CS}}$	Chip Select Voltage	2.0		V	
V_{DD}	Power Supply Slew Rate		100	V/μs	

AC REQUIREMENTS: T_A = 0°C to +70°C

SYMBOL	PARAMETER	35L38 BDC		35L38 ADC		35L38 DC		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{CYC}	Read or Write Cycle Time	400		500		650		ns	V_{DD} = +5.0 V ± 5%, V_{SS} = 0 V
t_{AW}	Address to Write Time	100		150		200		ns	
t_{WP}	Write Pulse Width	200		250		350		ns	
t_{WR}	Write Recovery Time	50		50		50		ns	
t_{DS}	Data Set-up Time	150		200		250		ns	
t_{DH}	Data Hold Time	50		50		50		ns	
t_{CW}	Chip Select to Write Time	200		250		350		ns	
t_{WC}	Write to Chip Select Time	50		50		50		ns	

AC CHARACTERISTICS: T_A = 0°C to +70°C

SYMBOL	PARAMETER	35L38B		35L38A		35L38		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_A	Read Access Time		400		500		650	ns	V_{DD} = +5.0 V ± 5%, V_{SS} = 0 V
t_{CO}	Chip Select to Output Time		200		200		250	ns	
t_{OH1}	Data Valid After Address	50		50		50		ns	
t_{OH2}	Previous Data Valid After Chip Deselect	0	150	0	150	0	200	ns	
C_{IN}	Input Capacitance		5		5		5	pF	T_A = 25°C, f = 1 MHz,
C_{OUT}	Output Capacitance		10		10		10	pF	V_{IN} = V_{SS}, V_{OUT} = V_{SS}

WAVEFORMS

READ CYCLE TIMING

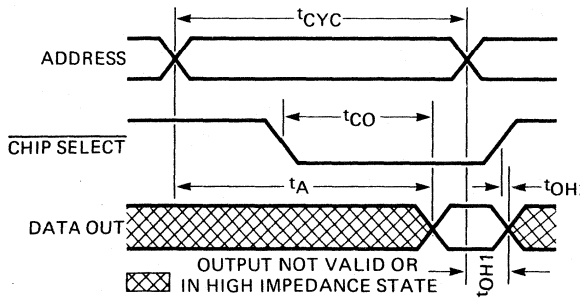


Fig. 1

POWER DOWN MODE TIMING

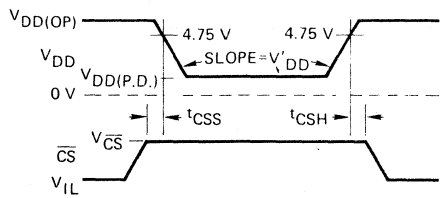
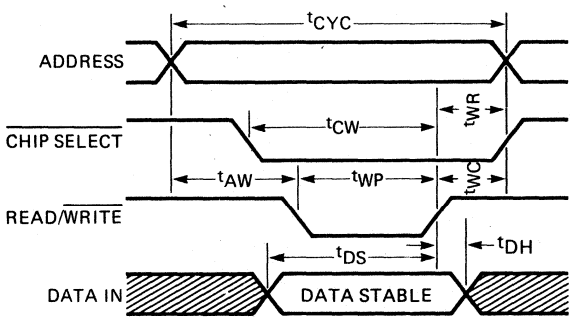


Fig. 2

WRITE CYCLE TIMING



AC CONDITIONS
Input Levels: $V_{IL(max)}$ to $V_{IH(min)}$
Input Rise and Fall Times: 10 ns

Timing Measurement Reference Level: 1.5 V
Output Load: 2 TTL Gate + 100 pF

Fig. 3

3538
256 × 4 STATIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION — The 3538 is a 256-word by 4-bit Static Random Access Memory. It requires a single 5 V power supply, is fully TTL compatible on the inputs and outputs and requires no clocking or refresh. The Chip Select ($\overline{CS}$) controls a 3-state output which allows the outputs to be wired-OR.

The 3538 is manufactured with the n-channel Isoplanar process. It is available in the 22-pin ceramic Dual In-line Package in commercial, limited military or military temperature ranges.

- **FAST ACCESS TIME (350 ns and 450 ns)**
- **SINGLE 5 V POWER SUPPLY**
- **TTL COMPATIBLE ON INPUTS AND OUTPUTS**
- **TOTALLY STATIC — NO CLOCKS OR REFRESH**
- **3-STATE OUTPUTS**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **22-PIN CERAMIC DUAL IN-LINE PACKAGE**

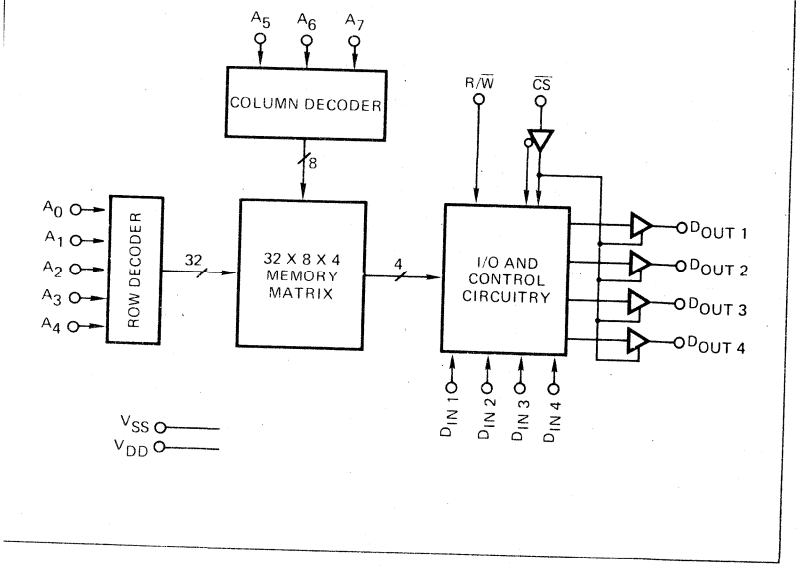
PIN NAMES

A_n	Address Inputs
D_{OUTX}	Data Outputs
D_{INX}	Data Inputs
$R/\overline{W}$	Read/Write Control Input
$\overline{CS}$	Chip Select

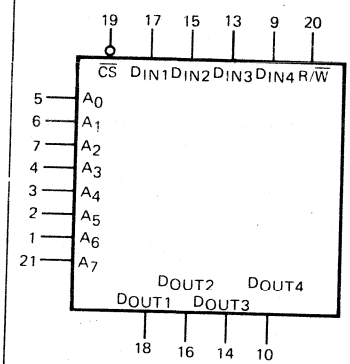
ABSOLUTE MAXIMUM RATINGS

Any Pin with Respect to V_{SS}		−0.5 V to +7.0 V
Storage Temperature		−55°C to +150°C
Operating Temperature:	DC	0°C to +70°C
	DL	−55°C to +85°C
	DM	−55°C to +125°C

BLOCK DIAGRAM

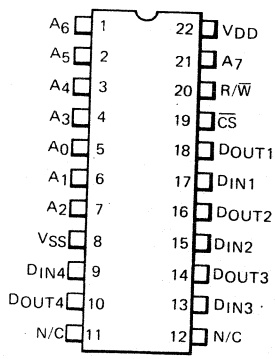


LOGIC SYMBOL



V_{SS} = Pin 8
V_{DD} = Pin 22

CONNECTION DIAGRAM
DIP (TOP VIEW)



N/C = No Connection

TRUTH TABLE

$\overline{CS}$	$R/\overline{W}$	D_{INX}	D_{OUTX}	Comments
H	X	X	*	Chip Deselected
L	L	H	H	Write "1"†
L	L	L	L	Write "0"†
L	H	X	D_n	Read †

X = Don't Care
* = Output HIGH Impedance State
D_n = Data at Addressed Location
† = Chip Selected

FUNCTIONAL DESCRIPTION – The 3538 is a 256 x 4 static RAM. When the Chip Select ($\overline{CS}$) goes HIGH, the Read/Write (R/$\overline{W}$) input is disabled and the Data Outputs (D_{OUT}) are forced into a high impedance state. When Chip Select goes LOW, the Read/Write is enabled.

When R/$\overline{W}$ goes LOW, data from the Data Inputs (D_{IN}) is written at the location specified by the Address Inputs (A_n). The Data Outputs will be identical to the Data Inputs during a write command. When R/$\overline{W}$ goes HIGH, the contents of the addressed location will appear at D_{OUT}. D_{OUT} is not inverted from D_{IN} in the 3538.

DC REQUIREMENTS: DC: T_A = 0°C to +70°C; DL: T_A = –55°C to +85°C; DM: T_A = –55°C to +125°C

SYMBOL	PARAMETER	DC		DL		DM		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	2.2	V_{DD}	2.0	V_{DD}	2.0	V_{DD}	V	
V_{IL}	Input LOW Voltage	–0.5	0.65	–0.5	0.8	–0.5	0.8	V	V_{SS} = 0 V
V_{DD}	Power Supply Voltage	4.75	5.25	4.50	5.50	4.50	5.50	V	

DC CHARACTERISTICS: DC: T_A = 0°C to +70°C; DL: T_A = –55°C to +85°C; DM: T_A = –55°C to +125°C
V_{SS} = 0 V, $V_{DD(Min)} \leq V_{DD} \leq V_{DD(Max)}$ (Note 1)

SYMBOL	PARAMETER	DC		DL		DM		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	2.2		2.2		2.2		V	I_{OH} = –100 μA
V_{OL}	Output LOW Voltage		0.45		0.45		0.45	V	I_{OL} = 1.9 mA
I_{IN}	Input Leakage Current		10		10		10	μA	$V_{IN} = V_{DD(Max)}$
I_{OUT}	Output Leakage Current	–10	10	–10	10	–10	10	μA	V_{OUT} = 0 V to $V_{DD(Max)}$
I_{DD}	Power Supply Current		60		70		70	mA	$V_{IN} = V_{DD(Max)}$

AC REQUIREMENTS: DC: T_A = 0°C to +70°C; DL: T_A = –55°C to +85°C; DM: T_A = –55°C to +125°C

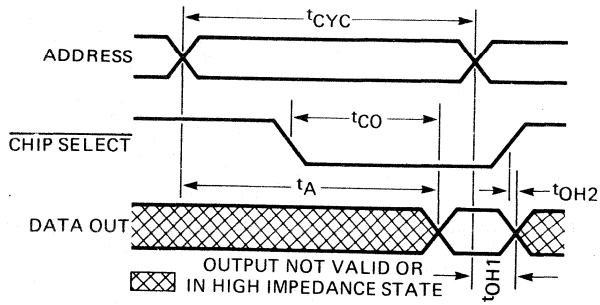
SYMBOL	PARAMETER	3538F DC/DL/DM		3538-1 DC/DL/DM		3538 DC/DL/DM		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{CYC}	Read or Write Cycle Time	350		450		650		ns	
t_{AW}	Address to Write Time	100		170		200		ns	
t_{WP}	Write Pulse Width	170		200		350		ns	$V_{DD(Min)} \leq V_{DD} \leq V_{DD(Max)}$ (See Note 1) V_{SS} = 0 V
t_{WR}	Write Recovery Time	50		50		50		ns	
t_{DS}	Data Set-up Time	170		200		350		ns	
t_{DH}	Data Hold Time	50		50		50		ns	
t_{CW}	Chip Select to Write Time	200		250		400		ns	
t_{WC}	Write to Chip Select Time	50		50		50		ns	

AC CHARACTERISTICS: DC: T_A = 0°C to +70°C; DL: T_A = –55°C to +85°C; DM: T_A = –55°C to +125°C

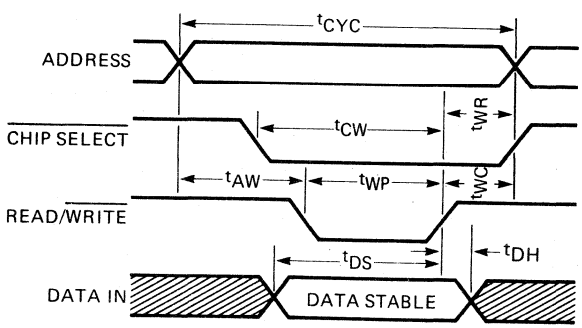
SYMBOL	PARAMETER	3538F DC/DL/DM		3538-1 DC/DL/DM		3538 DC/DL/DM		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_A	Read Access Time		350		450		650	ns	
t_{CO}	Chip Select to Output Time		180		200		400	ns	$V_{DD(Min)} \leq V_{DD} \leq V_{DD(Max)}$ (See note 1) V_{SS}= 0 V
t_{OH1}	Data Valid After Address	50		50		50		ns	
t_{OH2}	Previous Data Valid After Chip Deselect	0		0		0		ns	
C_{IN}	Input Capacitance		5		5		5	pF	V_{IN} = 0 V, f = 1 MHz, T_A = 25°C, V_{SS} = 0 V
C_{OUT}	Output Capacitance		10		10		10	pF	

TE 1: See DC Requirements.

READ CYCLE TIMING



WRITE CYCLE TIMING



AC CONDITIONS:

Input Levels: $V_{IL(Max)}$ to $V_{IH(Max)}$
Input Rise and Fall Times: 10 ns
Timing Measurement Reference Level: 1.5 V
Output Load: 1 TTL Gate + 100 pF

3539

256 × 8 STATIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION – The 3539 is a 2048-bit Static Read/Write Random Access Memory. Organized as 256 8-bit words, the 3239 features a common I/O structure which allows packaging in a standard 22-pin ceramic DIP. This device uses a single +5 volt power supply and is TTL-compatible on inputs and outputs. The 3539 is manufactured using Fairchild's n-channel Isoplanar process.

- **256 x 8 WITH COMMON I/O BUS**
- **STANDARD 22-PIN DIP**
- **SINGLE +5 VOLT POWER SUPPLY**
- **COMPLETELY STATIC – NO CLOCKS OR REFRESH**
- **TOTALLY TTL-COMPATIBLE**
- **650 NS MAXIMUM ACCESS TIME**
- **<500 mW POWER DISSIPATION**
- **TWO SEPARATE CHIP SELECT INPUTS**
- **SEPARATE OUTPUT DISABLE FUNCTION**

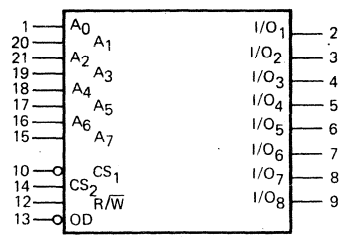
PIN NAMES

An	Address Inputs
$\overline{CS}_n$	Chip Select Inputs
$\overline{OD}$	Output Disable
R/W	Read/Write Control Input
I/O_n	Data Buss Pins
V_{DD}	+5 V Power Supply
V_{SS}	0 V Power Supply

ABSOLUTE MAXIMUM RATINGS

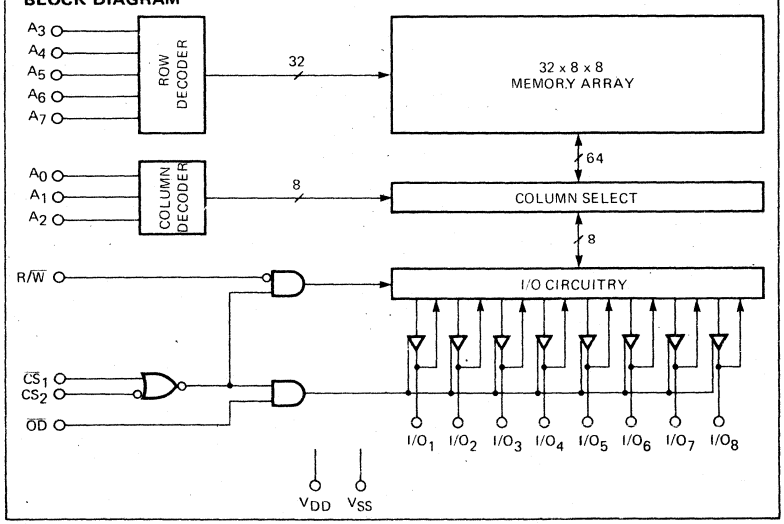
Any Pin with Respect to V_{SS}	−0.5 V to + 7.0 V
Storage Temperature	−55°C to + 150°C
Operating Temperature	0°C to + 70°C

LOGIC SYMBOL

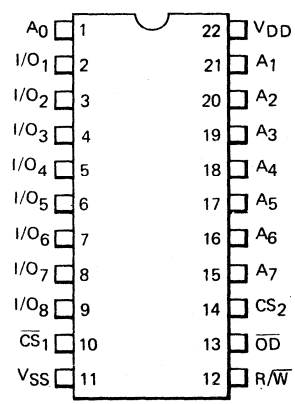


V_{DD} = PIN 22
V_{SS} = PIN 11

BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION: The 3539 uses a multiplexed Input/Output (I/O) structure, allowing the device to be packaged in a 22-pin DIP. The I/O network is controlled by the Read/Write (R/$\overline{W}$), Output Disable ($\overline{OD}$), and two Chip Select ($\overline{CS}_1$ and CS_2) inputs.

The I/O network is in a high impedance state and the R/$\overline{W}$ input disabled whenever $\overline{CS}_1$ is HIGH or CS_2 is LOW. When $\overline{CS}_1$ is LOW and CS_2 is HIGH the circuit will read or write, depending on the $\overline{OD}$ and R/$\overline{W}$ inputs.

When $\overline{OD}$ is HIGH, the eight I/O pins are in the Output mode, so that the R/$\overline{W}$ input should be HIGH to force the chip into a read mode. However, when R/$\overline{W}$ is HIGH, the $\overline{OD}$ can be used as a chip select input, turning the outputs off when it goes LOW.

When the R/$\overline{W}$ and $\overline{CS}_1$ are LOW and CS_2 is HIGH, the circuit is in the write mode. $\overline{OD}$ must be LOW to turn off the output structures. Data is then entered from the I/O pins. The $\overline{OD}$ is used to turn off the output structures independent of the Chip Selects, allowing input data to be entered at the I/O ports sooner than if the I/O were controlled by R/$\overline{W}$. Output data is not inverted by the 3539. The output buffers will each drive one standard TTL Load.

The eight address inputs specify which location of the memory array will be selected for the read or write operations. Each control, address and I/O input is directly TTL-compatible.

DC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$; $V_{DD} = 5.0\ V \pm 5\%$

SYMBOL	PARAMETER	35391		35392		3539		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	2.2		2.2		2.2		V	
V_{IL}	Input LOW Voltage		0.65		0.65		0.65	V	
V_{OH}	Output HIGH Voltage	2.2		2.2		2.2		V	$I_{OH} = -100\ \mu A$
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	$I_{OL} = 1.6\ mA$
I_{BH}	Bus HIGH Current		10		10		10	μA	$V_{IN} = V_{DD}$, Chip Deselected
I_{BL}	Bus LOW Current		-10		-10		-10	μA	$V_{IN} = 0\ V$, Chip Deselected
I_{DD}	Power Supply Current		95		95		95	mA	$V_{DD} = 5.25\ V$
PD	Power Dissipation		500		500		500	mW	

AC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$; $V_{DD} = 5.0\ V \pm 5\%$

SYMBOL	PARAMETER	35391		35392		3539		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{CYC}	Read or Write Cycle Time	400		500		650		ns	
t_A	Read Access Time		400		500		650	ns	
t_{AW}	Address to Write Delay	150		200		300		ns	
t_{DS}	Data Set-Up Time	200		250		275		ns	
t_{DH}	Data Hold Time	25		25		50		ns	
t_{WR}	Write Recovery Time	75		75		100		ns	
t_{WW}	Write Pulse Width	175		225		250		ns	
t_{CS}	Chip select to write set-up time	100		125		200		ns	
t_{CD}	Chip Select Delay Time		100		100		100	ns	
t_{CH}	Chip select to write hold time	25		25		50		ns	
t_{OD}	Output Disable Time		150		150		150	ns	
t_{OE}	Output Enable Time		150		150		150	ns	

TRUTH TABLE

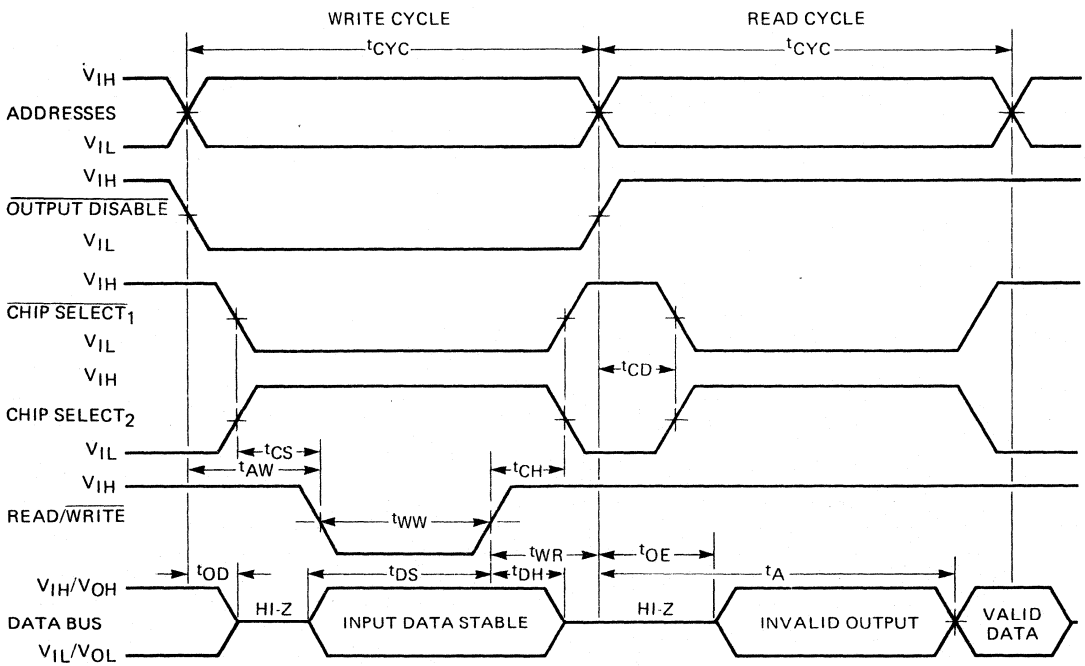
CONTROL INPUTS				3539 OPERATING MODE				I/O BUS MODE		
$\overline{CS_1}$	CS_2	$\overline{OD}$	R/$\overline{W}$	Selected	Deselected	Write	Read	Input	Output	HI-Z
H	X	X	X		•					•
X	L	X	X		•					•
L	H	L	L	•		•		•		
L	H	H	L	•		•			•	
L	H	L	H	•			•			•
L	H	H	H	•			•		•	

X = IRRELEVENT STATE

L = LOW ($-V_{SS}$)

H = HIGH ($-V_{DD}$)

3539 TIMING DIAGRAM



4096

4096×1 DYNAMIC RANDOM ACCESS MEMORY

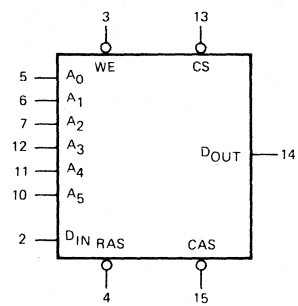
GENERAL DESCRIPTION – The 4096DC is a 4096-bit dynamic Random Access Memory organized as 4096 one-bit words. This device is designed utilizing the single transistor dynamic memory cell.

A unique address multiplexing and latching technique permits the packaging of the 4096DC in a standard 16-pin ceramic Dual In-line Package. The use of this package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment.

The 4096DC features direct TTL compatibility, on-chip address, data input and data output latches, TTL-level clocks with extremely low capacitance and a range of access times from 200 ns (4096-2DC) to 350 ns (4096-5DC). The 4096DC is manufactured using the n-channel Isoplanar process.

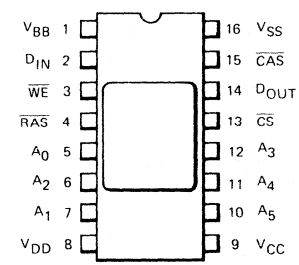
- **ALL INPUTS TTL-COMPATIBLE, INCLUDING CLOCKS**
- **ON-CHIP LATCHES FOR ADDRESSES, CHIP SELECT, DATA INPUT**
- **THREE-STATE TTL-COMPATIBLE OUTPUT**
- **CHIP SELECT DECODING DOES NOT ADD TO ACCESS TIME**
- **READ OR WRITE CYCLES: 4096-2: 300 ns, 4096-3: 360 ns, 4096-4: 420 ns, 4096-5: 500 ns**
- **ACTIVE POWER: 4096-2: <431 mW, 4096-3: <378 mW, 4096-4: <341 mW, 4096-5: <315 mW**
- **STANDBY POWER: <25 mW**
- **STANDARD 16-PIN CERAMIC PACKAGE**

LOGIC SYMBOL

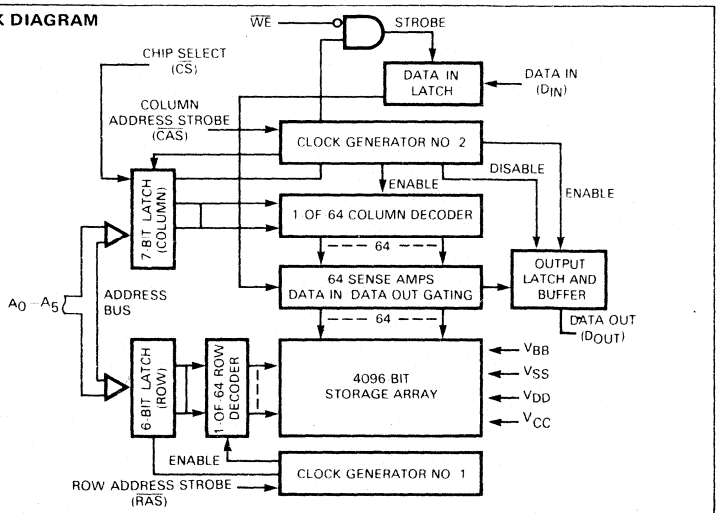


V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

CONNECTION DIAGRAM DIP (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

An	Address Inputs	D_{OUT}	Data Output
D_{IN}	Data Input	V_{CC}	+5 V Power Supply
$\overline{CS}$	Chip Select Input	V_{SS}	0 V Power Supply
$\overline{WE}$	Write Enable Input	V_{BB}	−5 V Power Supply
$\overline{RAS}$	Row Address Strobe (Clock) Input	V_{DD}	+12 V Power Supply
$\overline{CAS}$	Column Address Strobe (Clock) Input		

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage of any pin relative to V_{BB}	−0.5 V to +25.0 V
Operating Temperature	0°C to 70°C
Storage Temperature (Ambient)	−55°C to 150°C

ADDRESSING – The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits onto the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits plus Chip Select ($\overline{CS}$) onto the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system access or cycle time.

DATA INPUT/OUTPUT – Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WE}$ and $\overline{CAS}$. The last of these signals making its negative transition is the strobe for the Data In register. This permits several options in the write timing. In a write cycle, if the $\overline{WE}$ input is activated prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to this signal. If the cycle is to be a read-write cycle or read-modify-write cycle, then the $\overline{WE}$ input will not go to a logic 0 until after the access time has elapsed. But now, because $\overline{CAS}$ is ready at a logic 0, the Data In is strobed in by $\overline{WE}$ and the set-up hold times are referenced to $\overline{WE}$.

At the beginning of a memory cycle the state of the Data Out Latch and buffer depend on the previous memory cycle. If during the previous cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read, read-write, or read-modify-write cycle and the chip was selected then the output latch and buffer will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the previous cycle was a write cycle ($\overline{WE}$ active low before access time) and the chip was selected, then the output latch and buffer will contain a logic 1. Regardless of the state of the output it will remain valid until $\overline{CAS}$ goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until after an access time has elapsed. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a WRITE command and the output will remain in the open-circuit state.

INPUT/OUTPUT LEVELS – All inputs, including the two address strobes, will interface directly with TTL. The high impedance, low capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Even though the inputs may be driven directly by TTL gates, pull-up or termination resistors are normally required in a system to prevent ringing of the input signals due to line inductance and reflections. In high speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series rather than parallel terminations may be employed at some degradation of system speed.

The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The resistance to V_{CC} is 500 ohms maximum and 150 ohms typically. The resistance to V_{SS} is 200 ohms maximum and 100 ohms typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which chips are interfaced. During battery standby operation, the V_{CC} pin may be unpowered without affecting the 4096 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH – Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any read cycle refreshes the selected row, regardless of the state of the Chip Select. A write, read-write, or read-modify-write cycle also refreshes the selected row but the chip should be unselected to prevent writing data into the selected cell.

POWER DISSIPATION/STANDBY MODE – Most of the circuitry used in the 4096 is dynamic and draws power only as the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency. Typically, the power is 120mW at a 1 μS cycle time for the 4096DC with a worst case power of less than 341 mW at a 420 ns cycle time. To reduce the overall system power the Row Address Strobe ($\overline{RAS}$) must be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected outputs). But those chips that did not receive a $\overline{RAS}$ will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the output. If the $\overline{RAS}$ is decoded and supplied to the selected chips, then the Chip Select input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	V	2
V_{CC}	Supply Voltage	4.5	5.0	V_{DD}	V	2
V_{SS}	Supply Voltage	0	0	0	V	2,12
V_{BB}	Supply Voltage	−5.5	−5.0	−4.5	V	2
V_{IH1}	Input HIGH Voltage Address Input	2.4	5.0	V_{GG}	V	2,14
V_{IL}	Input LOW Voltage, All Inputs	−1.0	0	0.6	V	2,14
V_{IH2}	Input HIGH Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$	2.7	5.0	V_{GG}	V	2,14

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0 V ± 5%, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = −5.0 V ± 10%)

SYMBOL	PARAMETER	PART NUMBER								UNITS	NOTES
		4096-2		4096-3		4096-4		4096-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I_{DD1}	Average V_{DD} Power Supply Current		35		30		27		25	mA	16
I_{CC}	V_{CC} Power Supply Current									mA	9
I_{BB}	Average V_{BB} Power Supply Current		75		75		75		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		2		2		2		2	mA	
I_{IN}	Input Leakage Current (Any Input)		10		10		10		10	μA	10
I_{OUT}	Output Leakage Current		10		10		10		10	μA	11
V_{OH}	Output HIGH Voltage at I_{OUT} = −5 mA	2.4		2.4		2.4		2.4		V	
V_{OL}	Output LOW Voltage at I_{OUT} = 2 mA		0.4		0.4		0.4		0.4	V	
C_{IN1}	Input Capacitance ($A_0 - A_5$)		10		10		10		10	pF	
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WE}$, $\overline{CS}$)		7		7		7		7	pF	
C_{OUT}	Output Capacitance (D_{OUT})		8		8		8		8	pF	

RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0 V ± 5%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = −5.0 V ± 10%) (Note 17)

SYMBOL	PARAMETER	PART NUMBER								UNITS	NOTES
		4096-2		4096-3		4096-4		4096-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	300		365		425		500		ns	3
t_{RAC}	Access Time from ROW Address Strobe		200		250		300		350	ns	3, 15
t_{CAC}	Access Time from Column Address Strobe		120		150		175		200	ns	4
t_{OFF}	Output Buffer Turn-Off Delay	0	70	0	80	0	90	0	100	ns	4
t_{RP}	ROW Address Strobe Precharge Time	100		115		125		150		ns	
t_{RCL}	ROW to Column Strobe Lead Time	80		100		125		150		ns	3
t_{CPW}	Column Address Strobe Pulse Width	120		150		175		200		ns	
t_{AS}	Address Set-Up Time	0		0		0		0		ns	3, 4
t_{AH}	Address Hold Time	50		60		70		80		ns	3, 4
t_{CH}	Chip Select Hold Time	70		80		90		100		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		0		ns	4
t_{RCH}	Read Command Hold Time	30		35		40		45		ns	5
t_{WCH}	Write Command Hold Time	90		110		140		150		ns	4, 6
t_{WP}	Write Command Pulse Width	120		150		175		200		ns	
t_{CRL}	Column to ROW Strobe Lead Time	−20		−20		−20	+20	−20		ns	7
t_{CWL}	Write Command to Column Strobe Lead Time	120		150		175		200		ns	13
t_{DS}	Data In Set-Up Time	0		0		0		0		ns	13
t_{DH}	Data In Hold Time	90		110		130		150		ns	13
t_{RFSH}	Refresh Period		2		2		2		2	ms	
t_{MOD}	Modify Time		10		10		10		10	μs	8

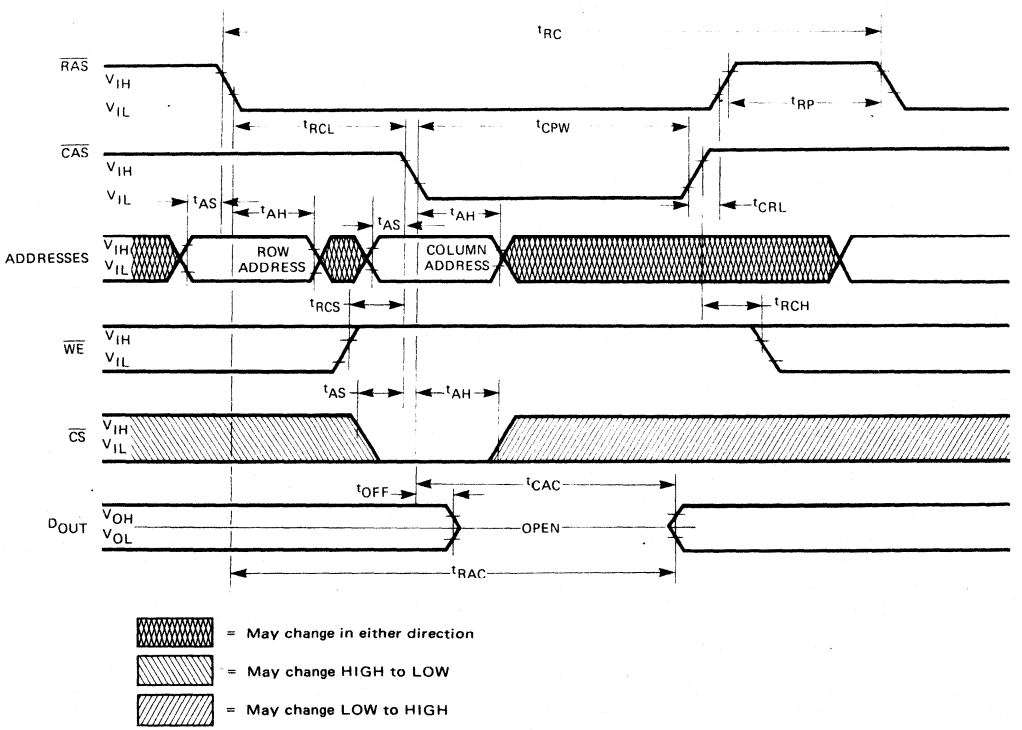
Notes on following page.

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}.
3. Referenced to $\overline{RAS}$ leading edge.
4. Referenced to $\overline{CAS}$ leading edge.
5. Referenced to $\overline{CAS}$ trailing edge.
6. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read-modify-write cycles, the Write Command Pulse Width is the limiting parameter.
7. Referenced to the $\overline{RAS}$ trailing edge.
8. Referenced to access time.
9. Depends upon output loading. The V_{CC} supply is connected only to the output buffer.
10. All device pins at 0 volts except V_{BB} at −5 volts and pin under test which is at +10 volts.
11. Output disabled by chip select input.
12. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}.
13. These parameters are referenced to the $\overline{CAS}$ leading edge in random write cycle operation and to the $\overline{WE}$ leading edge in read-write or read-modify-write cycles.
14. Input voltages greater than TTL levels (0 to 5 V) require device operation at reduced speed.
15. Assumes t_{RCL} minimum.
16. Current is proportional to speed with maximum current measured at fastest cycle rate.
17. AC measurements assume ≈10 ns rise and fall times.

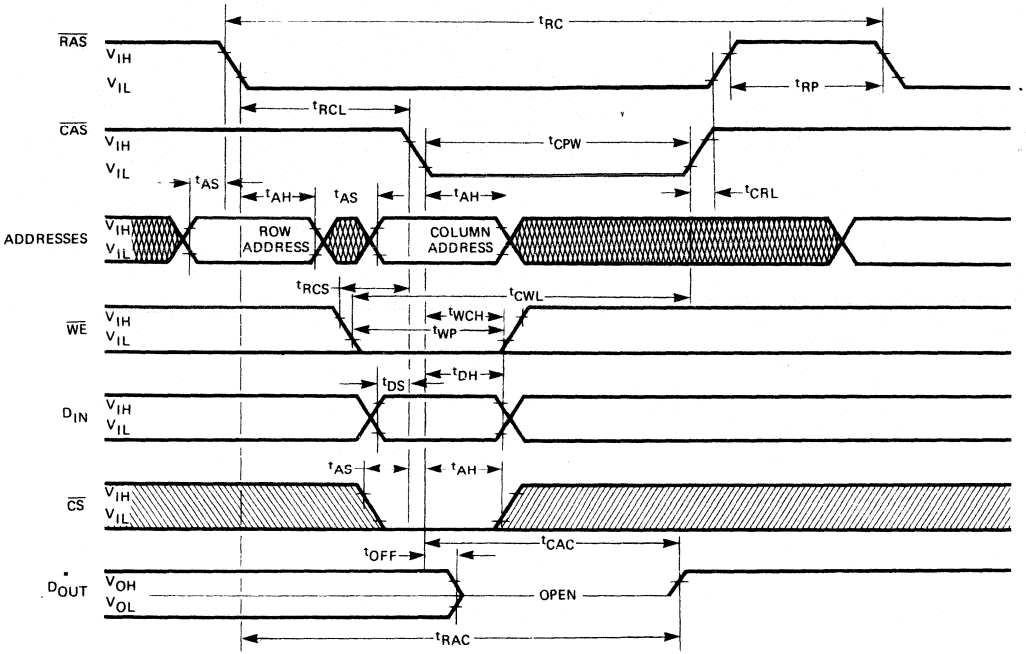
TIMING DIAGRAMS

READ CYCLE

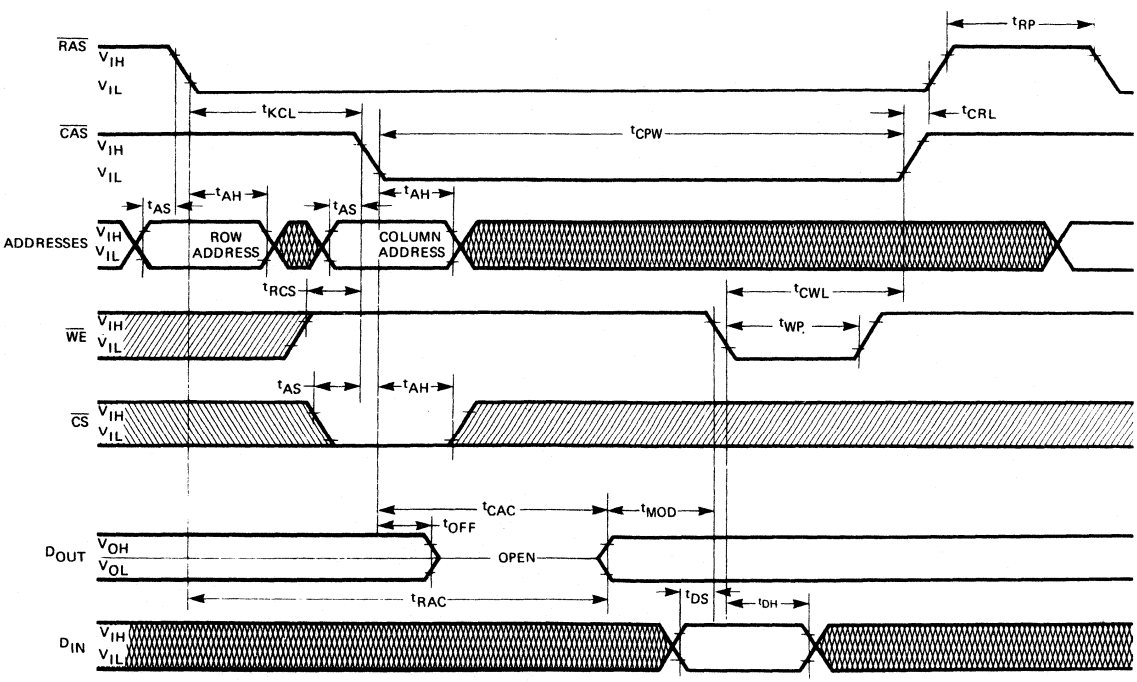


TIMING DIAGRAMS (Cont'd)

WRITE CYCLE



READ-MODIFY-WRITE CYCLE*



*Read-modify-write cycle time = $t_{RCL} + t_{CAC} + t_{MOD} + t_{CWL} + t_{CRL} + t_{RP} + 3\,t_f + t_r$.

3262A

TV SYNC GENERATOR

GENERAL DESCRIPTION – The 3262A is a Sync Pulse Generator that produces the necessary outputs for synchronizing television broadcast information. These outputs include Horizontal Drive, Vertical Drive, Composite Sync, Composite Blanking, and Even and Odd Fields, all of which are provided in the format specified by RS170EIA Standard Output Signals. The Color Subcarrier (3.58 MHz) and the Color Burst Flag outputs are provided for color operation. All waveforms are derived from a low-voltage two-phase clock (for color operation) or a single phase low-voltage clock for black and white operation. All outputs except the Color Subcarrier are capable of driving a TTL load directly. The Color Subcarrier is designed to drive a capacitive load. The 3262A is a monolithic integrated circuit manufactured with Isoplanar p-channel silicon gate technology.

- **COLOR OR BLACK/WHITE OPERATION**
- **ALL COUNTERS SYNCHRONOUS**
- **PULSE WIDTHS DERIVED DIGITALLY**
- **LOW POWER DISSIPATION – < 567 mW**
- **OUTPUTS DRIVE TTL DIRECTLY (EXCEPT COLOR SUBCARRIER)**
- **SEPARATE VERTICAL AND HORIZONTAL RESET**

APPLICATIONS

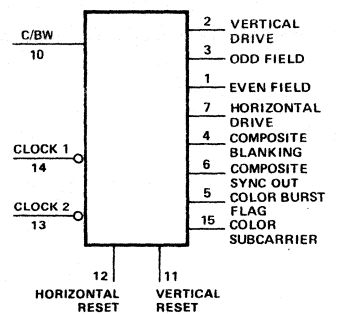
- **CAMERA LOGIC REPLACEMENT**
- **HOME TV GAMES**
- **VIDEO TAPE RECORDERS**
- **VIDEO TERMINALS**

ABSOLUTE MAXIMUM RATINGS

All Inputs (Note 1)	−20 V to +0.3 V
V_{GG}	−20 V to +0.3 V
V_{DD} and Outputs	−6 V to +0.3 V
DC Output Current (when output LOW)	< 10 mA
Storage Temperature	−55°C to 150°C
Operating Temperature	0°C to 70°C
Maximum Power Dissipation	750 mW

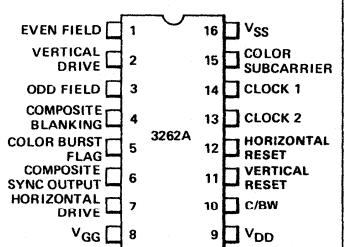
Note 1. All Inputs with respect to V_{SS}.

LOGIC SYMBOL

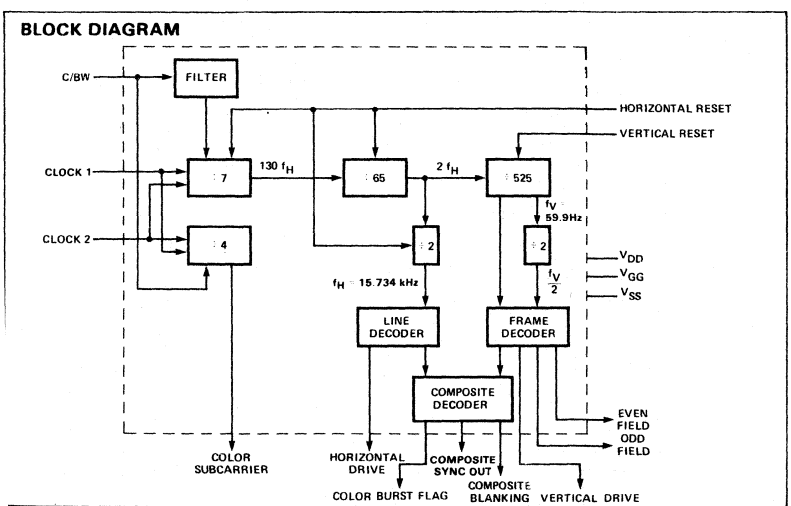


V_{SS} = Pin 16
V_{DD} = Pin 9
V_{GG} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The 3262A block diagram shows the counting and decoding scheme used to generate all output waveforms. The clock frequency is divided down in three steps (÷7, ÷65, ÷2) and decoded to generate the horizontal drive. A signal at twice the horizontal frequency is divided by 525 to generate the vertical drive. The Color Subcarrier is generated by a ÷4 Johnson counter driven directly from the input clock. This is approximately a sinusoidal signal. Pulses at the horizontal and vertical frequencies are combined in the composite decoder to generate the outputs Composite Sync, Composite Blanking, and Color Burst Flag.

For use in special applications, the 3262A provides a 30 Hz pulse at the start of the field (Odd Field) and again at the start of the next field (Even Field).

Separate Horizontal and Vertical Reset input pins are provided to allow the 3262A to be used in systems requiring gen-lock operation. Tie Horizontal and Vertical Resets to V_{SS} when they are not used.

The C/BW input is used to select either color or black and white operation. A logic HIGH applied to C/BW will select color operation; if C/BW is LOW, the ÷4 and ÷7 counters will be bypassed for black and white operation. In addition, the only clock needed for black and white operation is Clock 1; Clock 2 should be tied to V_{SS}. The input frequency should be 2.0475 MHz for normal operation.

C/BW when LOW also resets the Color Subcarrier. If the LOW pulse on C/BW is within the specification for t_{RS} – Color Subcarrier Reset Pulse – the color operation for the 3262A will be unaffected.

DC CHARACTERISTICS: V_{SS} = 5.1 ± .25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS} −0.8		V_{SS} +0.3	V	
V_{IL}	Input LOW Voltage	−5.0		V_{SS} −4.35	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −0.1 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{IHC}	Clock Input HIGH Voltage	V_{SS} −1.0		V_{SS} +0.3	V	
V_{ILC}	Clock Input LOW Voltage	−5.0 V		V_{SS} −4.35	V	
$V_{SUBCARRIER}$	Subcarrier Output Voltages Approx. Sine Wave	0.5			V (Peak to Peak)	C = 10 pF to V_{DD}* R = 10 kΩ to V_{DD}*
I_{IN}	Input Leakage Current		1.0		μA	V_{IN} = 0 V
I_{DD}	V_{DD} Current		30		mA	
I_{GG}	V_{GG} Current		15		mA	

*Subcarrier Output should be D.C. blocked with .01 μF before loading.

AC CHARACTERISTICS: V_{SS} = 5.1 ± .25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, C_L = 10 pF, 1 TTL Load (1.6 mA), T_A = 0°C to +70°C (See Timing diagrams)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
f	Input Frequency Color	13.3	14.31818	15.4	MHz	See Fig. 2, t_r, $t_f \leq$ 5 ns
f_1	Input Frequency Black/White	1.5	2.0475	2.2	MHz	See Fig. 2, t_r, $t_f \leq$ 20 ns
t_{PW1}	B/W Clock LOW Time	200	215	230	ns	t_r, $t_f \leq$ 20 ns
$t_{\overline{PW1}}$	B/W Clock HIGH Time	200	215		ns	t_r, $t_f \leq$ 20 ns
t_{PW2}	Color Clock LOW Time	30	35	40	ns	t_r, $t_f \leq$ 5 ns
$t_{\overline{PW2}}$	Color Clock HIGH Time	30	35		ns	t_r, $t_f \leq$ 5 ns
t_{0V}	Color Clock Overlap Time			5	ns	
$t_{HR\ PW}$	Horizontal Reset Pulse Width	200			ns	t_r, $t_f \leq$ 20 ns
$t_{VR\ PW}$	Vertical Reset Pulse Width	200*			ns	t_r, $t_f \leq$ 20 ns
t_{RS}	Color Subcarrier Reset Pulse Width on C/BW	130		200	ns	t_r, $t_f \leq$ 20 ns

*If t_{HR} occurs simultaneously; if t_{HR} does not occur, t_{VR} = 400 ns min.

RS170EIA TIMING DIAGRAM

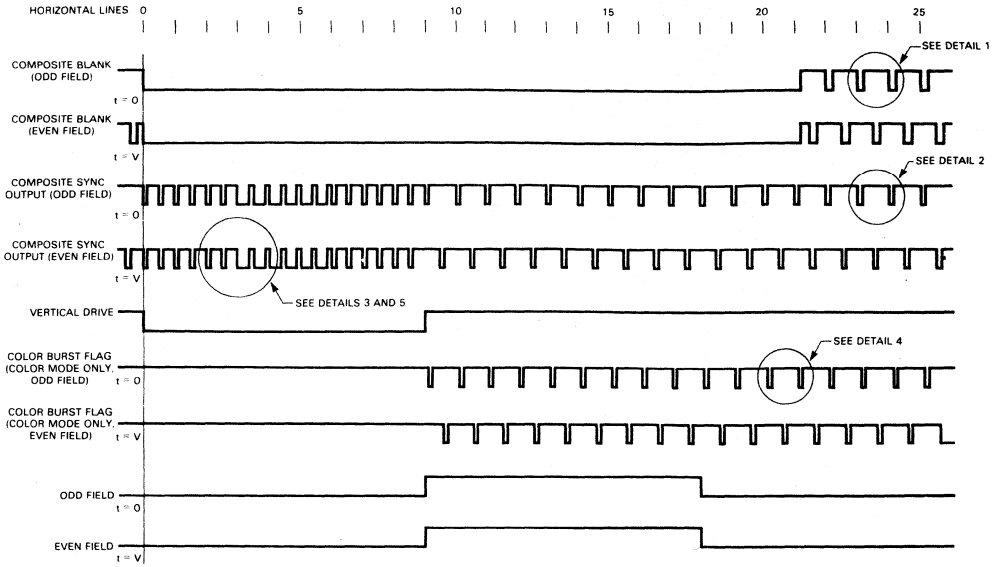
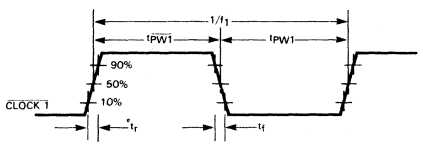
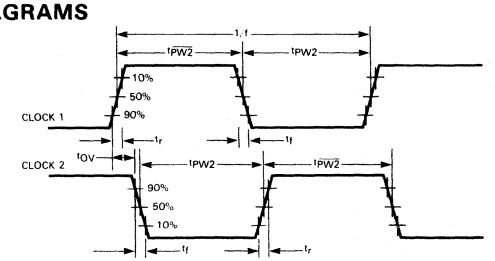


Fig. 1

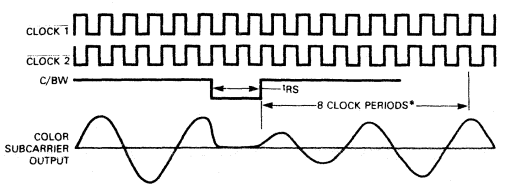
CLOCK TIMING DIAGRAMS



a) Black and White Clock

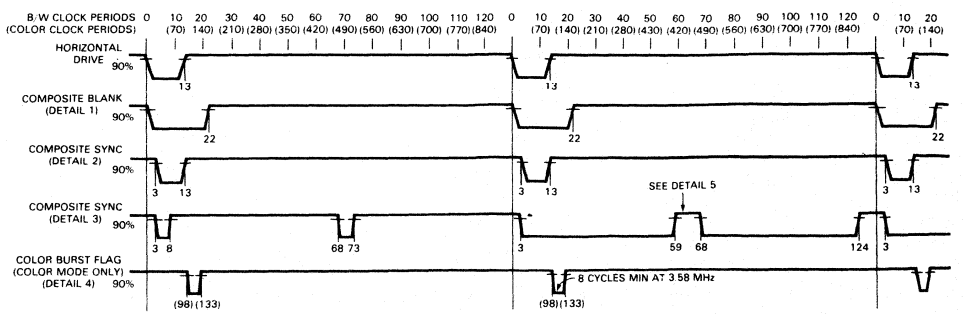


b) Color Clocks



*MAX. SUBCARRIER AMPLITUDE ATTAINED WITHIN 8 COLOR CLOCK PERIODS FOLLOWING RISING EDGE OF C/BW.

c) Color Subcarrier Timing and Reset Detail



d) RS170EIA Timing Details

Fig. 2

HORIZONTAL AND/OR VERTICAL RESET DETAIL (DETAIL 5)

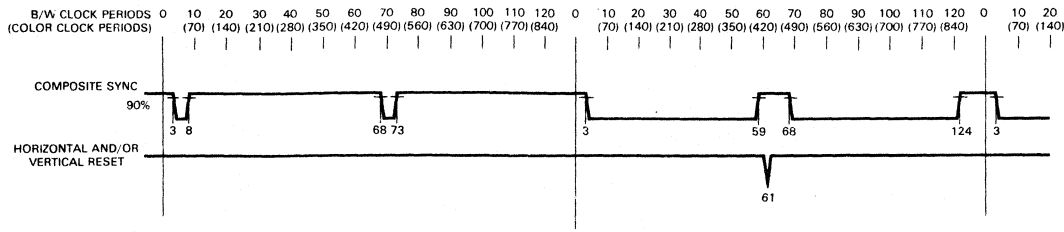
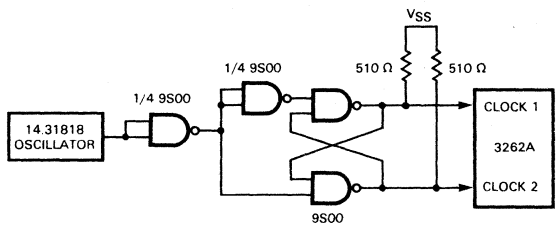
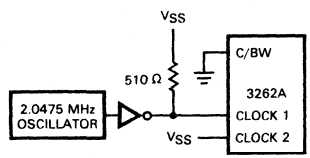


Fig. 3

CLOCK GENERATOR CIRCUITRY



a) Color Clocks



b) Black and White Clock

Fig. 4

APPLICATION TV CAMERA SYSTEM

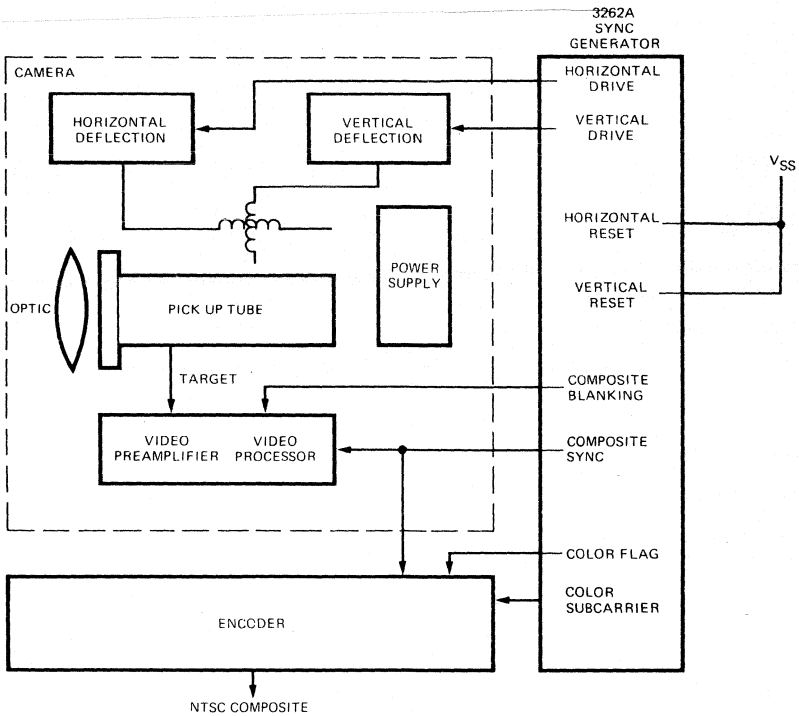


Fig. 5

3262B

TV SYNC GENERATOR FOR GEN-LOCK

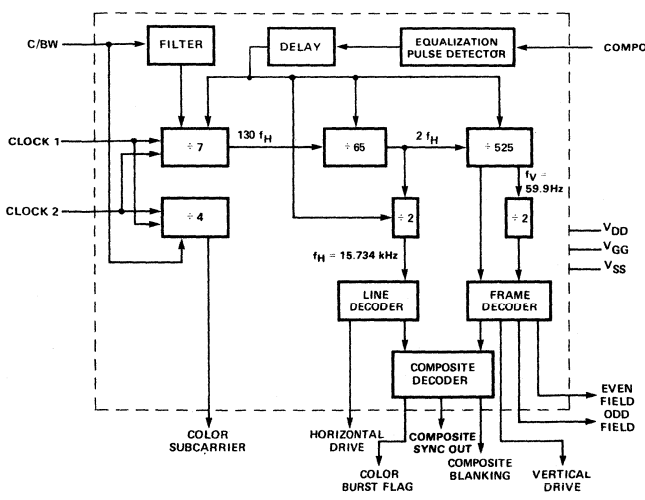
GENERAL DESCRIPTION – The 3262B is a Sync Pulse Generator that produces the necessary outputs for synchronizing television broadcast information. These outputs include Horizontal Drive, Vertical Drive, Composite Sync, Composite Blanking, and Even and Odd Fields, all of which are provided in the format specified by RS170EIA Standard Output Signals. The Color Subcarrier (3.58 MHz) and the Color Burst Flag outputs are provided for color operation. All waveforms are derived from a low-voltage two-phase clock (for color operation) or a single phase low-voltage clock for black and white operation. All outputs except the Color Subcarrier are capable of driving a TTL load directly. The Color Subcarrier is designed to drive a capacitive load. The 3262B is a monolithic integrated circuit manufactured with Isoplanar p-channel silicon gate technology.

- **COLOR OR BLACK/WHITE OPERATION**
- **ALL COUNTERS SYNCHRONOUS**
- **PULSE WIDTHS DERIVED DIGITALLY**
- **LOW POWER DISSIPATION – < 567 mW**
- **OUTPUTS DRIVE TTL DIRECTLY (EXCEPT COLOR SUBCARRIER)**
- **IDEAL FOR GEN-LOCK OPERATION – SYNCHRONIZES TO COMPOSITE SYNC INPUT**

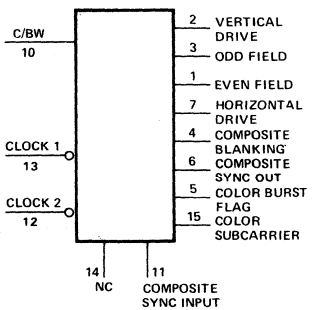
APPLICATIONS

- **CAMERA LOGIC REPLACEMENT**
- **HOME TV GAMES**
- **VIDEO TAPE RECORDERS**
- **VIDEO TERMINALS**

BLOCK DIAGRAM

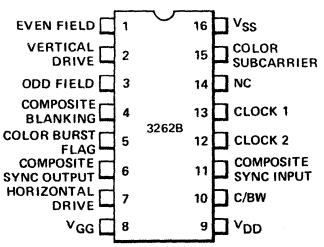


LOGIC DIAGRAM



V_{SS} = Pin 16
V_{DD} = Pin 9
V_{GG} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = NO CONNECTION

ABSOLUTE MAXIMUM RATINGS

All Inputs (Note 1)	−20 V to +0.3 V
V_{GG}	−20 V to +0.3 V
V_{DD} and Outputs	−6 V to +0.3 V
DC Output Current (when output LOW)	< 10 mA
Storage Temperature	−55°C to 150°C
Operating Temperature	0°C to 70°C
Maximum Power Dissipation	750 mW

Note 1. All Inputs with respect to V_{SS}

FUNCTIONAL DESCRIPTION – The 3262B block diagram shows the counting and decoding scheme used to generate all output waveforms. The clock frequency is divided down in three steps (÷7, ÷65, ÷2) and decoded to generate the horizontal drive. A signal at twice the horizontal frequency is divided by 525 to generate the vertical drive. The Color Subcarrier is generated by a ÷4 Johnson counter driven directly from the input clock. This is approximately a sinusoidal signal. Pulses at the horizontal and vertical frequencies are combined in the composite decoder to generate the outputs Composite Sync, Composite Blanking, and Color Burst Flag.

For use in special applications, the 3262B provides a 30 Hz pulse at the start of the field (Odd Field) and again at the start of the next field (Even Field).

The Composite Sync Input is provided for gen-lock operation. The detection circuit shown in the block diagram detects the first equalizing pulse in the Odd Field and, as a result, generates a reset. This causes the Composite Sync Output and Composite Sync Input to synchronize such that Composite Sync Output occurs before Composite Sync Input (See Figure 3). For gen-lock application the input clock must be locked to master generator clock in order to provide stable operation.

The C/BW input is used to select either color or black and white operation. A logic HIGH applied to C/BW will select color operation; if C/BW is LOW, the ÷4 and ÷7 counters will be bypassed for black and white operation. In addition, the only clock needed for black and white operation is Clock 1; Clock 2 should be tied to V_{SS}. The input frequency should be 2.0475 MHz for normal operation.

C/BW when LOW also resets the Color Subcarrier. If the LOW pulse on C/BW is within the specification for t_{RS} – Color Subcarrier Reset Pulse – the color operation for the 3262B will be unaffected.

DC CHARACTERISTICS: V_{SS} = 5.1 ± .25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS} −1.0		V_{SS} +0.3	V	
V_{IL}	Input LOW Voltage	−5.0		V_{SS} −4.35	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = −0.1 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{IHC}	Clock Input HIGH Voltage	V_{SS} −1.0		V_{SS} +0.3	V	
V_{ILC}	Clock Input LOW Voltage	−5.0 V		V_{SS} −4.35	V	
$V_{SUBCARRIER}$	Subcarrier Output Voltages Approx. Sine Wave	0.5			V (Peak to Peak)	C = 10 pF to V_{DD}* R = 10 kΩ to V_{DD}*
I_{IN}	Input Leakage Current		1.0		μA	V_{IN} = 0 V
I_{DD}	V_{DD} Current		30		mA	
I_{GG}	V_{GG} Current		15		mA	

*Subcarrier Output should be D.C. blocked with .01 μF before loading.

AC CHARACTERISTICS: V_{SS} = 5.1 ± .25 V, V_{GG} = −12 V ± 5%, V_{DD} = 0 V, C_L = 10 pF, 1 TTL Load (1.6 mA), T_A = 0°C to +70°C (See Timing diagrams)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
f	Input Frequency Color	13.3	14.31818	15.4	MHz	See Fig. 2, t_r, $t_f \leq 5$ ns
f_1	Input Frequency Black/White	1.5	2.0475	2.2	MHz	See Fig. 2, t_r, $t_f \leq 20$ ns
t_{PW1}	B/W Clock LOW Time	200	215	230	ns	t_r, $t_f \leq 20$ ns
$t_{\overline{PW1}}$	B/W Clock HIGH Time	200	215		ns	t_r, $t_f \leq 20$ ns
t_{PW2}	Color Clock LOW Time	30	35	40	ns	t_r, $t_f \leq 5$ ns
$t_{\overline{PW2}}$	Color Clock HIGH Time	30	35		ns	t_r, $t_f \leq 5$ ns
t_{OV}	Color Clock Overlap Time			5	ns	
t_{CA}*	Time by which Composite Sync Output preceeds Composite Sync Input		2.0		μs	Black/White
			500		ns	Color
t_S	Synchronization Time for Composite Sync Input			34**	ms	Fig. 1
t_{RS}	Color Subcarrier Reset Pulse	130		200	ns	t_r, $t_f \leq 20$ ns

*t_{CA} is derived digitally from the input clock t_{CA} 4 black and white clock periods (7 color clock periods) + skew between Composite Sync Input and negative clock transition + 250 ns propagation delay.

**One full frame maximum. Synchronizes as a result of the region detected in Composite Sync Input as shown in Figure 3. The minimum time is the width of this region.

RS170EIA TIMING DIAGRAM

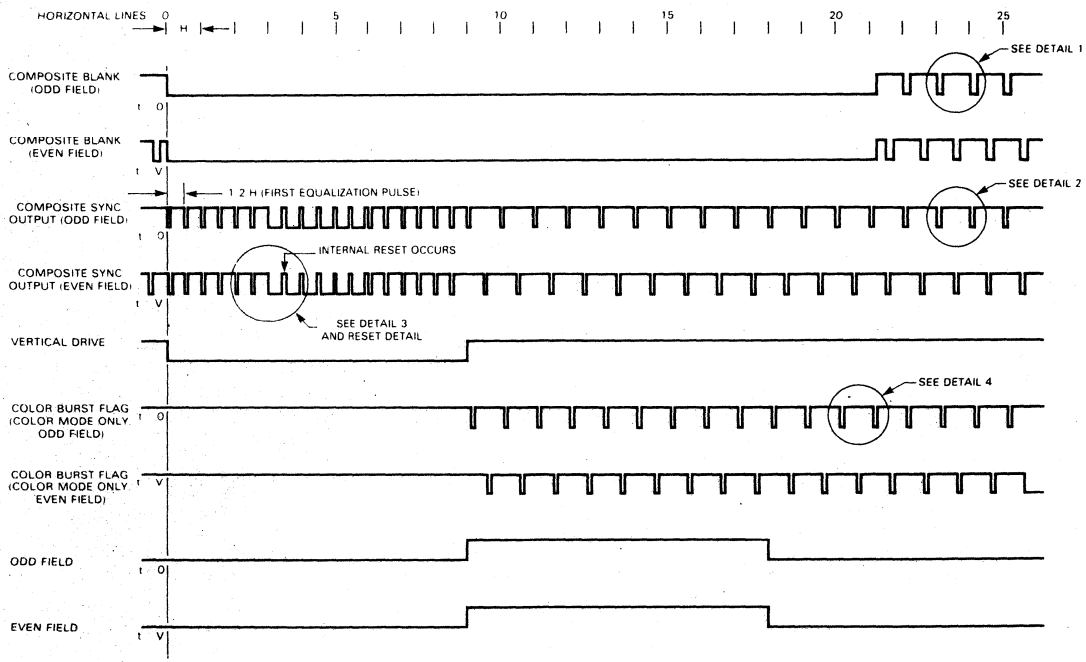
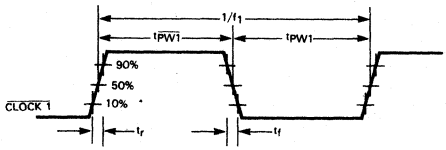
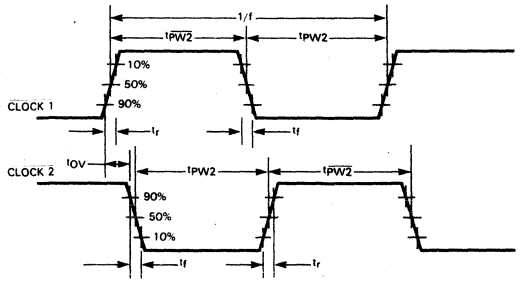


Fig. 1

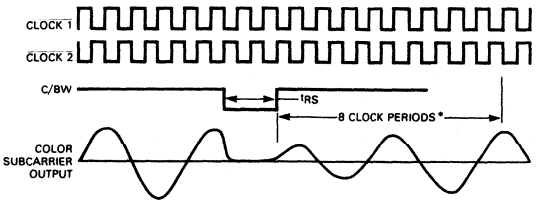
CLOCK TIMING DIAGRAMS



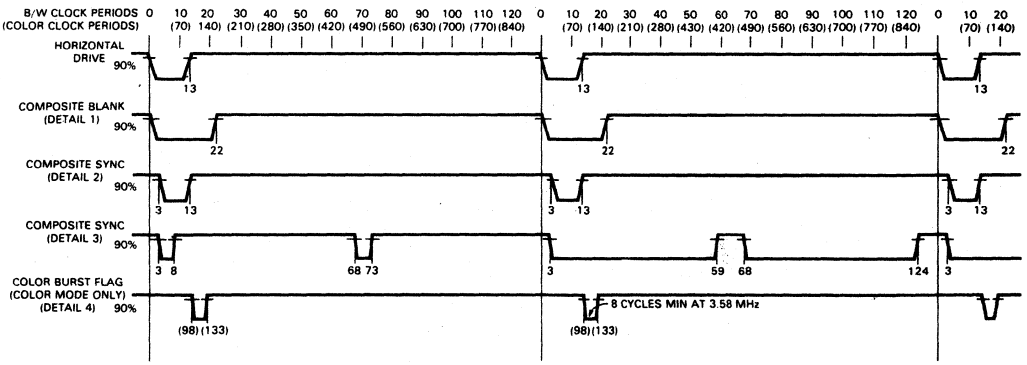
a) Black and White Clock



b) Color Clocks



c) Color Subcarrier Timing and Reset Detail



*Max. subcarrier amplitude attained within 8 color clock periods following rising edge of C/BW.

d) RS170EIA Timing Details

Fig. 2

3262B RESET DETAIL

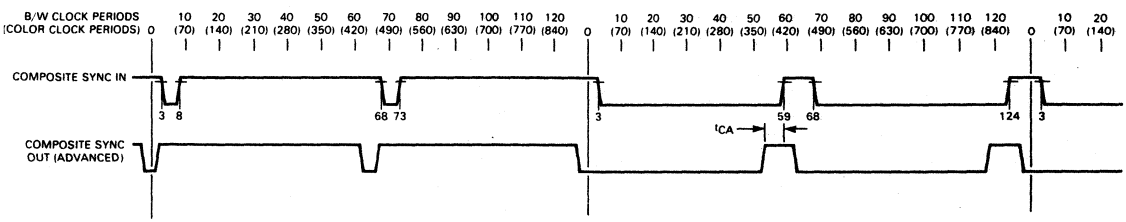
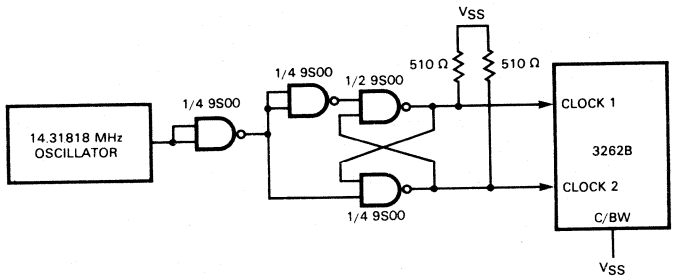
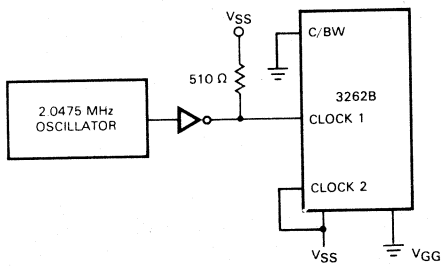


Fig. 3

COLOR CLOCK



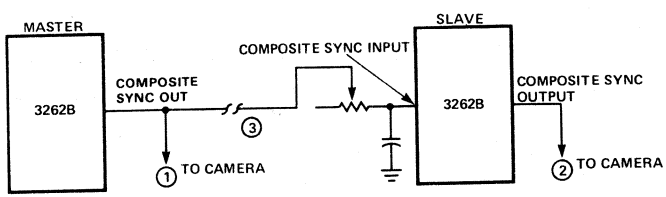
(A) COLOR CLOCK

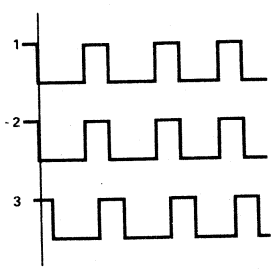


(B) BLACK AND WHITE CLOCK

Fig. 4

GEN-LOCK OPERATION





NOTE: Due to propagation delay associated with distance, Composite Sync at (3) is delayed from (1). Since Composite Sync Out from the Slave camera is advanced by t_{CA} from (3), the RC network can be adjusted so that (1) and (2) are exactly in sync.

Fig. 5

3814

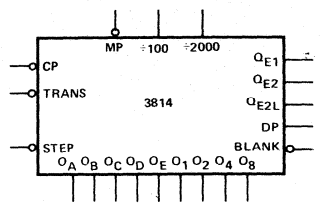
DIGITAL VOLTMETER LOGIC ARRAY

GENERAL DESCRIPTION – The 3814 provides the logic required to implement a four and one-half decade Digital Voltmeter. In addition to four full decade counters and two overflow latches, the device provides a Binary Coded Decimal output (to drive a BCD converter) and five decoded outputs to strobe a multiplexed display.

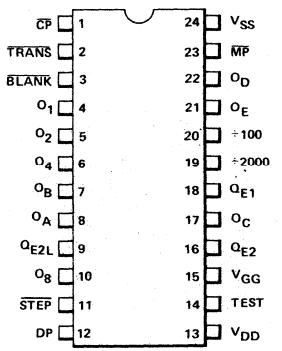
Automatic leading-zero blanking is simply accomplished, and a separate input is provided to blank the entire display. Other outputs provide counter overflow information and auto-ranging control signals. The 3814 is manufactured using silicon gate p-channel enhancement mode technology.

- **DIRECT TTL/DTL COMPATIBILITY – NO EXTERNAL COMPONENTS**
- **DC TO 600 kHz OPERATION**
- **BCD OUTPUT – COMPATIBLE WITH DISPLAY DECODERS**
- **EXTERNAL CONTROL MULTIPLEX FREQUENCY – ACCOMMODATES LED DISPLAYS**
- **UNDERRANGE AND OVERRANGE OUTPUTS**
- **10-COUNT DELAY TO MASK ANALOG SWITCHING NOISE**

LOGIC SYMBOL



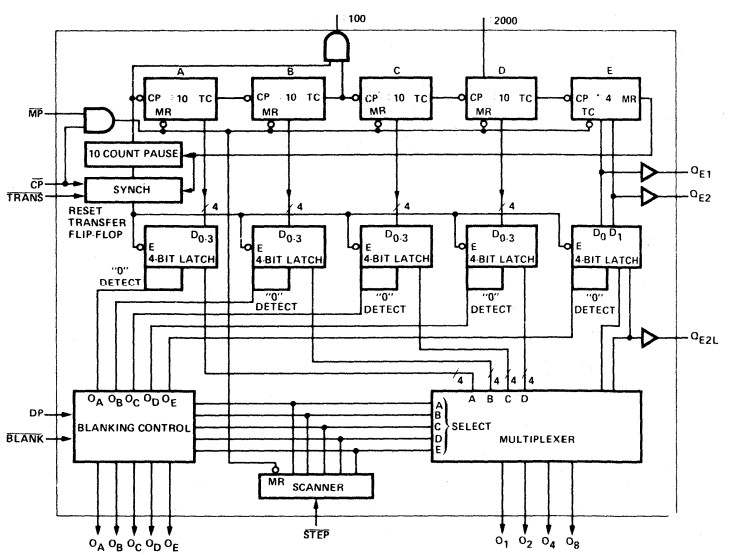
CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

$\overline{CP}$	Clock Pulse Input
$\overline{MP}$	Master Preset
$\overline{TRANS}$	Transfer Count Control
$\overline{BLANK}$	Display Blank Control
O_1, O_2, O_4, O_8	Display Count Outputs
O_A, O_B, O_C, O_D, O_E	Selected Digit Outputs
DP	Decimal Point Control Input
$\overline{STEP}$	Digit Scanner Step Control
Q_{E2L}	Overrange Output
Q_{E2N}	Count Control Outputs
÷100	Count-divided-by-100 Output
÷2000	Underrange Output
TEST	Test Input (Tie to V_{SS})

BLOCK DIAGRAM



3814

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- **EXTERNAL CONTROL MULTIPLEX FREQUENCY – ACCOMMODATES LED DISPLAYS**
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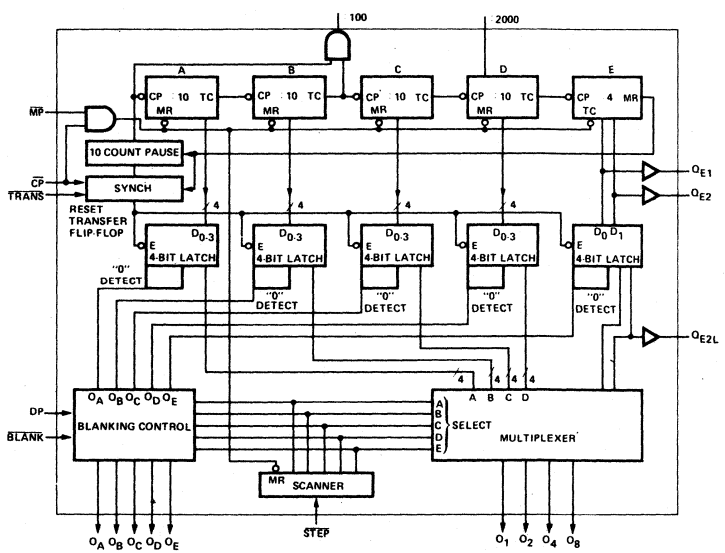
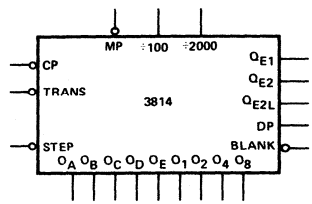
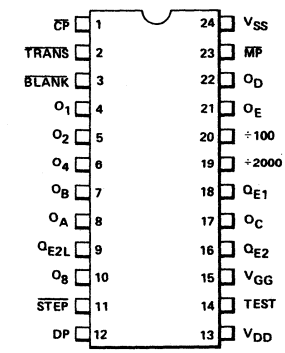
BLOCK DIAGRAM



LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



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$\overline{STEP}$	Digit Scanner Step Control
O_{E2L}	Overrange Output
O_{E2N}	Count Control Outputs
÷100	Count-divided-by-100 Output
÷2000	Underrange Output
TEST	Test Input (Tie to V_{SS})

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to 70°C
V_{GG}	+0.3 to −24 V
All Other Inputs	+0.3 to −16 V
Outputs	+0.3 to −8 V (I_L <10 mA)

FUNCTIONAL DESCRIPTION — The 3814 is intended for use as the digital logic portion of digital voltmeter systems. An input clock ($\overline{CP}$) drives 4-1/2 decades of BCD counters, with the counters changing state on the LOW to HIGH clock transition. The output of the second decade is gated with the input clock ($\overline{CP}$) and brought off chip (÷100) for use as an additional clock. This clock may be used to drive the multiplexer input ($\overline{Step}$).

A clock input synchronized with a LOW state on Master Preset ($\overline{MP}$) will set the counters to 30,000. The 3814 will then count the next 10,000 clock pulses, and be in the 00,000 state. At this count the device will ignore the next 10 clock inputs. This feature is useful when the device is used in systems where the current switching associated with analog to digital conversion generates transients which might cause false triggering. This 10 count correction requires a small current (equal to the integral of 10 counts of the standard current) be added to the unknown current. Thus, even if the current to be measured is zero, the integrator output voltage is moved off zero, eliminating comparator transient triggering. Following this 10 count pause, the 3814 continues to count; in normal operation the A/D circuitry will provide a transfer input, causing the count to be loaded into the latches. The count stored (and present at the output multiplexer) will be proportional to the ratio of the unknown current to the standard current. The counter will continue to accept clock pulses, and at 20,000 the Q_{E1} output will go LOW and the Q_{E2} output will go HIGH. This state may be decoded and used to reset the analog circuitry. Since current switching associated with this reset may again cause false triggering, only one transfer command is accepted during the interval from 00,000 to 39,000.

In typical operation, the states of the two overflow flip-flops (Q_{E1} and Q_{E2}) may be used to control system operation.

Table 1.

COUNT	Q_{E1}	Q_{E2}
30,000 to 00,000	1	1
00,000 to 10,000	0	0
10,000 to 20,000	1	0
20,000 to 30,000	0	1

COUNT CONTROL OUTPUTS

Table 2.

DIGIT FED BACK TO DP	EXAMPLE COUNT	DISPLAY*
A, or DP = V_{SS}	00000	0
A, or DP = V_{SS}	00120	120
B	00120	12.0
C	00120	1.20
D	00120	0.120
E, or DP = V_{DD}	00120	0.0120
		E DCBA

*The decimal point itself in the display is not controlled by the 3814.

LEADING-ZERO BLANKING

In addition, the Q_{E2} output is latched and brought out as Q_{E2L}. If a system utilizing a full scale count of 19,999 is implemented with the 3814, the HIGH state of Q_{E2L} will indicate an overrange condition. The divide by 2,000 output (÷2,000) is intended for use as an underrange indicator. If this output has not gone HIGH when a transfer command is received, the total count is less than 10% of full scale.

A power-on reset should be provided externally to insure proper counter initialization.

DATA OUTPUTS — The state of one of the 4-1/2 decade counters is presented as a BCD multiplexed output (O_1, O_2, O_4, O_8). One of the five decoded outputs (O_A, O_B, O_C, O_D, O_E) will be HIGH, indicating which decade's count is present at the BCD outputs. The multiplexer is clocked by a separate input ($\overline{Step}$) which may be driven at 1/100 of the clock frequency by directly connecting the ÷100 output to the $\overline{Step}$ input.

BLANKING — Automatic leading zero blanking is simply accomplished by directly wiring two pins of the 3814. One of the decade outputs (O_A through O_E) when wired to the decimal point (DP) input will cause all leading zeros to the left of the feedback decade to be automatically blanked. For example if the count is 00120 and decade "A" (O_A) is connected to DP, the display will be "120". With the same count, and decade "D" (O_D) connected to DP, the display will be 0120. When the $\overline{Blank}$ input is LOW all outputs (O_A thru O_E) go LOW (see Table 2).

TEST INPUT — This pin is used during the testing of the 3814 and must be wired to V_{SS} for operation.

DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS}−1.0		V_{SS}+0.3	V	All Inputs Including $\overline{CP}$
V_{IL1}	Input LOW Voltage	−2		0.5	V	$\overline{CP}$ and $\overline{STEP}$
V_{IL2}	Input LOW Voltage	−2		+0.8	V	All Inputs Except $\overline{CP}$ and $\overline{STEP}$
V_{OH1}	Output HIGH Voltage	2.4		V_{SS}	V	a) Sourcing 200 μA for Outputs; Q_{E1}, Q_{E2}, Q_{E2L}, ÷2000, C_L <20 pF. b) Sourcing 400 μA for Outputs; O_1, O_2, O_4, O_8; C_L <30 pF.
V_{OH2}	Output HIGH Voltage	V_{SS}−1.0		V_{SS}	V	Sourcing 200 μA for Outputs O_A, O_B, O_C, O_D, O_E, ÷100; C_L <20 pF
V_{OL}	Output LOW Voltage			0.4	V	a) Sink 1.6 mA on Outputs Q_{E1}, Q_{E2}, Q_{E2L}, O_A, O_B, O_C, O_D, O_E, ÷ 100, ÷ 2000; C_L <20 pF. b) Sink 2.0 mA on Outputs O_1, O_2, O_4, O_8, C_L <30 pF.
R_{IN1}	Input Resistor Returned to V_{SS}	1	2.5	5	kΩ	Inputs: $\overline{CP}$, $\overline{Blank}$, $\overline{MP}$, $\overline{Trans}$.
R_{IN2}	Input Resistor Returned to V_{SS}	10	25	50	kΩ	Inputs: $\overline{Step}$, DP
I_{GG}	V_{GG} Supply Current	3	5	15	mA	
I_{SS}	V_{SS} Supply Current	20	30	50	mA	

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to 70 C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
f	Operating Frequency	DC		600	kHz	Fig. 1
t_{PWC}	Clock Pulse Width	300	220		ns	Fig. 1
t_{TS}	$\overline{TRANS}$ Set Up Time	250			ns	Fig. 2
t_{TH}	$\overline{TRANS}$ Hold Time	50			ns	Fig. 2
t_{DHL}	HIGH to LOW Transition for Outputs					
	÷100		320	1000	ns	Fig. 3
	÷2000		375	1000	ns	Fig. 3
	Q_{E1}, Q_{E2}		400	800	ns	Fig. 3
	O_1, O_2, O_4, O_8		450	1000	ns	Fig. 4
t_{DLH}	LOW to HIGH Transition for Outputs					
	÷100		350	1000	ns	Fig. 3
	÷2000		450	1000	ns	Fig. 3
	Q_{E1}, Q_{E2}		425	800	ns	Fig. 3
	O_1, O_2, O_4, O_8		550	1000	ns	Fig. 4
t_r, t_f	Clock Rise and Fall Times			200	ns	Fig. 1
t_{MPS}	Master Preset Set-up Time	300			ns	Fig. 1
t_{MPH}	Master Preset Hold Time	200			ns	Fig. 1

TIMING DIAGRAMS

INPUT CLOCK ($\overline{STEP}$ OR $\overline{CP}$) WAVEFORM

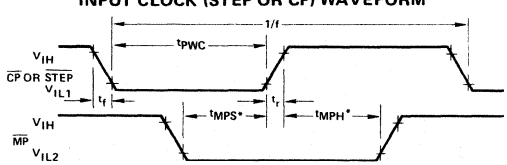


Fig. 1. *APPLIES ONLY TO $\overline{CP}$ INPUT

TRANSFER SETUP AND HOLD TIMES

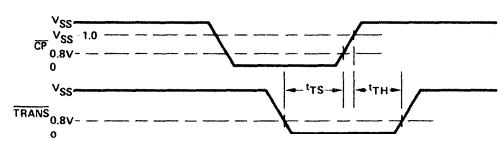


Fig. 2.

PROPAGATION DELAY-OUTPUTS

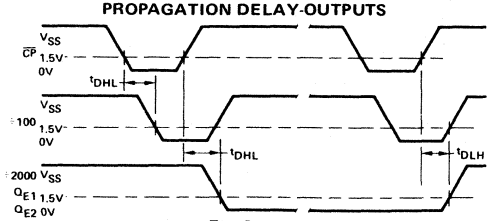


Fig. 3.

PROPAGATION DELAY – BCD OUTPUTS

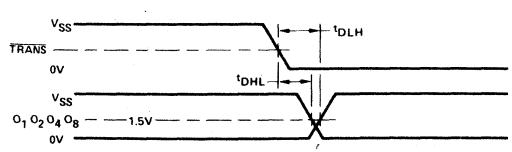
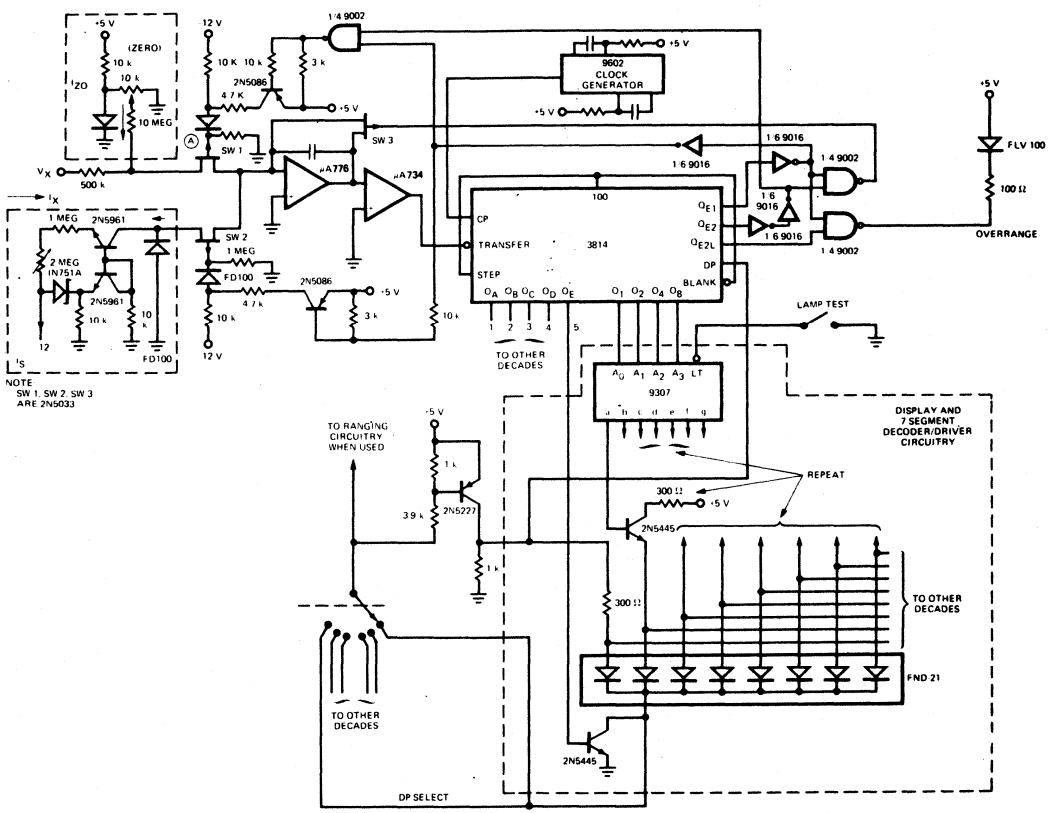


Fig. 4.

LOW COST DVM – Figure 5 shows one version of a basic DVM. An input buffer, such as μA776, could have been added to boost the input resistance to 400 MΩ and provide isolation of the unknown from the action of the current sources. If source resistance is low, the buffer may not be needed. The I_{ZO} and I_S current sources have been implemented with discrete components. Also, temperature compensation has been added to the I_S circuit as this is most critical to system accuracy. As designed, only positive inputs are properly integrated. If negative input capability is also desired, additional current sources and gating are needed.

Ideally, SW_1 and SW_2 have zero resistance when on, infinite resistance when off and no offset voltage. For an accurate system then, bipolar transistors cannot be used because of offset. P-Channel or N-Channel FETs ably satisfy all three of the switch criteria. To avoid gate-to-source debiasing, P-Channel devices should be used for negative input voltages and N-Channel devices for positive inputs. The versatile μA776 is used again as the integrator amplifier; the μA734 comparator receives the integrator signal and upon a null crossing, generates the transfer command to the 3814. All gating for mode control to SW_1, SW_2 and SW_3 is obtained from the Q_{E1} and Q_{E2} output. The FND21 LED Display Module and the associated decoder and drivers are also shown. For flexibility of decimal point location and zero suppression, a five position SPST switch has been added to appropriately gate the DIGIT SELECT outputs to the DP inputs.

This DVM (exclusive of display circuitry) can be built with a total of *only six integrated circuits – seven* if input buffering is required.



3817A/3817D

DIGITAL CLOCK RADIO OR DIGITAL ALARM CLOCK

GENERAL DESCRIPTION – The 3817A and 3817D are 4 digit Alarm Clocks utilizing the MOS P-channel Isoplanar, silicon gate process. The 3817A and 3817D contain all the logic required to build a variety of clocks and timers using 50 or 60 Hz line frequencies. Interfacing to LED, LCD, Gas Discharge and Vacuum Fluroescent displays is possible with a minimum number of external components.

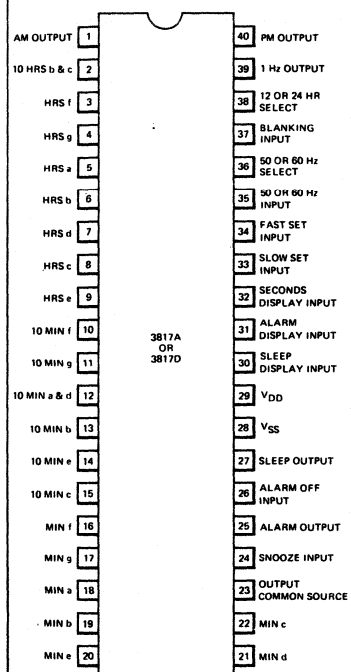
Four different display modes may be selected:

- Time (unselected) - Hours and minutes
- Seconds – Minutes and seconds
- Alarm – Display the present setting of the alarm
- Sleep (countdown) – Displays time (minutes) to turn-off of radio

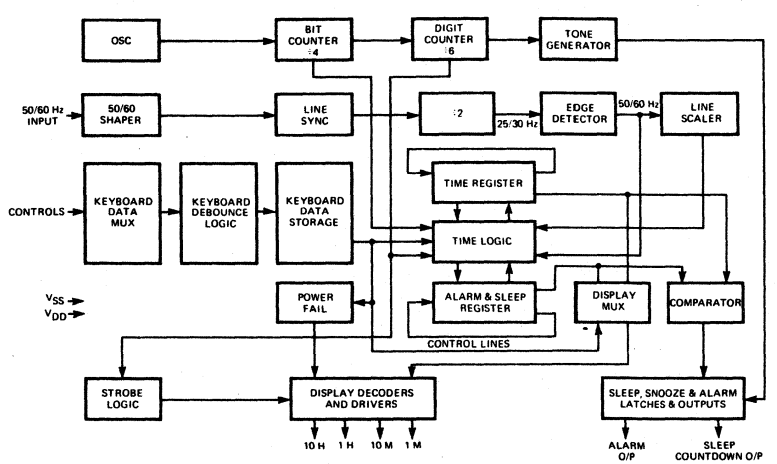
A display format of either 12 or 24 hours may be externally selected. These devices operate from a single unregulated power supply over a range of 8 to 22 volts with an indication to inform the viewer that a power failure has occurred. They are available in the 40-pin ceramic or plastic Dual In-line Package.

- **50 OR 60 Hz OPERATION**
- **SINGLE POWER SUPPLY**
- **12 OR 24 HOUR DISPLAY FORMAT**
- **AM/PM OUTPUTS (12-HOUR DISPLAY FORMAT)**
- **LEADING ZERO BLANKING (12-HOUR DISPLAY FORMAT)**
- **FAST AND SLOW SET CONTROLS**
- **POWER FAILURE INDICATION**
- **BLANKING/BRIGHTNESS CONTROL CAPABILITY**
- **DIRECT INTERFACE TO LED, FLUORESCENT TUBES, OR LCD DISPLAYS**
- **9 MINUTE SNOOZE ALARM**
- **PRESETTABLE 59 MINUTE SLEEP TIME**

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



APPLICATIONS

- Alarm Clocks
- Desk Clocks
- Clock Radios
- Automobile Clocks
- Stop Watches
- Industrial Clocks
- Military Clocks
- Photography Timers
- Industrial Timers
- Sequential Controllers

ABSOLUTE MAXIMUM RATINGS (All voltages relative to V_{SS})

Supply Voltage Range, V_{DD}	−22 V to +0.3 V
Input Voltage Range	−22 V to +0.3 V
Output Voltage Range	−22 V to +0.3 V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

TABLE 1: OPERATING MODES FOR 3817A AND 3817D

DISPLAY MODE	DISPLAY CONTROL (PIN) CONNECTED TO V_{SS}	SET CONTROL CONNECTED TO V_{SS}			
		NONE	FAST SET (34)	SLOW SET (33)	BOTH
Time-of-Day	None	Time-of-Day Display	Time Set Advance (60 Hz)	Time Set Advance (1 Hz)	Same as FAST SET
Seconds	Seconds (32)	Seconds Display (1M, 10S, 1S)*	Seconds Reset to 00 (No Carry to Minutes)	Time Count Inhibited (Hold Mode)	Time Reset 12:00:00AM (12 hr) 00:00:00 (24 hr)
Alarm Time	Alarm Time (31)	Alarm Time Display (10H, 1H, 10M, 1M)	Alarm Set Advance (60 Hz)	Alarm Set Advance (1 Hz)	Alarm Reset 12:00AM (12 hr) 00:00 (24 hr)
Sleep Countdown	Sleep Countdown (30)	Sleep Countdown Display (10M, 1M)**	Sleep Countdown Set (Countback from 00 at 1 Hz)	Sleep Countdown Set (Countback from 00 at 1 Hz)	Same as FAST SET

*Leading digit is blanked.
**Leading two digits are blanked.

FUNCTIONAL DESCRIPTION

50/60 Hz Input (Pin 35) and Select (Pin 36) – The timing for the Clock is obtained from the 50 Hz or 60 Hz ac line. Internal circuitry allows interfacing with the ac line through a high-value resistor. Internal limiting is provided, and hysteresis is designed in to minimize noise response. A series resistor is always necessary to limit the current at this input.

The input frequency may be 50 or 60 Hz. To select a frequency of 50 Hz connect pin 36 to V_{SS}; to select a 60 Hz frequency leave pin 36 disconnected. An internal pull-down resistor provides the logic level.

Display Modes/Time Settings (Pins 30 to 32) – There are four display modes:

1) Time-of-day – This is the normal mode of operation where tens and unit hours (10 H, 1 H) and tens and unit minutes (10 M, 1 M) are displayed. It is obtained by leaving all Display Controls unconnected. To set any desired time, the Fast Set and/or Slow Set inputs must be connected to V_{SS}. Fast Set advances the time at a 60 Hz rate; Slow Set advances the time at a 1 Hz rate (see Table 1).

2) Seconds Display Input (Pin 32) – If a more accurate time display is desired, the Seconds Display mode may be activated by connecting the Seconds Display input to V_{SS}. The Output will display unit minutes (1 M) and tens and unit seconds (10 S, 1 S). If, during a Seconds Display, Fast Set is connected to V_{SS}, seconds will reset to 00 with no effect on the minutes display. If Slow Set is connected to V_{SS}, the entire counter will stop (Hold mode) until Slow Set is disconnected. Activating both Fast Set and Slow Set simultaneously will reset the time-of-day to 12:00 AM (12-hour format). (See Table 1)

3) Alarm Display Input (Pin 31) – The contents of the alarm register may be displayed by connecting pin 31 to V_{SS} causing 10 H, 1 H, 10 M, 1 M to be displayed. The Alarm is set in the same manner as "time-of-day". Activating both Fast Set and Slow Set simultaneously will reset the Alarm Time to 12:00 AM (12-hour format) or 00:00 (24-hour format). (See Table 1)

FUNCTIONAL DESCRIPTION (Cont'd)

4) Sleep Display Input (Pin 30) – The Sleep Countdown is generally used to turn off a radio after falling asleep. It displays in minutes (10 M, 1 M) and counts down the time remaining from a maximum of 59 minutes until any external circuitry is turned off. The Sleep Time is set by using the Fast Set and/or Slow Set inputs which decrement the counter from 00 (00, 59, 58, etc.) to the desired Countdown time. Once set, the counter will count down to 00. For times other than 00, the Sleep Countdown output (open-drain device) is pulled toward V_{SS}. A 00 display will cause a high impedance at the Sleep Countdown output. The countdown may be terminated at any time by momentarily connecting the Snooze input to V_{SS}.

Time Setting Inputs – Fast (Pin 34) and Slow (Pin 33) – Two inputs are provided to set time, where the Fast Set is 50 or 60 Hz and the Slow Set is 1 Hz. Their function varies for each of the four display modes: Time, Seconds, Alarm and Sleep Countdown (see Table 1).

Alarm Output (Pin 25), Snooze (Alarm) Input (Pin 24) and Alarm Off (Pin 26) – The Alarm has the option to output either a dc level (3817D) or a 700 Hz frequency (3817A) for a variety of industrial or commercial applications. The level or tone output will be active for 60 minutes after the Alarm setting.

Connecting the Snooze input to V_{SS} during the 60-minute period while the alarm is active will inhibit the Alarm Output for about 9 minutes. The Alarm is turned off by momentarily connecting Pin 26 to V_{SS}. The alarm is inhibited as long as Pin 26 is left at V_{SS}.

A Power Failure is caused when the V_{SS}-to-V_{DD} voltage difference drops below 8 volts and is indicated by a 1 Hz flashing of the AM or PM segments in the 12-hour mode and the C/F, C, or G segments in the 24-hour mode. The failure indicator is reset by connecting either the Fast or Slow Set Inputs to V_{SS} (Pins 33 or 34).

Blanking Input (Pin 37) – The displays will be enabled or be blanked by connecting Pin 37 to V_{SS} (HIGH) or V_{DD} (LOW), respectively. This is the only control pin where the input must be connected to a voltage.

Common Source Connection (Pin 23) – All segments including AM and PM are open drain devices with all sources connected in common to Pin 23. Connecting all sources in common permits these devices to be used with a multitude of display devices, even those which have different power supply requirements.

Segment Outputs (Pins 1, 3 to 11, 13 to 22, and 40) – Each of these segment outputs may source a maximum of *8 milliamps* of direct current. The maximum power is *25 milliwatts* per output device (see Figure 1), at an ambient temperature of 50°C.

Segment Outputs (Pins 2 and 12) – Each of these segment outputs may source a maximum of *16 milliamps* of direct current or a maximum power of *50 milliwatts* per output device at an ambient temperature of 50°C.

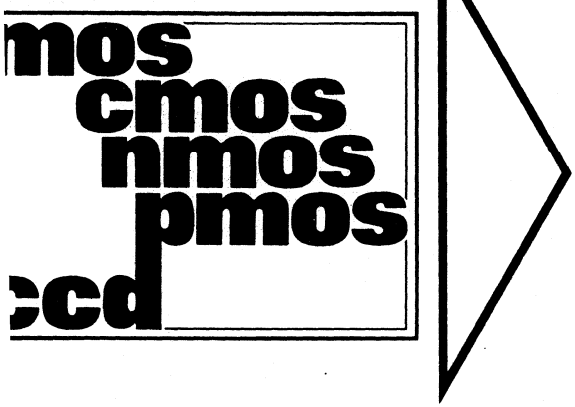
DC REQUIREMENTS: $T_A = 0°C$ to $+70°C$, $V_{SS} = +15\ V \pm 7\ V$, $V_{DD} = 0\ V$

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{FIH}	50/60 Hz Input HIGH Voltage	$V_{SS}-1$		V	External Series Resistor to limit current to $-10\ \mu A \leq I_{FIL} \leq -350\ \mu A$ and $10\ \mu A \leq I_{FIH} \leq 150\ \mu A$
V_{FIL}	50/60 Hz Input LOW Voltage		$V_{SS}-6$	V	
V_{IH}	Control Input HIGH Voltage	$V_{SS}-1$	V_{SS}	V	Internal R, typically 2.5 MΩ to V_{DD}
V_{IL}	Control Input LOW Voltage	V_{DD}	$V_{DD}+2$	V	
V_{BIH}	Blanking Input HIGH Voltage	$V_{SS}-2$	V_{SS}	V	
V_{BIL}	Blanking Input LOW Voltage		$V_{SS}-4$	V	

DC CHARACTERISTICS: $T_A = 0°C$ to $+70°C$, $V_{SS} = +15\ V \pm 7\ V$, $V_{DD} = 0\ V$

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{PF}	Power Failure Detect Voltage	8		V	
I_{IN}	Input Leakage Current		1	μA	$V_{IN} = -20\ V$, Pin 37 only
I_{DD}	Power Supply Current		6	mA	No output loading
I_{OH}	Output HIGH Current	1.5		mA	$V_{OH} = V_{SS}-2$
I_{OL}	Output LOW Current		1.0	μA	$V_{COMMON} = V_{SS}$ $V_{OL} = V_{DD}$ See Fig. 1
*I_{OH2}	Output HIGH Current	3.0		mA	
*I_{OL2}	Output LOW Current		1.0	μA	
I_{IOH}	1 Hz Output HIGH Current	4.5		mA	

*Pins 2 and 12



THINK F8 UNIVERSAL STANDARD MICROPROCESSOR

VERSATILE . . EFFICIENT . . COST EFFECTIVE

The ultimate goal, from F8 design concept through development and production, was to produce the most versatile, efficient, cost-effective microprocessor system available today. To accomplish this, five stringent parameters, based on user experience with other systems, were set forth as guidelines for the F8.

- Minimum Parts Count
- Cost Effectiveness
- Simple Peripheral Interfaces
- Easy Expansion through Modular Architecture
- Simplified Programming and Debugging

HOW WERE F8 GOALS MET ?

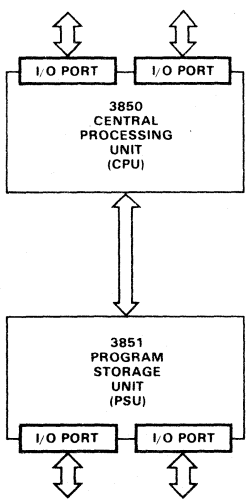
By . . . *unique system partitioning* the system functions, have been divided among the various circuits of the F8 family to provide sophisticated modularity. As a result, it is now possible to build a minimum microprocessor system with only two devices. To this system PSU, RAM and I/O devices can be added to form medium size or memory intensive systems with a minimum use of external parts. And, finally, for solving complex problems, the F8 devices can be connected as subsystems into a synergistic system of independent microprocessors.

By . . . *incorporating the I/O structure on the chips* so that the majority (95%) of the peripheral devices can be directly controlled without the need for special circuits. The trick is to accommodate the characteristics of a given peripheral device in the software. The I/O hardware structure includes a programmable timer, an efficient interrupt system and bidirectional I/O ports.

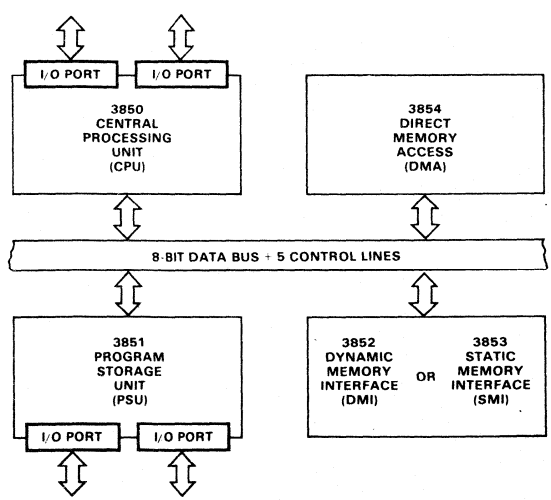
By . . . providing *carefully thought out software* for generating and debugging microprograms and a choice of three hardware modules for speeding up prototype development.

WHAT IS THE RESULT ?

. . . *a complete family of LSI circuits* that can be used as building blocks to construct versatile, efficient, cost effective systems from the most simple to the highly complex.

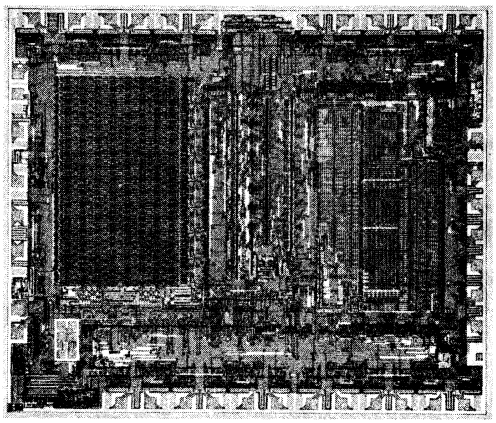


MINIMUM SYSTEM

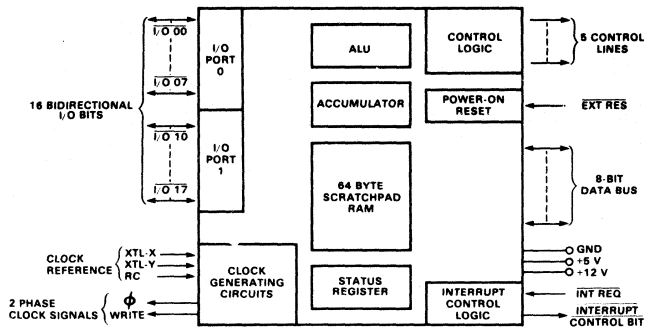


F8 DEVICE FAMILY

3850 CENTRAL PROCESSING UNIT

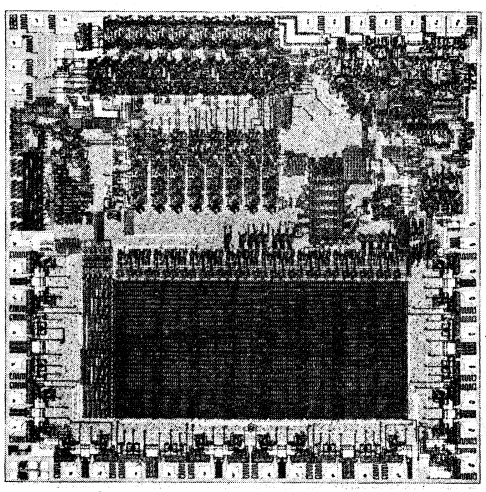


Fairchild's F8 Central Processing Unit (CPU) contains all of the functions of an ordinary central processor and adds some time and money saving features uniquely its own. For instance, the 64 bytes of scratchpad RAM memory already included on the F8 CPU eliminate the need for external RAM circuits in many applications. Clock and power-on-reset circuitry, normally requiring additional integrated circuit packages, are included on-chip. Fairchild's CPU also contains 16 bits of fully bidirectional input and output lines internally latched (for storing output data) and capable of driving a standard TTL load.



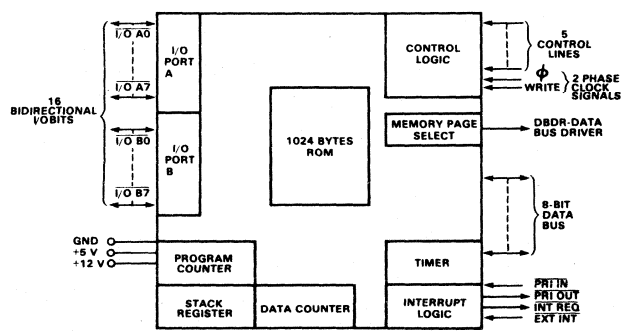
3850
CPU BLOCK DIAGRAM

3851 PROGRAM STORAGE UNIT

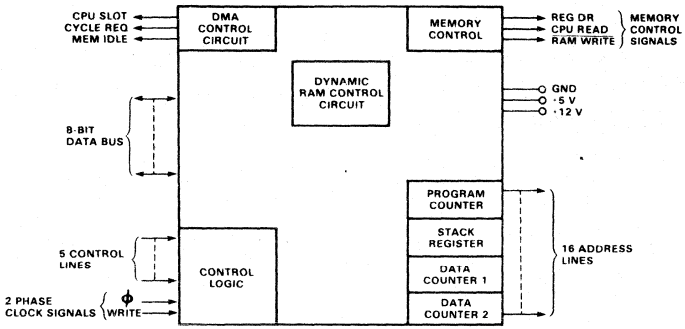


It is important to note that Fairchild's Program Storage Unit (PSU) is not just a conventional Read Only Memory. In addition to containing 1024 bytes of mask programmable ROM for program and constant storage, the F8 PSU includes the addressing logic for memory referencing, a Program Counter, an Indirect Address Register (the Data Counter) and a Stack Register. A complete vectored interrupt level, including an external interrupt line to alert the central processor, is provided. All of the logic necessary to request, acknowledge and reset the interrupt is on the F8 PSU. The 8-bit Programmable Timer is especially useful for generating real time delays. The PSU has an additional 16 bits of TTL compatible, bidirectional, fully latched I/O lines.

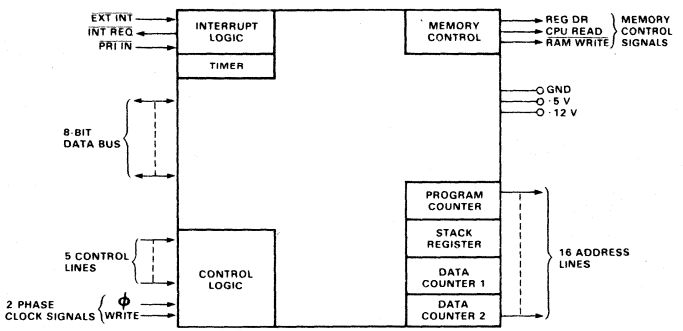
Systems requiring more program storage may be expanded by adding more PSU circuits. For example, one F8 CPU and three F8 PSUs will produce a microprocessor system complete with 64 bytes of RAM, 3072 bytes of ROM, 64 I/O bits, three interrupt levels, and three programmable timers. This complete system will require only four IC packages.



3851
PSU BLOCK DIAGRAM



3852
DMI BLOCK DIAGRAM

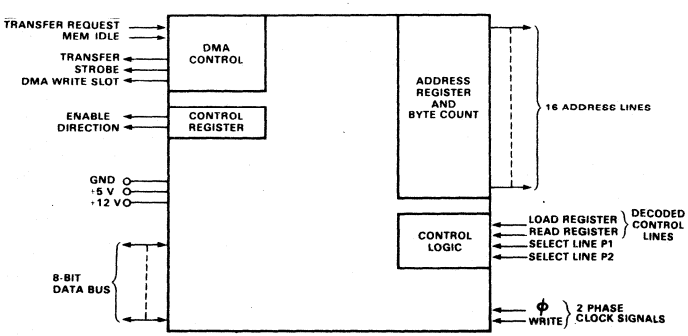


3853
SMI BLOCK DIAGRAM

3852/3853 MEMORY INTERFACE

For applications requiring more than the 64 byte RAM located on the CPU, two memory interface circuits are included in the F8 set. Each device generates the 16 address lines and the signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory. Either device may be used in conjunction with standard static semiconductor memory devices.

The Static Memory Interface (SMI) contains a full level of interrupt capability and a programmable timer. The Dynamic Memory Interface (DMI) contains all of the logic necessary to refresh MOS dynamic memories without degrading the system throughput time. The F8 DMI can also interface with static memories when desired.



3854
DMA BLOCK DIAGRAM

3854 DIRECT MEMORY ACCESS

Fairchild's Direct Memory Access (DMA) device sets up a high speed data path to link F8 memory with peripheral electronics. The F8 DMA circuit, when working in conjunction with the F8 DMI, does not require overhead electronics to keep track of memory addresses, bytes transferred and handshaking signals. The data transfer is initiated by the CPU under program control. Once started, the DMA transfer will continue without CPU intervention. The CPU can sense the enable line of the DMA to determine the completion of a transfer. The entire DMA transfer will take place without halting the central processor.

F8 MICROPROCESSOR APPLICATION SPECTRUM

Because of its unique system partitioning, the F8 device set can be applied across a wide range of applications. The minimum two-circuit system is the basis for a modular architecture that can handle increasingly complex problems. A system of medium complexity can be designed by adding more F8 PSUs. The use of an F8 memory interface device allows up to 65K bytes of standard memories to be incorporated into the F8 system. For highly complex applications, independent F8 subsystems can be connected into a multiprocessing system in which each subsystem can operate independently yet can be controlled by one CPU that is the coordinator.

CUSTOM

COST SENSITIVE

PERFORMANCE SENSITIVE

MINICOMPUTER OR BIT-SLICE STRUCTURE

- AUTOMOTIVE IGNITION CONTROL
- AUTOMOTIVE BRAKES
- AUTOMOTIVE DASH CONTROL
- HOME APPLIANCES
- VENDING MACHINES
- ELECTRONIC SCALES
- SPECIALTY CALCULATORS
- ELECTRONIC GAMES
- AUTOMATED GAS PUMPS
- FAST FOOD CASH REGISTERS
- PAPER TAPE HANDLERS
- CASSETTE TAPE HANDLERS
- CASH REGISTERS
- COMMUNICATION LINE CONTROLLERS
- PRINTER CONTROLLERS
- TRAFFIC LIGHT CONTROLLERS
- COPIERS
- PABX
- FILM PROCESSING
- AUTOMOTIVE ANALYZERS
- FLOPPY DISK CONTROLLERS
- MESSAGE CONCENTRATORS
- MEDICAL INSTRUMENTS
- MACHINE TOOL CONTROL
- STORAGE AND FORWARD MESSAGE SWITCHING
- ADAPTIVE EQUALIZERS
- FAST FOURIER TRANSFORM ANALYZERS

F8

A TWO-CIRCUIT SYSTEM

The two-circuit F8 microprocessor is suitable for small data terminals, controllers, and specialty calculators. The keyboard is connected directly to the F8 I/O ports without special interfaces. Switch-bounce protection, rollover, and key encoding are all under software control. Software also decodes signals for LED readouts.

As an appliance controller, for example, the two-circuit system can perform all input-output sensing, actuating, timing, and computation operations. A system like the combination washing-machine-and-dryer controller in *Figure 1* requires more than 250 components when other microprocessor device sets are used, but with the F8 devices uses only 55 components, including 28 LEDs and the power semiconductor devices and relays used to control the motors. A set of custom circuits would also require about 50 parts, but initial engineering expense is heavy and severe penalties are incurred if changes are required. With the F8 system changes can be made by merely changing the program.

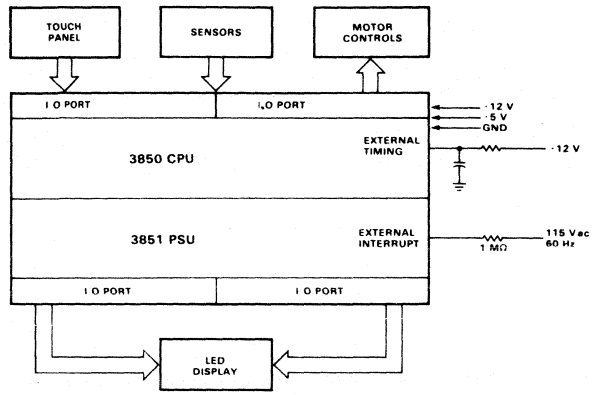


Fig. 1. Two-Circuit System

A MORE COMPLEX SYSTEM

The versatility of the F8 system is indicated by the traffic-light-controls system in *Figure 2*. The use of one CPU and two PSU circuits provides the designer with two timers, two interrupts, an onboard clock, onboard power-on reset, onboard switch decoding, and 48 bidirectional I/O bits. This system could be tied to vehicle detectors in the road, to monitor traffic for left-turn lanes as well as through-traffic flow in four directions. It would also react to interrupts from the pedestrian control buttons at each corner. There also is sufficient I/O capability to permit communication with and control of neighboring intersections and to allow the system to be operated manually or tested for proper operation.

Five F8 features are of particular interest for this type of application. One of the interrupts can eliminate the need for such external circuits as a comparator to compare a count of the cars with a predetermined value to cause the light to change. (The CPU can handle the simple arithmetic of counting cars.) This interrupt also eliminates the need for continuous polling of traffic count by the microcomputer. The second interrupt would be ideal for permitting pedestrian control to override the automatic system. The internal clock, with an external crystal, can also control light routines.

The two timers permit simultaneous counting of delay for vehicle signals and flashing warning lights for pedestrians. The onboard power-on reset acts in case of power failure to start the system automatically when power is renewed. The bidirectional I/Os have built-in latches that eliminate the need for external latches for the job of "holding" commands for lights as well as the momentary commands provided by timers and sensors.

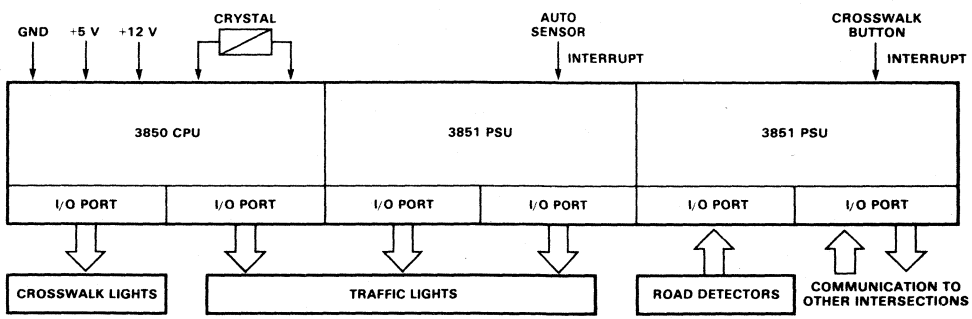


Fig. 2. Medium Complexity System

A MEMORY INTENSIVE SYSTEM

A typical application is a printing credit-verification terminal *(Figure 3)*. Such a system requires high performance and yet must be low in cost if it is to reach a large market. Only four different F8 devices are required to handle a keyboard input, visual display, card reader, and printer as well as provide a modem interface and memory interface for external RAM storage. This printing credit-verification system might be compared to a "bare mini-computer" in terms of utility; however, a detailed engineering evaluation would show that it costs less, has fewer parts and a more flexible I/O structure.

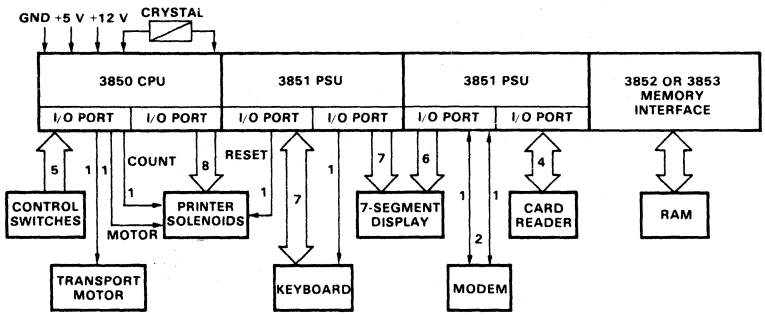


Fig. 3. Memory Intensive System

MULTI-MICROPROCESSOR SYSTEM

Figure 4 shows a specific application of the multi-processing concept as applied to a keyboard-to-floppy-disk system. Possibly this is the most cost-effective way of implementing this system, conservatively costing less than 50% of a conventional implementation. This system involves concurrent operation of three floppy disks, magnetic tape, CRT, keyboard, printer, and modem. While the low-speed devices (the keyboard, printer, and modem) can be adequately handled by the programmed I/O structure, the high-speed devices (disks, magnetic tape, and CRT) require separate F8 CPUs and PSUs.

This scheme provides simplicity of control, modularity, and freedom to expand. In this case, the units operating concurrently are: one magnetic-tape unit (25 μs/byte); three floppy-disk units (32 μs/byte each); and a CRT unit (71 μs/byte). This combination requires an aggregate bandwidth of 0.1478 byte/μs. This is well within the F8's upper bandwidth limit of 0.5 byte/μs.

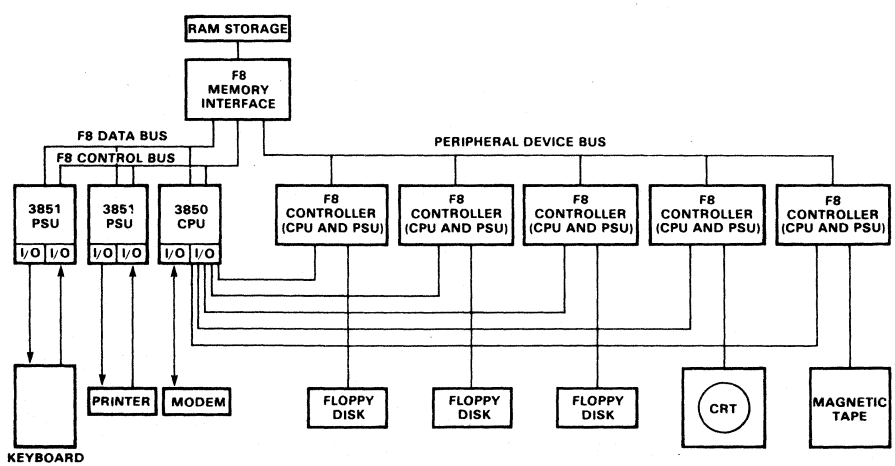


Fig. 4. Multi Microprocessor System

F8 MICROPROCESSOR DEVELOPMENT SUPPORT HARDWARE

Development support hardware is an integral part of Fairchild's F8 Microprocessor product concept. Fairchild's Microprocessor Support Engineering Group has developed an extensive set of design aids to enable customers to shorten their development cycle time and speed up programming. The F8 development support hardware provides a working model of the user's system and facilitates:

- Evaluation of F8 Microprocessor hardware operation
- Reduction of engineering time and development costs
- Preparation of system software and firmware programs
- Reduction of system hardware, software and firmware evaluation and debug time

F8 MICROPROCESSOR EVALUATION KIT

The lowest cost method for quick evaluation of the operation of the F8 Microprocessor hardware. Comes complete with a preprogrammed debug ROM device, PC card, complete instructions on the operation of all devices in the kit and all pertinent F8 literature.

F8M – MICROMODULE

A complete printed circuit subassembly capable of demonstrating the operation of a customer's program. Comes complete with F8M User's Manual and all pertinent F8 literature.

F8S – DEVELOPMENT MODULE

A complete printed circuit subassembly capable of developing, debugging and demonstrating the operation of a customer's program. Comes complete with F8S User's Manual and all pertinent F8 literature.

F8SEM – SYSTEM EXPANSION MODULE

A printed circuit subassembly designed to be used with the F8S Development Module to expand the system memory in 4K byte increments, and to expand the number of I/O ports in increments of four each.

F8SPDM – DEVELOPMENT MODULE SET

A combination set of modules containing one F8S Development Module, two F8SEM System Expansion Modules, an F8S Native Assembler, F8S and SEM User's Manuals and all other pertinent F8 literature. A more economical solution for the user requiring the expansion modules.

F8 FORMULATOR – COMPLETE MICROPROCESSOR DEVELOPMENT SYSTEM

A benchtop self-contained, modularized F8 development system, complete with front panel controls, cabinet, power supply, resident assembler and text editor, complete F8 Formulator Operating and System Reference manuals, and all other pertinent F8 literature.

F8 MICROPROCESSOR EVALUATION KIT

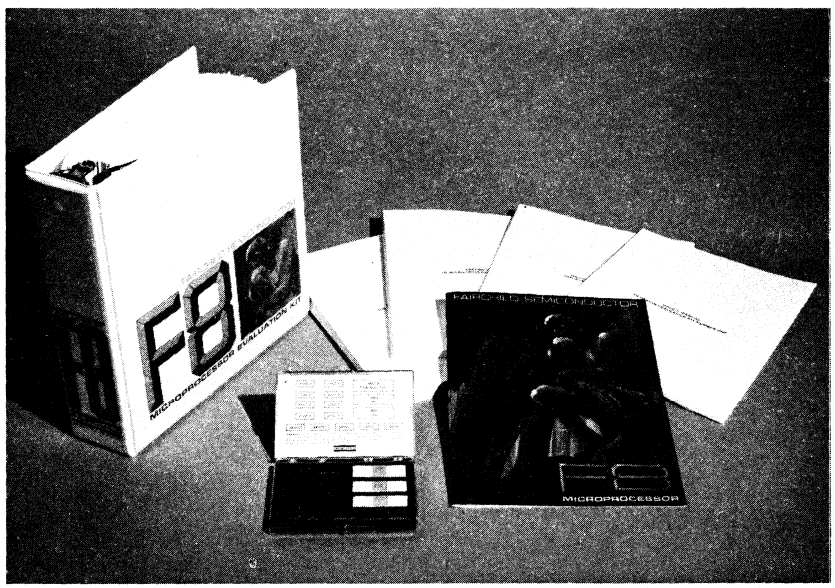
Fairchild's Microprocessor Evaluation Kit is designed for use by engineers, scientists and technicians in order to provide a straightforward method for constructing, using and evaluating prototype F8 microprocessor systems in real applications or training situations. It provides all of the semiconductor components, technical specifications, and instructions necessary to interconnect devices, demonstrate microprocessor programs up to 1K bytes in length, and to debug those programs.

The F8 Microprocessor Evaluation Kit contains the following semiconductor parts and documentation:

- 16 Semiconductor Devices, including
  - 1 – 3850 Central Processing Unit
  - 1 – 3851A* FAIR-BUG Programmed Storage Unit
  - 1 – 3853 Static Memory Interface
  - 8 – 2102-2 1K Static RAM Devices
  - 1 – 34001
  - 2 – 340097 } CMOS Gates and Buffers
  - 1 – 34023
  - 1 – 9N06 TTL Hex Inverter
- 1 PC Card to Facilitate Device Hook-up
- F8 Microprocessor Brochure
- F8 Design Evaluation Kit Instruction Manual
- A Guide to Programming the Fairchild F8 Microprocessor
- F8 Microprocessor Data Book
- F8 Timesharing Systems Operators Guide

*The 3851 FAIR-BUG PSU is a fixed programmed Fairchild 3851 PSU which provides the programmer with all its I/O subroutines and allows the programmer to display or alter memory and register contents via a teletype terminal.

The F8 Microprocessor Evaluation Kit is available now from your local Fairchild Franchised Distributor.



F8M – MICROMODULE

The F8M Micromodule is an inexpensive prototyping subassembly for the development and breadboarding of F8 Microprocessor designs. It is a complete printed circuit subassembly, requiring only the addition of power supplies and connection to a teleprinter to become fully operational.

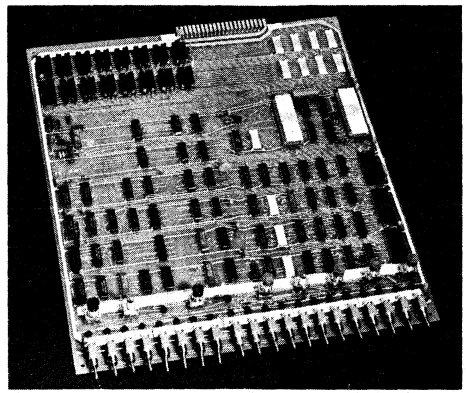
Features of the F8M include:

- Switches and LEDs Provide Control and Monitor Functions
- 1K Bytes of Static MOS RAM
- Sockets for 2K Bytes of Bipolar PROM (Fairchild 93426)
- 2 Preprogrammed 93426 Devices Forming a Bootstrap Loader
- External Interrupt
- 4 I/O Ports Available on the Edge Connector
- Programmable Interval Timer
- Serial Communications Interface, RS232 Format, 20 mA Current Loop

The customer's system is ready to demonstrate after the connection of peripheral circuits and either loading an object program into the RAM, or plugging in preprogrammed PROMs. The program can be halted and single-stepped to demonstrate statically how the design functions. Any PROM or ROM memory location can be monitored by halting the program. RAM memory locations can be altered before resuming operation of the system.

The F8M is supported by a Cross Assembler available for purchase from Fairchild Semiconductor or through a National Timesharing Network. Contact your Fairchild Sales Representative for more information.

The F8M Micromodule is available off the shelf for immediate delivery from your Fairchild Franchised Distributor.



F8S DEVELOPMENT MODULE

The F8S is an inexpensive F8 development and debugging subassembly. A self-contained complete printed circuit module, the F8S needs only power supply and connection to a teleprinter and the customer's peripheral circuits to form a complete F8 microcomputer system. Memory may be expanded to a maximum of 64K bytes with the system expansion modules described elsewhere in this brochure.

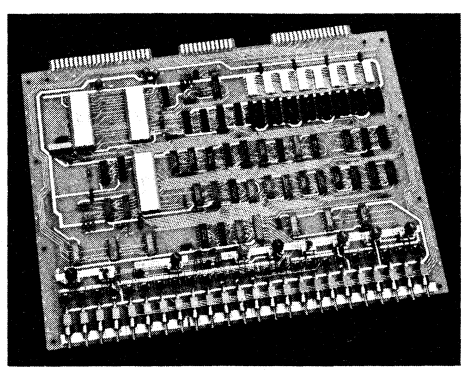
Features of the F8S include:

- Switches and LEDs Provide Control and Monitor Functions
- 64K Bytes of Addressable Memory Space (1K of Semiconductor Static RAM is Provided)
- Sockets for 2K Bytes of Bipolar PROM (Fairchild 93446)
- 2 External Interrupts
- 2 Programmable Interval Timers
- 4 Input/Output Ports (8 Bits Each)
- FAIR-BUG* Debugging Program

The F8S Development Module, with System Expansion Modules, allows source programs to be assembled inexpensively at the customer's location. Switches permit program RUN, HALT, and Single Step. Program breakpoints may be activated by changing instructions at the breakpoint locations. When a breakpoint is encountered, FAIR-BUG turns control over to you through the teleprinter. Commands consisting of single alphabetics allow you to examine or alter the contents of any memory location, group of locations or internal register of the CPU. Connection of peripheral circuits to the input/output ports enables the user to demonstrate his application.

The F8S is available now from your local Fairchild Franchised Distributor.

*The 3851 FAIR-BUG PSU is a fixed programmed Fairchild 3851 PSU which provides the programmer with all its I/O subroutines and allows the programmer to display or alter memory and register contents via a teletype terminal.



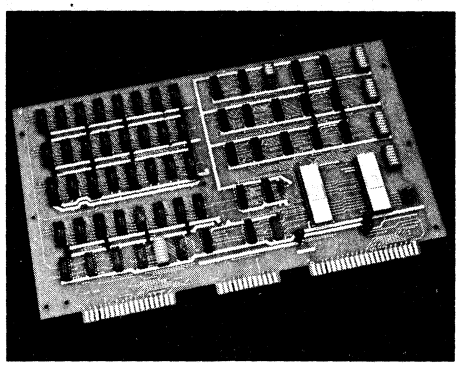
F8SEM – SYSTEM EXPANSION MODULE

Designed to operate with the F8S Development Module, the F8SEM System Expansion Module adds 4K byte increments of memory to the F8 development system and four additional I/O ports. Switches contained on the module allow the user to select the active page address that the module will respond to, the addresses of the input/output ports and the interrupt addresses.

Features of the F8SEM System Expansion Module include:

- 4K Bytes of Static RAM
- Memory Page Selection
- 4 Input/Output Ports (8 Bits Each)
- Switch Selectable I/O Port Addresses
- 2 External Interrupts
- 2 Programmable Interval Timers
- Switch Selectable Interrupt Addresses

Available October 1, 1975 from your local Fairchild Franchised Distributor.



F8SPDM – DEVELOPMENT MODULE SET

The F8SPDM is a combination set of modules containing one F8S module card, two F8SEM module cards, a paper tape F8S Native Assembler, and all necessary users manuals and F8 documentation literature.

Available October 1, 1975 from your local Fairchild Franchised Distributor.

F8 FORMULATOR

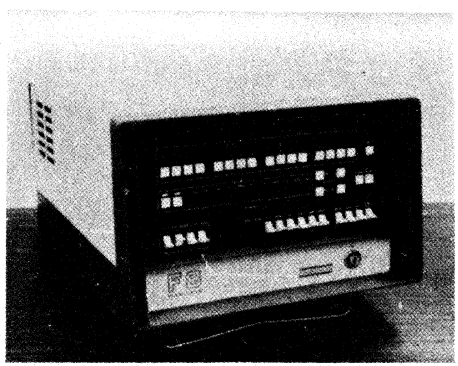
The F8 Formulator is a complete benchtop microprocessor development system designed to support every F8 application.

F8 Formulator features and capability include:

- F8 CPU Module
- Up to 64K Bytes of Addressable Memory
- Control and Monitor Console
- Virtually Unlimited Expansion of I/O Ports
- 2 External Interrupts Available for Every 4 I/O Ports
- Modular Construction
- Self-contained Power Supplies
- Resident Assembler
- Source Text Editor
- Complete Debug Capability

Standard memory modules and input/output modules permit expansion of the F8 Formulator to meet your need. Additional peripheral interfaces will also be available.

Available January 1976. Contact your local Fairchild salesman, representative or franchised distributor for pricing information.



F8 INSTRUCTION SET SUMMARY

The F8 instruction set contains over 60 different instructions which may be subdivided into 10 categories: Accumulator, Scratchpad Register, Indirect Scratchpad Address Register, Memory Reference, Data Counter, Status Register, Program Counter, Branch, Interrupt Control and Input/Output instructions. Because 55% of the F8 instructions are only one byte long, programs are short and memory requirements significantly reduced. An alphabetic listing of the instructions is shown below. The following pages contain a complete description of the F8 instructions, including the cycle time. Each cycle is 2 μs for a system with a 2 MHz clock frequency.

F8 ADDRESSING MODES

The F8 instruction set has eight modes of referencing either I/O, CPU registers or bulk memory.

Implied Addressing – The data for this one-byte instruction is implied by the actual instruction. For example, the POP instruction automatically implies that the content of the Program Counter will be set to the value contained in the Stack Register.

Direct Addressing – In these two-byte instructions, the address of the operand is contained in the second byte of the instruction. The Direct Addressing mode is used in the Input/Output class of instructions.

Short Immediate Addressing – Instructions whose addressing mode is Short Immediate have the instruction op code as the first four bits and the operand as the last four bits. They are all one-byte instructions.

Long Immediate Addressing – In these two-byte instructions, the first instruction byte is the op code and the second byte is the 8-bit operand.

Direct Register Addressing – This mode of addressing may be used to directly reference the Scratchpad Registers. By including the register number in the one-byte instruction, 12 of the 64 Scratchpad Registers may be referenced directly.

Indirect Register Addressing – All 64 Scratchpad Registers may be indirectly referenced, using the Indirect Scratchpad Register in the CPU. This 6-bit register, which acts as a pointer to the scratchpad memory, may either be incremented, decremented, or left unchanged while accessing the scratchpad register.

Indirect Memory Addressing – A 16-bit Indirect Address Register, the Data Counter, points to either data or constants in bulk memory. A group of one-byte instructions is provided to manipulate this area of memory. These instructions imply that the Data Counter is pointing to the desired memory byte. The Data Counter is self-incrementing, allowing for an entire data field to be scanned and manipulated without requiring special instructions to increment its content. The memory interface circuit contains two interchangeable data counters.

Relative Addressing – All F8 Branch Instructions use the relative addressing mode. Whenever a branch is taken, the Program Counter is updated by an 8-bit relative address contained in the second byte of the instruction. A branch may extend 128 locations forward or 127 locations back.

ALPHABETIC LIST OF INSTRUCTIONS

ADC	Add Data Counter with Accumulator
AI	Add Immediate with Accumulator
AM	Add Binary Accumulator with Memory
AMD	Add Decimal Accumulator with Memory
AS	Add Binary Accumulator with Scratchpad Register
ASD	Add Decimal Accumulator with Scratchpad Register
BC	Branch on Carry
BF	Branch on False Condition
BM	Branch if Negative
BNC	Branch if no Carry
BNO	Branch if no Overflow
BNZ	Branch if no Zero
BP	Branch if Positive
BR	Unconditional Branch
BR7	Branch if ISAR is not 7
BT	Branch on True Condition
BZ	Branch on Zero Condition
CI	Compare Immediate
CLR	Clear Accumulator
CM	Compare with Memory
COM	Complement Accumulator
DCI	Load Data Counter Immediate
DI	Disable Interrupt
DS	Decrement Scratchpad Register
EI	Enable Interrupt
INC	Increment Accumulator
IN	Input
INS	Input Short
JMP	Jump
LI	Load Accumulator Immediate
LIS	Load Accumulator Short
LISL	Load ISAR – Lower 3 Bits
LISU	Load ISAR – Upper 3 Bits
LM	Load Memory
LNK	Link Carry into Accumulator
LR	Load Register (5 Types)
	Scratchpad
	Program Counter
	ISAR
	Status
	Data Counter
NI	Logical AND Accumulator Immediate
NM	Logical AND from Memory
NOP	No Operation
NS	Logical AND Scratchpad and Accumulator
OI	Logical OR Immediate
OM	Logical OR Memory with Accumulator
OUT	Output
OUTS	Output Short
PI	Push Program Counter into Stack Register Set Program Counter to New Location
PK	Push Program Counter into Stack Register Set Program Counter from Scratchpad
POP	Put Stack Register into Program Counter
SL	Shift Left
SR	Shift Right
ST	Store to Memory
XDC	Exchange Data Counters
XI	Exclusive OR Immediate
XM	Exclusive OR Accumulator with Memory
XS	Exclusive OR Accumulator with Scratchpad

ACCUMULATOR GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD CARRY	LNK		ACC←(ACC) + CRY	19	1	1	1/0	1/0	1/0	1/0
ADD IMMEDIATE	AI	ii	ACC←(ACC) + H'ii'	24ii	2	2.5	1/0	1/0	1/0	1/0
AND IMMEDIATE	NI	ii	ACC←(ACC) ∧ H'ii'	21ii	2	2.5	0	1/0	0	1/0
CLEAR	CLR		ACC←H'00'	70	1	1	–	–	–	–
COMPARE IMMEDIATE	CI	ii	H'ii' + $(\overline{ACC})$ + 1	25ii	2	2.5	1/0	1/0	1/0	1/0
COMPLEMENT	COM		ACC←(ACC) ⊕ H'FF'	18	1	1	0	1/0	0	1/0
EXCLUSIVE-OR IMMEDIATE	XI	ii	ACC←(ACC) ⊕ H'ii'	23ii	2	2.5	0	1/0	0	1/0
INCREMENT	INC		ACC←(ACC) + 1	1F	1	1	1/0	1/0	1/0	1/0
LOAD IMMEDIATE	LI	ii	ACC←H'ii'	20ii	2	2.5	–	–	–	–
LOAD IMMEDIATE SHORT	LIS	i	ACC←H'0i'	7i	1	1	–	–	–	–
OR IMMEDIATE	OI	ii	ACC←(ACC) ∨ H'ii'	22ii	2	2.5	0	1/0	0	1/0
SHIFT LEFT ONE	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
SHIFT LEFT FOUR	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
SHIFT RIGHT ONE	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
SHIFT RIGHT FOUR	SR	4	SHIFT RIGHT 4	14	1	1	0	1/0	0	1

BRANCH INSTRUCTIONS

In all conditional branches PC_0←(PC_0) + 2 if the test condition is not met. Execution is complete in 3.0 cycles.

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
BRANCH ON CARRY	BC	aa	PC_0←[(PC_0) + 1] + H'aa' if CRY = 1	82aa	2	3.5	–	–	–	–
BRANCH ON POSITIVE	BP	aa	PC_0←[(PC_0) + 1] + H'aa' if SIGN = 1	81aa	2	3.5	–	–	–	–
BRANCH ON ZERO	BZ	aa	PC_0←[(PC_0) + 1] + H'aa' if ZERO = 1	84aa	2	3.5	–	–	–	–
BRANCH ON TRUE	BT	t, aa	PC_0←[(PC_0) + 1] + H'aa' if any test is true	8taa	2	3.5	–	–	–	–
BRANCH IF NEGATIVE	BM	aa	PC_0←[(PC_0) + 1] + H'aa' if SIGN = 0	91aa	2	3.5	–	–	–	–
BRANCH IF NO CARRY	BNC	aa	PC_0←[(PC_0) + 1] + H'aa' if CARRY = 0	92aa	2	3.5	–	–	–	–
BRANCH IF NO OVERFLOW	BNO	aa	PC_0←[(PC_0) + 1] + H'aa' if OVF = 0	98aa	2	3.5	–	–	–	–
BRANCH IF NOT ZERO	BNZ	aa	PC_0←[(PC_0) + 1] + H'aa' if ZERO = 0	94aa	2	3.5	–	–	–	–
BRANCH IF FALSE TEST	BF	t, aa	PC_0←[(PC_0) + 1] + H'aa' if all tests are met	9taa	2	3.5	–	–	–	–
BRANCH IF ISAR (LOWER) ≠ 7	BR7	aa	PC_0←[(PC_0) + 1] + H'aa' if ISARL ≠ 7 PC_0←(PC_0) + 2 if ISARL = 7	8Faa	2	2.5 2.0	–	–	–	–
BRANCH RELATIVE	BR	aa	PC_0←[(PC_0) + 1] + H'aa'	90aa	2	3.5	–	–	–	–
JUMP*	JMP	aaaa	PC_0←H'aaaa'	29aaaa	3	5.5	–	–	–	–

t = TEST CONDITION

2^2	2^1	2^0
ZERO	CRY	SIGN

t = TEST CONDITION

2^3	2^2	2^1	2^0
OVF	ZERO	CRY	SIGN

*Privileged instruction

MEMORY REFERENCE INSTRUCTIONS

In all Memory Reference Instructions, the Data Counter is incremented DC←DC + 1

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AM		ACC←(ACC) + ((DC))	88	1	2.5	1/0	1/0	1/0	1/0
ADD DECIMAL	AMD		ACC←(ACC) + ((DC))	89	1	2.5	1/0	1/0	1/0	1/0
AND	NM		ACC←(ACC) ∧ ((DC))	8A	1	2.5	0	1/0	0	1/0
COMPARE	CM		((DC)) + ($\overline{ACC}$) + 1	8D	1	2.5	1/0	1/0	1/0	1/0
EXCLUSIVE OR	XM		ACC←(ACC) ⊕ ((DC))	8C	1	2.5	0	1/0	0	1/0
LOAD	LM		ACC← ((DC))	16	1	2.5	–	–	–	–
LOGICAL OR	OM		ACC←(ACC) ∨ ((DC))	8B	1	2.5	0	1/0	0	1/0
STORE	ST		(DC)←(ACC)	17	1	2.5	–	–	–	–

ADDRESS REGISTER GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD to DATA COUNTER	ADC		DC←(DC) + (ACC)	8E	1	2.5	–	–	–	–
CALL to SUBROUTINE*	PK		PC_0U←(r12); PC_0L←(r13); PC_1←(PC_0)	0C	1	4	–	–	–	–
CALL to SUBROUTINE IMMEDIATE*	PI	aaaa	PC_1←(PC_0); PC_0←H'aaaa'	28aaaa	3	6.5	–	–	–	–
EXCHANGE DC	XDC		(DC_0) ⇄ (DC_1)	2C	1	2	–	–	–	–
LOAD DATA COUNTER	LR	DC,Q	DCU←(r14); DCL←(r15)	0F	1	4	–	–	–	–
LOAD DATA COUNTER	LR	DC,H	DCU←(r10); DCL←(r11)	10	1	4	–	–	–	–
LOAD DC IMMEDIATE	DCI	aaaa	DC←H'aaaa'	2Aaaaa	3	6	–	–	–	–
LOAD PROGRAM COUNTER	LR	PO,Q	PC_0U←(r14); PC_0L←(r15)	0D	1	4	–	–	–	–
LOAD STACK REGISTER	LR	P,K	PC_1U←(r12); PC_1L←(r13)	09	1	4	–	–	–	–
RETURN FROM SUBROUTINE*	POP		PC_0←(PC_1)	1C	1	2	–	–	–	–
STORE DATA COUNTER	LR	Q,DC	r14←(DCU); r15←(DCL)	0E	1	4	–	–	–	–
STORE DATA COUNTER	LR	H,DC	r10←(DCU); r11←(DCL)	11	1	4	–	–	–	–
STORE STACK REGISTER	LR	K,P	r12←(PC_1U); r13←(PC_1L)	08	1	4	–	–	–	–

SCRATCHPAD REGISTER INSTRUCTIONS

(Refer to Scratchpad Addressing Modes)

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AS	r	ACC←(ACC) + (r)	Cr	1	1	1/0	1/0	1/0	1/0
ADD DECIMAL	ASD	r	ACC←(ACC) + (r)	Dr	1	2	1/0	1/0	1/0	1/0
DECREMENT	DS	r	r←(r) + H'FF'	3r	1	1.5	1/0	1/0	1/0	1/0
LOAD	LR	A,r	ACC←(r)	4r	1	1	–	–	–	–
LOAD	LR	A,KU	ACC←(r12)	00	1	1	–	–	–	–
LOAD	LR	A,KL	ACC←(r13)	01	1	1	–	–	–	–
LOAD	LR	A,QU	ACC←(r14)	02	1	1	–	–	–	–
LOAD	LR	A,QL	ACC←(r15)	03	1	1	–	–	–	–
LOAD	LR	r,A	r←(ACC)	5r	1	1	–	–	–	–
LOAD	LR	KU,A	r12←(ACC)	04	1	1	–	–	–	–
LOAD	LR	KL,A	r13←(ACC)	05	1	1	–	–	–	–
LOAD	LR	QU,A	r14←(ACC)	06	1	1	–	–	–	–
LOAD	LR	QL,A	r15←(ACC)	07	1	1	–	–	–	–
AND	NS	r	ACC←(ACC) ∧ (r)	Fr	1	1	0	1/0	0	1/0
EXCLUSIVE OR	XS	r	ACC←(ACC) ⊕ (r)	Er	1	1	0	1/0	0	1/0

*Privileged instruction

MISCELLANEOUS INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
DISABLE INTERRUPT	DI		RESET ICB	1A	1	2	–	–	–	–
ENABLE INTERRUPT*	EI		SET ICB	1B	1	2	–	–	–	–
INPUT	IN	aa	ACC←(INPUT PORT aa)	26aa	2	4	0	1/0	0	1/0
INPUT SHORT	INS	a	ACC←(INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
LOAD ISAR	LR	IS,A	ISAR←(ACC)	0B	1	1	–	–	–	–
LOAD ISAR LOWER	LISL	a	ISARL←a	01101a**	1	1	–	–	–	–
LOAD ISAR UPPER	LISU	a	ISARU←a	01100a**	1	1	–	–	–	–
LOAD STATUS REGISTER*	LR	W,J	W←(r9)	1D	1	2	1/0	1/0	1/0	1/0
NO-OPERATION	NOP		PC_0←(PC_0) + 1	2B	1	1	–	–	–	–
OUTPUT	OUT	aa	OUTPUT PORT aa←(ACC)	27aa	2	4	–	–	–	–
OUTPUT SHORT	OUTS	a	OUTPUT PORT a←(ACC)	Ba	1	4***	–	–	–	–
STORE ISAR	LR	A,IS	ACC←(ISAR)	0A	1	1	–	–	–	–
STORE STATUS REG	LR	J,W	r9←(W)	1E	1	1	–	–	–	–

*Privileged instruction
**3-bit octal digit
***2 machine cycles for CPU ports

NOTES.

Each lower case character represents a Hexadecimal digit
Each cycle equals 4 machine clock periods
Lower case denotes variables specified by programmer

Function Definitions

←	is replaced by
( )	the contents of
(–)	Binary "1"s complement of
+	Arithmetic Add (Binary or Decimal)
⊕	Logical "OR" exclusive
∧	Logical "AND"
∨	Logical "OR" inclusive
H' '	Hexadecimal digit

Register Names

a	Address Variable
A	Accumulator
DC	Data Counter (Indirect Address Register)
DC_0	Data Counter #0 (Indirect Address Register #0)
DC_1	Data Counter #1 (Indirect Address Register #1)
DCL	Least significant 8 bits of Data Counter Addressed
DCU	Most significant 8 bits of Data Counter Addressed
H	Scratchpad Register #10 and #11
i and ii	immediate operand
ICB	Interrupt Control Bit
IS	Indirect Scratchpad Address Register
ISAR	Indirect Scratchpad Address Register
ISARL	Least Significant 3 bits of ISAR
ISARU	Most Significant 3 bits of ISAR
J	Scratchpad Register #9
K	Registers #12 and #13
KL	Register #13
KU	Register #12
PC_0	Program Counter
PC_0L	Least Significant 8 bits of Program Counter
PC_0U	Most Significant 8 bits of Program Counter
PC_1	Stack Register
PC_1L	Least Significant 8 bits of Program Counter
PC_1U	Most Significant 8 bits of Active Stack Register
Q	Registers #14 and #15
QL	Register #15
QU	Register #14
r	Scratchpad Register (any address thru 11)
W	Status Register

Scratchpad Addressing Modes (Machine Code Format)

r = C	(Hexadecimal), Register Addressed by ISAR (Unmodified)
r = D	(Hexadecimal), Register Addressed by ISAR; ISARL Incremented
r = E	(Hexadecimal), Register Addressed by ISAR; ISARL Decremented
r = F	(No operation performed)
r = 0 thru B	(Hexadecimal), Register 0 thru 11 addressed directly from the Instruction

Status Register

–	No change in condition
1/0	is set to "1" or "0" depending on conditions
CRY	Carry Flag
OVF	Overflow Flag
SIGN	Sign of Result Flag
ZERO	Zero Flag

POWER REQUIREMENTS: V_{DD} = +5.0 V ±5%; V_{GG} = +12.0 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; f = 2 MHz

PART TYPE	SYMBOL	PARAMETER	TYP	MAX	UNITS	TEST CONDITIONS (Outputs Unloaded)
3850	I_{DD}	V_{DD} Current	30	80	mA	2 MHz
	I_{GG}	V_{GG} Current	15	25	mA	
3851	I_{DD}	V_{DD} Current	30	70	mA	2 MHz
	I_{GG}	V_{GG} Current	10	18	mA	
3852	I_{DD}	V_{DD} Current	35	70	mA	2 MHz
3853	I_{GG}	V_{GG} Current	13	30	mA	
3854	I_{DD}	V_{DD} Current	20	40	mA	2 MHz
	I_{GG}	V_{GG} Current	15	28	mA	

SIGNAL ELECTRICAL SPECIFICATIONS: V_{DD} = +5.0 V ±5%; V_{GG} = +12.0 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C, f = 2 MHz

SIGNAL NAME (NUMBER, TYPE)	SOURCE OR RECEIVING DEVICE	V_{OH} MIN	V_{IH} MIN	V_{OL} MAX	V_{IL} MAX	LOAD
DATA BUS (8 INPUTS/OUTPUTS)	3850 3851 3852/3 3854	3.9	3.5	0.4	0.8	100 pF I_{SOURCE} 100 μA I_{SINK} 900 μA
CONTROL BUS (5 OUTPUTS)	3850	3.9		0.4		100 pF, I_{SINK} 900 μA I_{SOURCE} 100 μA
CONTROL BUS (5 INPUTS)[1]	3851 3852/3		3.5		0.8	
I/O PORTS (16 INPUTS/OUTPUTS)	3850 3851	2.9 (1 TTL) 3.9 (unloaded)	3.5[2]	0.4	0.8	-100 pF plus 1 H-TTL Load
CLOCK REFERENCE (INPUT)	3850		4.0		0.8	
SYSTEM CLOCKS (PHI AND WRITE OUTPUTS)	3850	4.4		0.4		100 pF, I_{SINK} 900 μA I_{SOURCE} 100 μA
SYSTEM CLOCKS (PHI AND WRITE INPUTS)	3851 3852/3 3854		4.0		0.8	
RESET (INPUT)	3850		3.5[2]		0.8	I_{IL} = 0.3 mA Max at V_{IN} = V_{SS}
INTERRUPT CONTROL BIT (OUTPUT)	3850	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
INTERRUPT REQUEST (INPUT)	3850		3.5[2]		0.8	I_{IL} = 1 mA Max at V_{IN} = 0.4
INTERRUPT REQUEST (OUTPUT)	3851 3853	OPEN DRAIN		0.4		100 pF plus I_{SINK} = 1 mA
EXTERNAL INTERRUPT (INPUT)	3851 3853		3.5		1.2	
PRIORITY IN (INPUT)	3851 3853		3.5		0.8	
PRIORITY OUT (OUTPUT)	3851	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
DBDR (OUTPUT)	3851	OPEN DRAIN[3]		0.4		100 pF plus I_{SINK} = 2.5 mA
ADDRESS LINES and RAM WRITE (16 OUTPUTS)	3852/3 3854	4.0		0.4		500 pF plus 2 TTL Loads
REGDR (INPUT/OUTPUT)	3852/3	3.9	3.5	0.4	0.8	100 pF plus 1 H-TTL Load
CPU READ (OUTPUT)	3852/3	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE, CYCLE REQ and CPU SLOT (OUTPUTS)	3852	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE (INPUT)	3854		3.5		0.8	
ENABLE, DIRECTION, TRANSFER, DMA WRITE SLOT, STROBE (OUTPUTS)	3854	3.9		0.4		50 pF plus 1 H-TTL Load
XFER REQ, P1,P2 (INPUTS)	3854		3.5		0.8	
LOAD REG, READ REG (INPUTS)	3854		3.5		0.8	

[1]3854 receives two control signals from external decoding device. [2]Internal pull-up resistor to V_{DD}. [3]External pull-up resistor required.

3843
UNIVERSAL SYNCHRONOUS AND ASYNCHRONOUS RECEIVER/TRANSMITTER (USART)

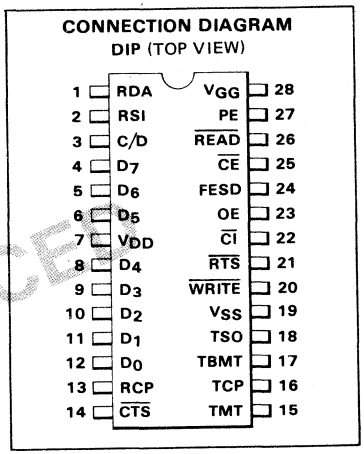
GENERAL DESCRIPTION – The 3843 USART is a complete serial communications formatting device. It receives serial data in virtually any format now in use and converts that data to parallel data in a form suitable for inputing to a microcomputer system. Conversely, it transmits microcomputer output data in a program-determined format. The USART is a peripheral device intended for use with a CPU controlling the format/configuration of the USART logic.

The USART has the capability of detecting simple parity errors and notifying the CPU of such errors in data transmission. It will also detect framing and overrun errors and notify the CPU when they occur.

The USART can simultaneously receive and transmit data in the format specified by the CPU.

- **VARIABLE CHARACTER LENGTH – 5, 6, 7, 8 BITS**
- **VARIABLE NUMBER OF STOP BITS – 1, 1-1/2, OR 2**
- **SELECTABLE TRANSMIT AND RECEIVE CLOCK RATES**
- **EVEN OR ODD PARITY DETECTION AND GENERATION**
- **FULL DUPLEX OPERATION – DOUBLE BUFFERED**
- **TTL COMPATIBLE ON INPUTS AND OUTPUTS**
- **STANDARD 28-PIN DUAL IN-LINE PACKAGE**

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

PIN NO.	LABEL/NAME	FUNCTION
1	RDA, RECEIVER DATA AVAILABLE	FLAG – Data available in receiver buffer register.
2	RSI, RECEIVER SERIAL IN	Serial input port for receiver.
3	C/D, CONTROL/DATA	During Write mode – This input differentiates a control word from a data word. C/D equal to a "1" indicates a control word. During Read mode – The input selects the data presented to the Data Bus Ports. C/D equal to "1" selects the status register. C/D equal to "0" selects the receiver register.
4,5,6, 8,9,10, 11,12	$D_0 - D_7$ DATA BUS PORTS	3-state I/O controlled by the $\overline{READ}$ input. $\overline{READ}$ equal to "0" drives out data.
7	V_{DD}, DRAIN VOLTAGE	Power
13	RCP, RECEIVER CLOCK INPUT	Clock
14	$\overline{CTS}$, CLEAR TO SEND	The transmitter is disabled until $\overline{CTS}$ is dropped.
15	TMT, TRANSMITTER REGISTER EMPTY	FLAG – Transmission of last word complete. TSO is mark time or sync words.
16	TCP, TRANSMITTER CLOCK IN	Clock
17	TBMT, TRANSMITTER BUFFER EMPTY	FLAG – Last word has been transferred to transmitter register and the buffer can accept a new word.
18	TSO, TRANSMITTER SERIAL OUT	Serial data output port for transmitter.
19	V_{SS}, SOURCE VOLTAGE	Power
20	$\overline{WRITE}$	Input is dropped to write data or control word into device.
21	$\overline{RTS}$, REQUEST TO SEND	Output from command register bit 1.
22	$\overline{CI}$, CHIP INITIALIZE	Input is dropped to cancel flags and initialize counters.
23	OE, OVERRUN ERROR	FLAG – Receiver buffer has been loaded with new data and the prior data had not been read out by controller.
24	FESD, FRAMING ERROR, SYNC DETECTED, or EXTERNAL SYNC	FLAG/INPUT – This pin is a FLAG during asynchronous and internal sync modes and an input during external sync mode.
25	$\overline{CE}$, CHIP ENABLE	Input is dropped when the device is selected for a READ/WRITE operation.
26	$\overline{READ}$	Input is dropped to read Data Bus Ports, outputs.
27	PE, PARITY ERROR	FLAG
28	V_{GG}, GATE VOLTAGE	Power

3705/3708

MOS MONOLITHIC 8-CHANNEL MULTIPLEX SWITCH

GENERAL DESCRIPTION — The 3705/3708 are 8-Channel Multiplex Switches with an output enable control and one-out-of-eight decoder included on-chip. They are manufactured using p-channel enhancement mode silicon gate technology. The logic input lines are npn bipolar compatible and can be used directly with TTL 5.0 V logic levels with no level shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

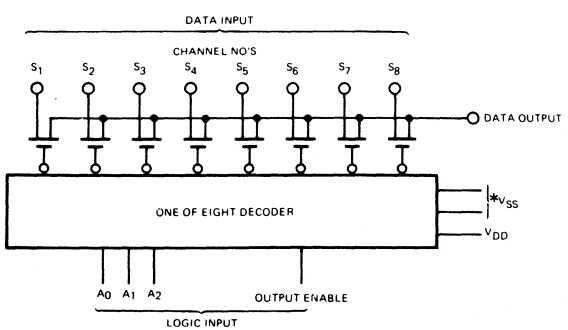
- **ONE-OUT-OF-EIGHT DECODER ON THE CHIP**
- **HIGH OFF-RESISTANCE-TO-ON-RESISTANCE RATIO**
- **OUTPUT ENABLE CONTROL**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**
- **FAST SWITCHING TIME: 1.0 μs (MAX) AT T_A = +85°C (3705 DL)**
- **TTL COMPATIBLE INPUT LOGIC LEVELS**

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	
DC	0°C to +70°C
DL	−55°C to +85°C
DM	−55°C to +125°C
Positive Voltage on any Pin	+0.3 V
Negative Voltage on Digital and Analog Input Pins	−30 V
Negative Voltage on Digital and Analog Output Pins	−30 V
Negative Voltage on V_{DD}	−30 V
Total Power Dissipation in Package (T_A = 25°C)	200 mW

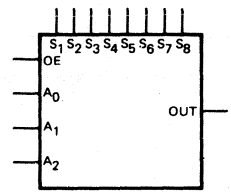
NOTES:
1. These ratings are limiting values above which the serviceability of the device may be impaired.
2. Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

BLOCK DIAGRAM



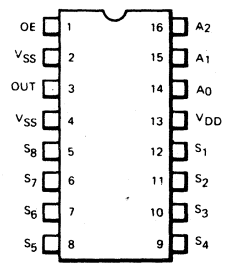
*Both V_{SS} lines are internally connected; either one or both may be used.

LOGIC SYMBOL



V_{SS} = Pins 2 and 4
V_{DD} = Pin 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

LOGIC INPUTS				CHANNEL
A_0	A_1	A_2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

ELECTRICAL CHARACTERISTICS

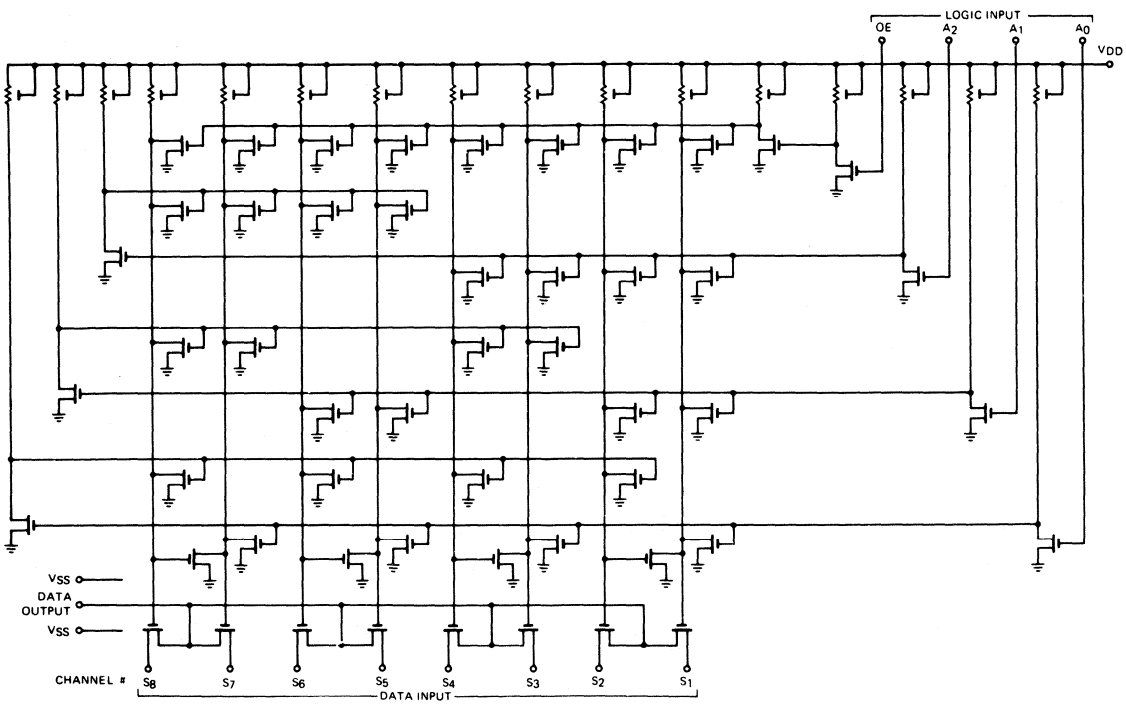
For 3705: V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −22 ±2 V, V_{SS} = 6.0 ±1 V
For 3708: V_{OUT} = −5.0 V to +5.0 V, V_{DD} = −19 ±1 V, V_{SS} = 5.5 ±0.5 V

T_A = DC 0°C to +70°C; DL −55°C to +85°C; DM −55°C to +125°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
*V_{IH}	Input HIGH Voltage	V_{SS} −1.5		V_{SS}	V	
*V_{IL}	Input LOW Voltage	V_{DD}		0.8	V	
I_{LI}	Logic Input Leakage Current			10	μA	$V_{SS} - V_{LOGIC\text{-}IN}$ = 15 V
I_{LD}	Data Input Leakage Current			500	nA	$V_{SS} - V_{IN}$ = 15 V
I_{LO}	Output Leakage Current			500	nA	$V_{SS} - V_{OUT}$ = 15 V
R_{ON}	Data Channel "ON" Resistance					
	3705			400	Ω	V_{OUT} = −5.0 V, I_{OUT} = −100 μA
	3708			450	Ω	V_{OUT} = −5.0 V, I_{OUT} = −100 μA
P_D	Power Dissipation			175	mW	V_{DD} = −26 V, V_{SS} = 0 V
t_S	Channel Switching Time			1.3	μs	3705 DM (Fig. 1)
				1.0	μs	3705 DL, DC (Fig. 1)
				1.5	μs	3708 DL, DC (Fig. 1)

*When driven by TTL elements, avoid excessive dc loading of TTL elements to insure 3708 logic levels under maximum fanout conditions. Analog input signal swing should not exceed V_{SS} (= V_{CC}).

SCHEMATIC DIAGRAM



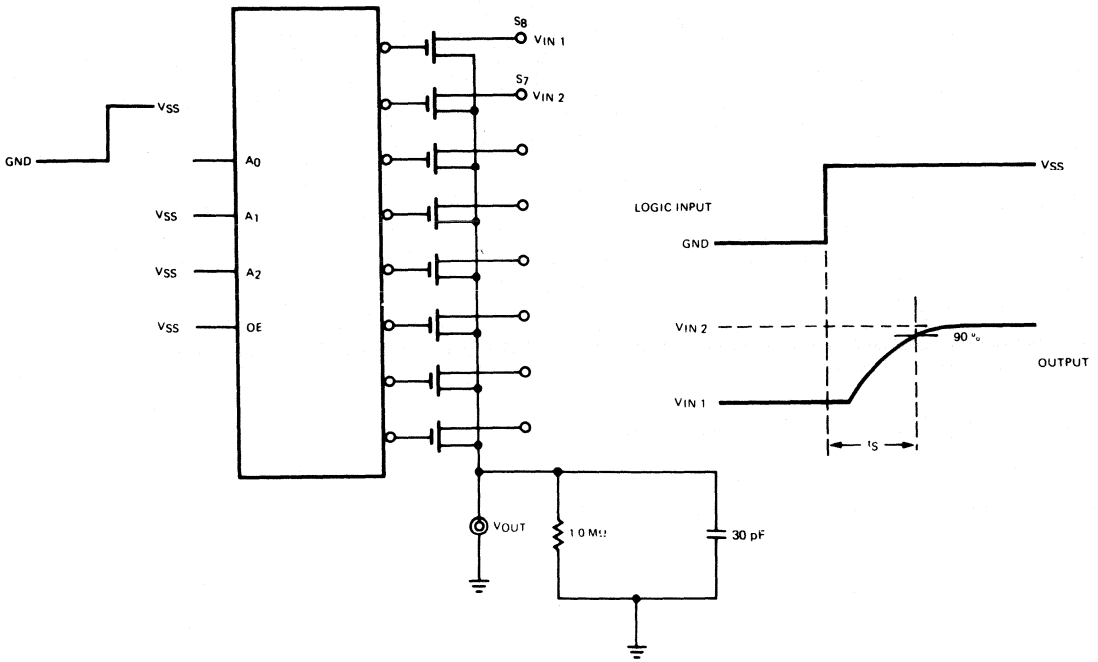
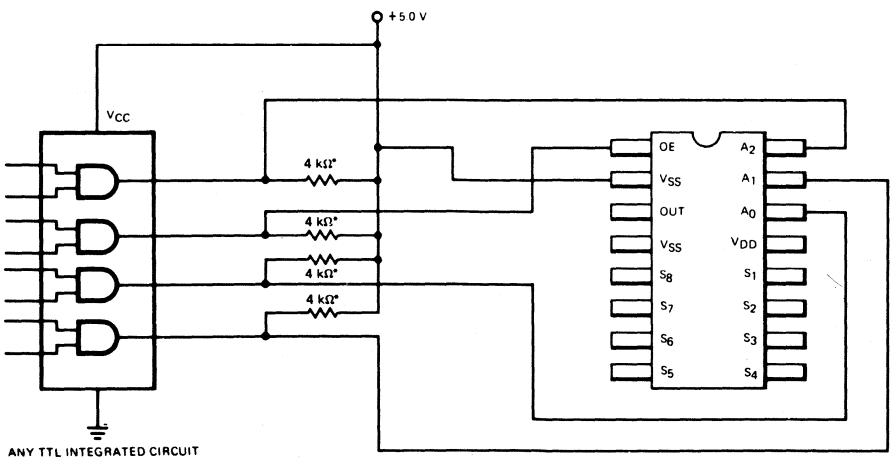


Fig. 1 SWITCHING TIME TEST CIRCUIT



*Optional components – not needed if TTL fanout is limited to 1.

Fig. 2 TYPICAL CONTROL CIRCUIT

3815
5-DECADE COUNTER

GENERAL DESCRIPTION – The 3815 is a 5-Decade Counter which includes a memory with static latches for each counter digit and an output multiplexer. Cathode driving, clock synchronization and decimal point logic are also provided. The 3815 is designed to drive a multiplexed display which has a Binary Coded Decimal output (drives a BCD converter plus low power latches, if necessary) and five decoded outputs to strobe the display.

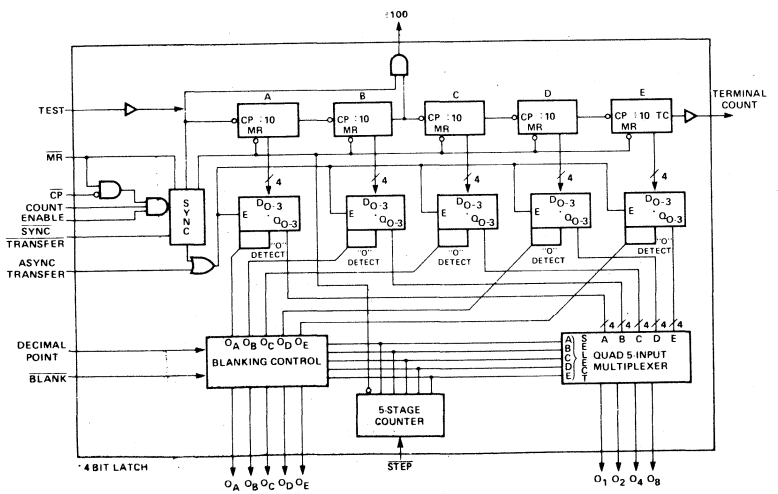
Automatic leading zero blanking is simply accomplished and a separate input is provided to blank the entire display. Other outputs provide terminal count indication and an output which can be used to drive the display outputs. The 3815 is manufactured using silicon gate p-channel technology.

- **DIRECT TTL/DTL COMPATIBILITY – NO EXTERNAL COMPONENTS**
- **DC TO 600 kHz OPERATION**
- **BCD OUTPUT – COMPATIBLE WITH DISPLAY DECODERS**
- **EXTERNAL CONTROL MULTIPLEX FREQUENCY – ACCOMMODATES LED DISPLAYS**

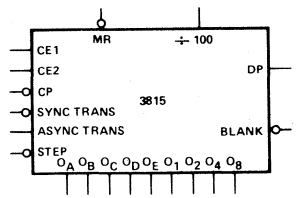
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to 70°C
V_{GG}	+0.3 to -24V
All Other Inputs	+0.3 to -16V
Outputs	+0.3 to -8V (I_L < 10 mA)

BLOCK DIAGRAM

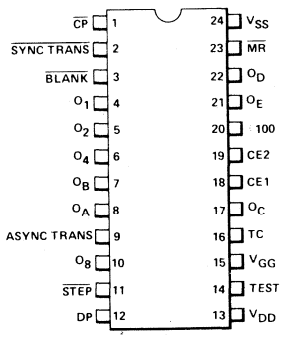


LOGIC SYMBOL



V_{SS} = +5 V ±5% = Pin 24
V_{DD} = GND = Pin 13
V_{GG} = −12 V ±5% = Pin 15

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

$\overline{CP}$	Clock Input
$\overline{SYNC\ TRANS}$	Synchronous Transfer Control
$\overline{BLANK}$	Display Blanking Control
O_1, O_2, O_4, O_8	BCD Counter Outputs
O_A, O_B, O_C, O_D, O_E	Digit Scanner Outputs
ASYNCH TRANS	Asynchronous Transfer Control
$\overline{STEP}$	Digit Scanner Step Control
DP	Decimal Point Control
TC	Terminal Count Output
÷100	Divide-by-100 Output
Test	Test Input (Tie to V_{SS})
$\overline{MR}$	Master Reset
CE_X	Count Enable Controls

FUNCTIONAL DESCRIPTION – Incrementing the counters is accomplished through a coordination of a clock input to $\overline{CP}$ (pin 1) and the count enables CE_1 (pin 18) and CE_2 (pin 19) being in a logic "1" or HIGH state. Both CE_1 and CE_2 will be enabled if these inputs are left open. Both must be HIGH for counting to occur. Output of the second decade is gated with the input clock and brought off chip as the ÷100 (pin 20) output. Count 99999 is gated with input clock LOW to provide a terminal count indication, TC (pin 16).

Memory update is accomplished in either of two ways. Present count may be transferred to the latches using the asynchronous transfer AT (pin 9) if there is no clock at the $\overline{CP}$ input during transfer or if clock LOW cannot be guaranteed. Synchronous Transfer $\overline{ST}$ (pin 2) is gated with the clock input on-chip during clock LOW. It is possible to load erronous results into memory if an AT command is received during the $\overline{CP}$ LOW to HIGH transition. It is during this transition that the flip-flops are settling out information on the slaves. Sync Transfer is active LOW and Async Transfer is active HIGH. $\overline{MR}$ (pin 23) is a master reset which synchronously sets all the counters to zero. Note that $\overline{MR}$ resets the scanner counter to the A decade.

The latched state of each decade is multiplexed out as BCD data on the outputs labeled O_1, O_2, O_4, and O_8 (pins 4, 5, 6, and 10, respectively). The on chip multiplexer is driven by a 5-state scanner counter whose outputs are gated out as the O_A, O_B, O_C, O_D, and O_E (pins 8, 7, 17, 22, and 21 respectively) outputs. The scanner counter is advanced by pulses fed into the STEP (pin 11) input. As the scanner is clocked, the stored data appears, decade by decade on the O_1 through O_8 outputs. Simultaneously, one of the O_A through O_E outputs will go HIGH indicating which decade is being displayed. A LOW on the BLANK input (pin 3) causes all five O_A through O_E outputs to go LOW. Because outputs O_A through O_E can drive display lamps in a multiplexed system, the display will blank when they are LOW.

The position of the decimal point in the display is selected by an external control. For zero suppression, the DP input of the 3815 must be driven by one of the five Digit Select (O_A through O_E) outputs. This feedback inhibits the zero suppression for that decade and all remaining decades to the right. If the DP input is tied to V_{SS}, all digits are displayed. Tying DP to V_{DD} has the same effect as tying it to output O_E.

DIGIT CONNECTED TO DECIMAL POINT	EXAMPLE COUNT	DISPLAY*
A, or DP = V_{SS}	00000	0
A, or DP = V_{SS}	00120	120
B	00120	12.0
C	00120	1.20
D	00120	0.120
E, or DP = V_{DD}	00120	0.0120
		E DCBA

*The decimal point itself in the display is not controlled by the 3815.

TEST INPUT – This pin is used during the testing of the 3815 and must be wired to V_{SS} for operation.

DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = –12 V ±5%, T_A = 0°C to +70°C

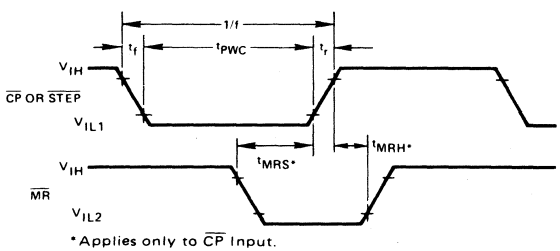
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	V_{SS}–1.0		V_{SS}+0.3	V	All Inputs Including $\overline{CP}$
V_{IL1}	Input LOW Voltage	–2		+0.5	V	$\overline{CP}$ and $\overline{STEP}$
V_{IL2}	Input LOW Voltage	–2		0.8	V	All Other Inputs
V_{OH1}	Output HIGH Voltage	2.4		V_{SS}	V	a) Sourcing 200 μA for Output TC, C_L <20 pF b) Sourcing 400 μA for Outputs O_1, O_2, O_4, O_8; C_L <30 pF
V_{OH2}	Output HIGH Voltage	V_{SS}–1.0		V_{SS}	V	Sourcing 200 μA for Outputs O_A, O_B, O_C, O_D, O_E, ÷ 100; C_l <20 pF
V_{OL}	Output LOW Voltage			0.4	V	a) Sink 1.6 mA on Outputs TC, O_A, O_B, O_C, O_D, O_E, ÷ 100, C_L <20 pF b) Sink 2.0 mA on Outputs O_1, O_2, O_4, O_8; C_L <30 pF
R_{IN1}	Input Resistor Returned to V_{SS}	1	2.5	5	kΩ	Inputs: $\overline{CP}$ $\overline{Blank}$ $\overline{MR}$, $\overline{Sync\ Transfer}$ Async Transfer, Count Enable
R_{IN2}	Input Resistor Returned to V_{SS}	10	25	50	kΩ	Inputs: $\overline{Step}$, DP, Test
I_{GG}	V_{GG} Supply Current	3	5	15	mA	
I_{SS}	V_{SS} Supply Current	20	30	50	mA	

AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{DD} = 0 V, V_{GG} = −12 V ±5%, T_A = 0°C to 70°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
f	Operating Frequency	DC		600	kHz	Fig. 1
t_{PWC}	Clock Pulse Width ($\overline{STEP}$ and $\overline{CP}$)	300	220		ns	Fig. 1
t_{STS}	$\overline{SYNC\ TRANS}$ Set Up Time	300			ns	Fig. 2
t_{STH}	$\overline{SYNC\ TRANS}$ Hold Time	200			ns	Fig. 2
t_{SET}	Separation, Count Enable to ASYNC TRANS	500			ns	Fig. 5
t_{PWAT}	ASYNC TRANS Pulse Width	500			ns	Fig. 5
t_{SCT}	Separation Clock to $\overline{SYNC\ TRANS}$	200			ns	Fig. 2
t_{STC}	Separation $\overline{SYNC\ TRANS}$ to Clock	200			ns	Fig. 2
t_{DHL}	HIGH to LOW Transition for Outputs					
	÷ 100		320	1000	ns	Fig. 3
	TC		400	800	ns	Fig. 3
	O_1, O_2, O_4, O_8		450	1000	ns	Fig. 4
t_{DLH}	LOW to HIGH Transition for Outputs					
	÷ 100		350	1000	ns	Fig. 3
	TC		425	800	ns	Fig. 3
	O_1, O_2, O_4, O_8		550	1000	ns	Fig. 4
$t_{r,f}$	Clock Rise and Fall Times			200	ns	Fig. 1
t_{MRS}	Master Reset Set-Up Time	300			ns	Fig. 1
t_{MRH}	Master Reset Hold Time	200			ns	Fig. 1

TIMING DIAGRAMS

INPUT CLOCK ($\overline{STEP}$ and $\overline{CP}$) WAVEFORM



*Applies only to $\overline{CP}$ Input.

Fig. 1

SYNC TRANSFER SETUP AND HOLD TIMES

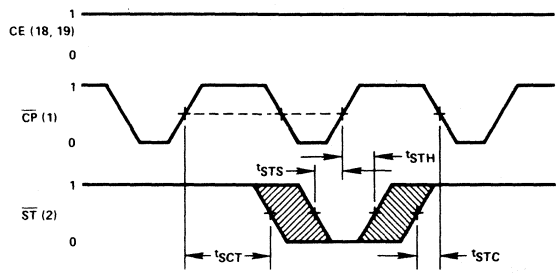


Fig. 2

PROPAGATION DELAY–OUTPUTS

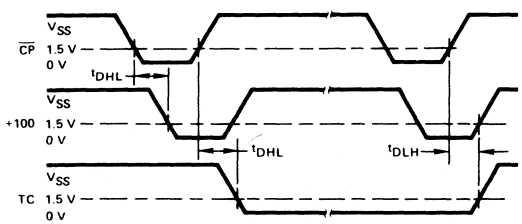


Fig. 3

PROPAGATION DELAY–BCD OUTPUTS

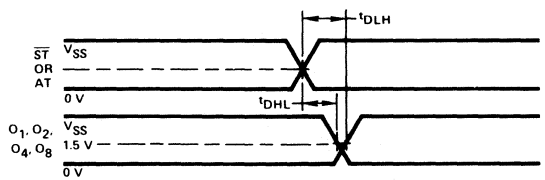


Fig. 4

ASYNC TRANSFER TIMING

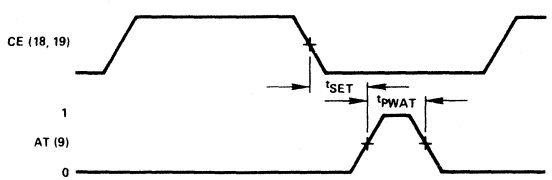


Fig. 5

3816
PROGRAMMABLE DIVIDER (3 through 262,145)

GENERAL DESCRIPTION – The 3816 is a programmable counter capable of dividing by any modulo from three to 262, 145 ($2^{18}+1$). The 3816 uses only nine leads to program 18 bits by applying one of four conditions to the nine leads.

This device is packaged in a hermetic ceramic 16-pin Dual In-line package and is specified for operation over the 0°C to +70°C temperature range. It is manufactured using silicon gate p-channel technology.

- **DC – 1.5 MHz**
- **FULL 18 BITS IN 16-LEAD PACKAGE**
- **TTL COMPATIBILITY**

PIN NAMES

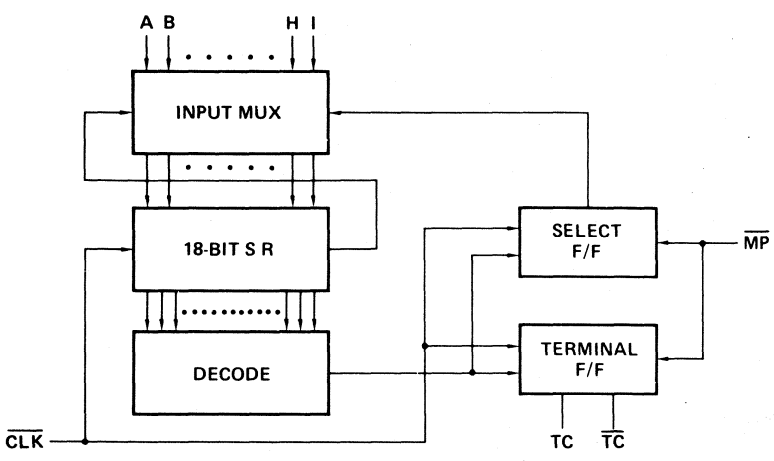
A-I	Program Inputs
$\overline{MP}$	Master Preset
$\overline{CLK}$	Clock
$\overline{TC}$	Terminal Count
TC	Terminal Count

ABSOLUTE MAXIMUM RATINGS

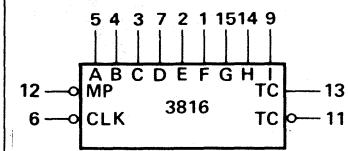
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
V_{GG}	+0.3 V to −24 V
All other inputs	+0.3 V to −16 V
Outputs (<10 mA)	+0.3 V to −16 V

Note: All voltages referenced to V_{SS}.

BLOCK DIAGRAM

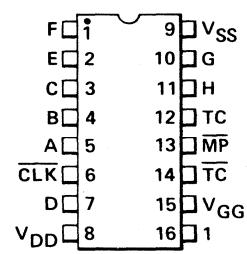


LOGIC SYMBOL



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to +70°C (unless otherwise specified)

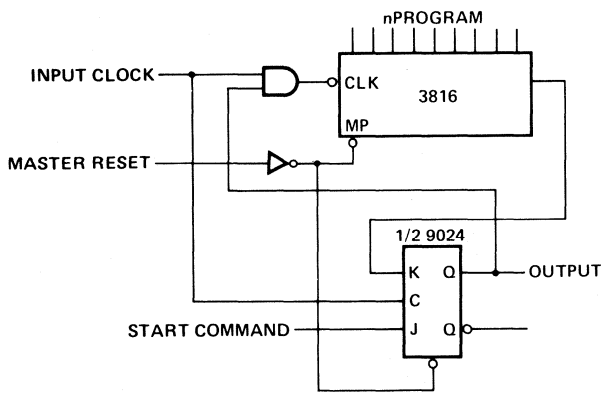
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	V_{SS} −1.0		V_{SS} +0.3	V	
V_{IL}	Input LOW Voltage			0.5	V	
V_{OH}	Output HIGH Voltage	2.4		V_{SS}	V	I_{OH} = 0.2 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
I_{LI}	Input Leakage Current			1.0	μA	V_{IN} = V_{SS}
R	Input Pull-up Resistor		2.5		kΩ	
I_{SS}	V_{SS} Current		12		mA	
I_{GG}	V_{GG} Current		2.5		mA	

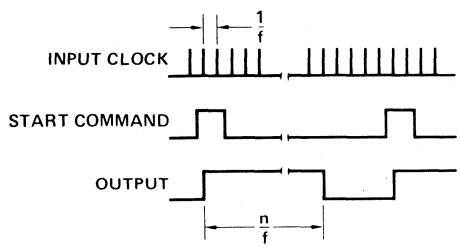
AC CHARACTERISTICS: V_{SS} = +5.0 V ±5%, V_{GG} = −12 V ±5%, V_{DD} = 0 V, T_A = 0°C to +70°C

SYMBOL	PARAMETER	LIMITS		UNITS
		MIN	MAX	
f	Operating Frequency		1.5	MHz
t_{PWH}	Clock Pulse Width HIGH	300		ns
t_{PWL}	Clock Pulse Width LOW	300		ns
t_r, t_f	Clock Rise and Fall		500	ns
t_{PWP}	Preset Pulse Width	1000		ns
t_{CTD}	Clock to TC, $\overline{TC}$ Delay		300	ns

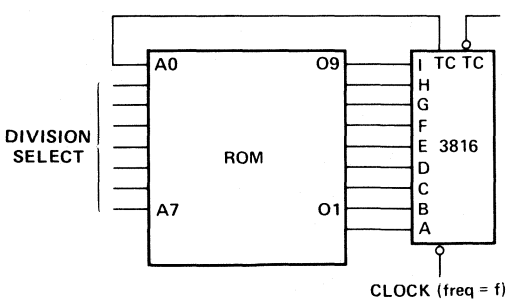
APPLICATION

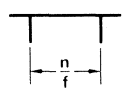
DIGITAL ONE SHOT – This circuit provides a pulse of duration n/f starting at the first positive transition of Input Clock following a Start Command. Start Command HIGH must be shorter than n/f.





PROGRAMMABLE COUNTER – This circuit converts regular binary instructions into the required coding for programming the 3816. As the diagram shows, any ROM or PROM with at least nine outputs will work. Twice as many words are required as there are different divisions required.





Example: 128 division, ROM = 256 x 9. Tie TC to A0
If ÷ 10,000 is required with A1 thru A7 at 100, then the programming is as follows:
÷ 10,000 = TDSNNNNNS (A through I)

ADDRESS*

A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	1	0	0	0
1	1	0	0	1	0	0	1

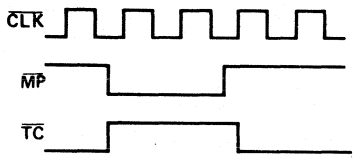
*Decimal address 100 on A_1 – A_7

OUTPUT

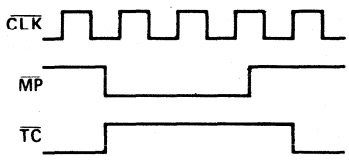
A O1	B O2	C O3	D O4	E O5	F O6	G O7	H O8	I O9
0	0	1	1	1	1	1	1	1
1	0	1	0	0	0	0	0	1

FUNCTIONAL DESCRIPTION – The 3816 is intended for application where a division of a central timing signal is required. An 18-bit linear feedback shift register provides the counting medium. Nine inputs are used to program the counter with each lead selectively connected to V_{DD} (Ground), V_{SS} (+5.0 V), TC (Terminal Count) or $\overline{TC}$ (Not Terminal Count). This method allows each lead to preset two flip-flops consecutively (one at TC being HIGH and the other at one clock time later). This allows the programming of 18 bits with nine leads.

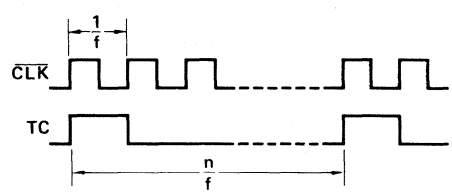
TIMING – A Master Preset ($\overline{MP}$) LOW always overrides the counter and forces the 3816 to the TC HIGH state. When $\overline{MP}$ is brought HIGH, the counter will increment on the first positive going $\overline{CLK}$ transition if $\overline{CLK}$ is LOW. When the counter increments, TC will go LOW. TC will go HIGH again n (the programmed number) $\overline{CLK}$ pulses after $\overline{MP}$ goes HIGH. The 3816 increments on the positive going transition of $\overline{CLK}$.



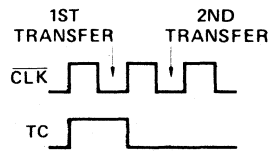
a. Preset Timing ($\overline{CLK}$ LOW)



b. Preset Timing ($\overline{CLK}$ HIGH)



c. Regular Timing



d. Transfer Points

PROGRAMMING – The 3816 is programmed by applying one of four conditions to nine leads. These conditions are labeled as follows:

SYMBOL	TIE TO	TC = 1 1ST TRANSFER	TC = 0 2ND TRANSFER
S	V_{SS}	1	1
D	V_{DD}	0	0
T	TC	1	0
N	$\overline{TC}$	0	1

A shorthand notation has been developed to represent the connections required for a specific division. This shorthand is a group of nine of the above four symbols. These symbols are written with A (Pin 5) on the left followed by B (Pin 4), C (Pin 3), D (Pin 7), E (Pin 2), F (Pin 1), G (Pin 15), H (Pin 14) and ending with I (Pin 9) on the right.

Some examples of this shorthand for specific divisions are:

Count	Shorthand	Count	Shorthand
50	SSTNSNSNS	20,000	SNDSDNTNT
60	NSNSTSSNT	50,000	SSNNSSDNS
500	DTSNNSSSN	86,400	SNDNTDTSS
1,000	NSTSTNNNN	100,000	TNDNNNSDT
3,600	TDNTTTNDT	150,000	NTNSNTTNT
5.000	TNNTSSSSD	200,000	DNDSDSTNS
10,000	TDSNNNNNS	262,145	NSSSSSSSS

A Fortran program to determine the connections has been included in this data sheet. Other connections can also be obtained by contacting the MOS Marketing group at Fairchild.

FORTRAN PROGRAM

This Fortran program calculates the 3816 inputs required for any given count. The required count should be entered right justified in columns 2 through 7 of data set reference number 5; the 3816 inputs are read in order from data set reference number 6.

```
      DIMENSION L(35),N(19),PRINT(2,2)
      DATA PRINT /'D','N','T','S'/
      WRITE (6,100)
100   FORMAT (1X,'NOTE: D=VDD, S=VSS, T=TC, N=TCN')
110   READ (5,120,END=999) M
120   FORMAT (1X,I6)
      IF (M.GE.3.AND.M.LE.262145) GO TO 140
      WRITE (6,130) M
130   FORMAT (1X,'N=',I6,1X,'IS AN ILLEGAL COUNT')
      GO TO 110
140   K=M+3
      DO 150 I=1,19
      N(I)=K-2*(K/2)
150   K=K/2
      DO 160 I=1,18
160   L(I)=1
      L(2)=-1
      J=20
170   J=J-1
      IF (N(J).EQ.0) GO TO 170
180   J=J-1
      IF (J.EQ.0) GO TO 220
      DO 190 I=1,17
      L (37-2*I)=L(19-I)
190   L(36-2*I)=1
      DO 200 I=1,17
      L(25-I)=L(25-I)*L(36-I)
      L(18-I)=L(18-I)*L(36-I)
200   CONTINUE
      IF (N(J).EQ.0) GO TO 180
      DO 210 I=1,18
210   L(20-I)=L(19-I)
      L(1)=L(19)
      L(8) = L(8) *L(1)
      GO TO 180
220   DO 230 I=1,18
230   L(30-I)=(L(19-I)+3)/2
      DO 240 I=1,11
240   L(I)=L(I+18)
      WRITE (6,250) M,(PRINT(L(19-I),L(18-I)),I=1,17,2)
250   FORMAT (1X,'N=',I6,1X,'INPUTS=',9A1)
      GO TO 110
999   CALL EXIT
      END
```

F4000
SERIES CMOS

GENERAL DESCRIPTION – Fairchild CMOS logic combines popular 4000 series functions with the advanced isoplanar C process. The result is a logic family with a superior combination of noise immunity and standardized drive characteristics. Under static conditions, these devices dissipate very low power, typically 10 nW per gate. The low power combined with the wide (3 to 15 V) recommended operating supply voltage requirement greatly minimizes power supply costs. The CMOS family is designed with standardized output drive characteristics which, combined with relative insensitivity to output capacitance loading, simplify system design.

- **LOW POWER – TYPICALLY 10 nW PER GATE STATIC**
- **WIDE OPERATING SUPPLY VOLTAGE RANGE –**
  3 TO 15 V RECOMMENDED
  18 V ABSOLUTE MAXIMUM
- **HIGH NOISE IMMUNITY**
- **BUFFERED OUTPUTS STANDARDIZE OUTPUT DRIVE AND REDUCE VARIATION OF PROPAGATION DELAY WITH OUTPUT CAPACITANCE**
- **WIDE OPERATING TEMPERATURE RANGE**
  COMMERCIAL -40°C TO +85°C
  MILITARY -55°C TO +125°C
- **HIGH DC FAN OUT – GREATER THAN 50**

ISOPLANAR C

The Fairchild CMOS logic family uses isoplanar C for high performance. This technology combines local oxidation isolation techniques with silicon gate technology to achieve an approximate 35% to 100% savings in area as shown in Figure 1-1a. Operating speeds are increased due to the self-alignment of the silicon gate and reduced sidewall capacitance.

Conventional CMOS circuits are fabricated on an n-type substrate as shown in Figure 1-1b. The p-type substrate required for complementary n-channel MOS is obtained by diffusing a lightly doped p-region into the n-type substrate. Conventional CMOS fabrication requires more chip area and has slower circuit speeds than Isoplanar C CMOS. This is a result of the n+ or p+ channel stop which surrounds the p- or n-channels respectively in conventional metal gate CMOS, Silicon gate CMOS (Figure 1-1c) has a negligible reduction in area, though transient performance is improved.

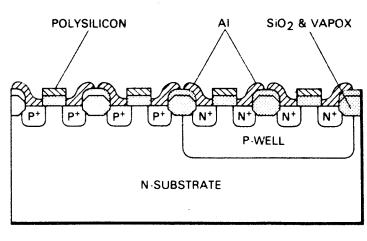


Fig. 1-1a. ISOPLANAR C CMOS STRUCTURE REDUCES AREA 35%

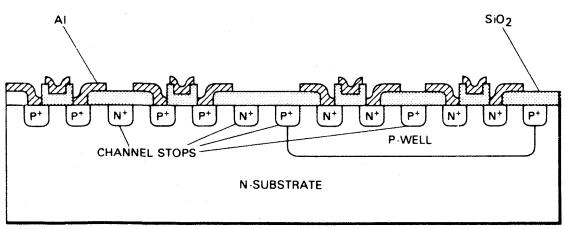


Fig. 1-1b. CONVENTIONAL METAL GATE CMOS STRUCTURE

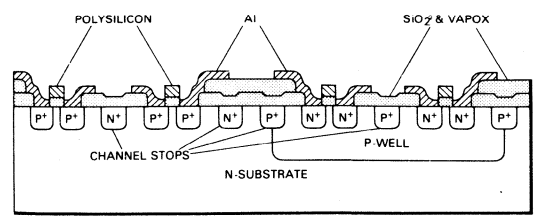


Fig. 1-1c. CONVENTIONAL SILICON GATE CMOS STRUCTURE REDUCES AREA 8%

FULLY BUFFERED CONFIGURATION DESCRIPTION

Fairchild CMOS logic is designed with the system user in mind. Output buffering is used on all devices to achieve high performance, standardized output drive, highest noise immunity and decreased ac sensitivity to output loading. Figure 1-2 illustrates a conventional unbuffered 2-Input NOR Gate. Either n-channel transistor connected to V_{SS} (ground) conducts when either input is HIGH, causing the output to go LOW through the ON resistance of the device. If both inputs are HIGH, both n-channel devices are on; effectively halving the ON resistance, thereby making the output impedance (and hence fall time) a function of input variables. Similarly the p-channel devices are switched on by LOW signals; i.e., when both inputs are LOW, conduction from V_{DD} to the output will occur.

Since the p-channel devices are in series, their ON resistance must be decreased (larger chip area) to hold output HIGH impedance within specification. As the number of gate inputs increases, even larger p-channel devices are required, and the output impedance to V_{SS} becomes even more pattern sensitive.

A conventional unbuffered CMOS 2-Input NAND Gate interchanges the parallel and serial transistor gating to achieve the NAND function (Figure 1-3). The changes in output resistance then move to the p-channel transistors connected to V_{DD}, while the n-channel devices must be increased in size due to their serial connection.

Fairchild CMOS uses small geometry logic transistors to generate the required function which drive standard low impedance output buffers (Figures 1-4 and 5). This technique reduces chip size, since only two large output transistors are required and rise and fall times are independent of input pattern. Buffered outputs also increase system speeds and make propagation delay less sensitive to output capacitance. Figure 1-6 illustrates typical propagation delay vs. output capacitance for conventional and buffered CMOS Gates.

Another advantage of the Fairchild approach is improved noise immunity. Because of the increased voltage gain, nearly ideal transfer characteristics are realized as shown in Figure 1-7. The high gain (greater than 10,000) also provides significant pulse shaping; the waveforms of Figures 1-8 and 9 compare the output waveforms of conventional and buffered CMOS gates. For input transition times of 100 ns or less, the outputs of both gate types are similar. When the input transitions are stretched to one microsecond, the conventional gate exhibits increased transition times while the buffered gate has unchanged output transition times. This feature eliminates progressive deterioration of pulse characteristics in a system. The combination of Isoplanar C and buffered outputs results in new standards of CMOS logic performance.

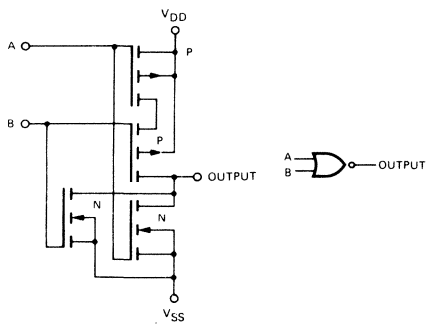


Fig. 1-2. CONVENTIONAL NON-BUFFERED 2-INPUT NOR GATE

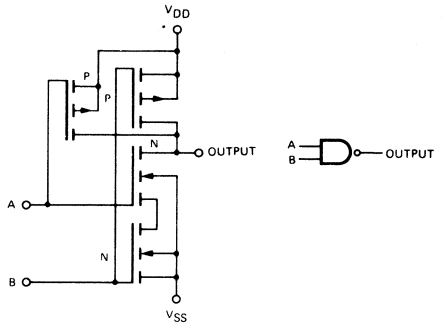


Fig. 1-3. CONVENTIONAL NON-BUFFERED 2-INPUT NAND GATE

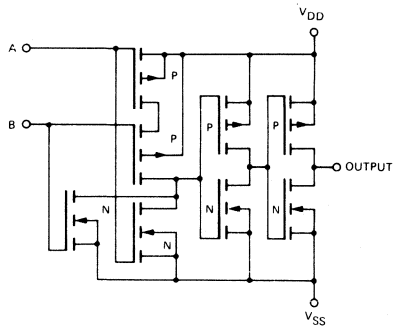


Fig. 1-4. FAIRCHILD F4001 FULLY BUFFERED NOR GATE

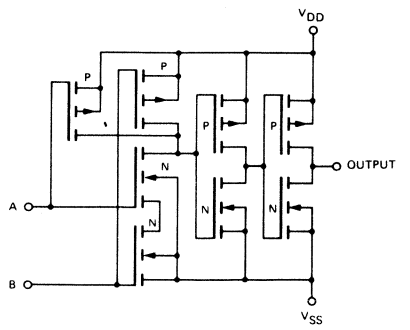


Fig. 1-5. FAIRCHILD F4011 FULLY BUFFERED NAND GATE

Fig. 1-6
COMPARISON OF PROPAGATION DELAY VS LOAD CAPACITANCE FOR CONVENTIONAL AND FULLY BUFFERED NAND GATES

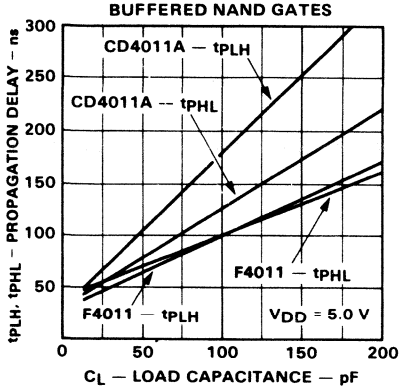


Fig. 1-7
TYPICAL VOLTAGE TRANSFER CHARACTERISTICS FOR CONVENTIONAL AND FULLY BUFFERED DEVICES

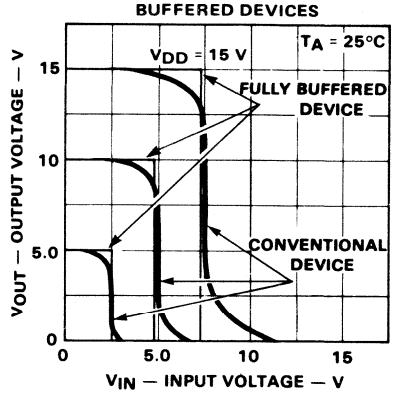


Fig. 1-8
POSITIVE-GOING INPUT RAMPS OF 0.1 μs AND 1.0 μs APPLIED TO CONVENTIONAL AND FULLY BUFFERED GATES

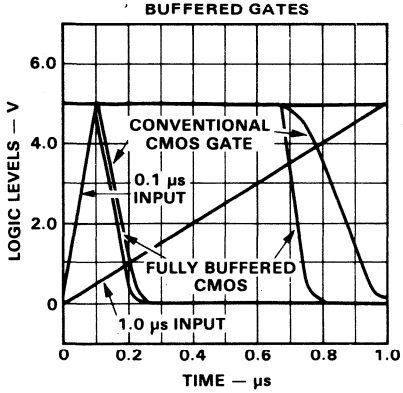
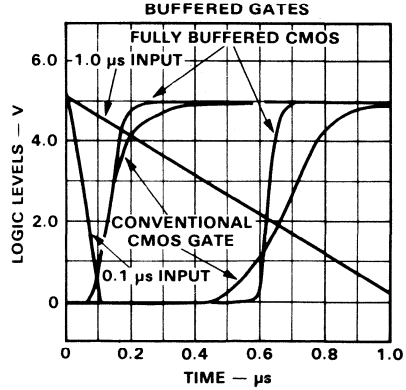


Fig. 1-9
NEGATIVE-GOING INPUT RAMPS OF 0.1 μs AND 1.0 μs APPLIED TO CONVENTIONAL AND FULLY BUFFERED GATES



DESIGN CONSIDERATIONS WITH F4000 SERIES CMOS

INTRODUCTION

Complementary MOS digital logic building blocks of SSI and MSI complexity have been hailed as the ideal logic family. They are rapidly gaining popularity as more and more manufacturers introduce increasing numbers of parts at reasonable prices.

Originally designed for aerospace applications, CMOS now finds its way into portable instruments, industrial and medical electronics, automotive applications and computer peripherals, besides dominating the electronic watch market.

In late 1973, Fairchild introduced the F4000 CMOS family, using Isoplanar technology to achieve superior electrical performance. Most of these devices are functional equivalents and pin-for-pin replacements of the well-known 4000 series; some are equivalent to TTL circuits and some are proprietary logic designs.

A few CMOS devices, such as bidirectional analog switches, exploit the unique features of CMOS technology; some take advantage of the smaller device size and higher potential packing density to achieve true LSI complexity; but most of the available CMOS elements today are of SSI and MSI complexity and perform logic functions that have been available in DTL or TTL for many years. Therefore, it is both helpful and practical to compare the performance of CMOS with that of the more familiar DTL/TTL *(Figure 2-1)*. The TTL to CMOS Comparison Guide in Section 3 lists numerous CMOS circuits that are pinout identical to their TTL counterparts, others that are functionally identical only, still others that are similar and, in most cases, offer added features.

CMOS speed is comparable to 74L-TTL and DTL, and about three to six times slower than TTL or Low Power Schottky (LS-TTL). Voltage noise immunity and fan out are almost ideal, supply voltage is noncritical, and the quiescent power consumption is close to zero-several orders of magnitude lower than for any competing technology.

POWER CONSUMPTION

Under static conditions, the p-channel (top) and the n-channel (bottom) transistors are not conducting simultaneously, thus only leakage current flows from the positive (V_{DD}) to the negative (V_{SS}) supply connection. This leakage current is typically 0.5 nA per gate, resulting in very attractive low power consumption of 2.5 nW per gate (at 5 V).

Whenever a CMOS circuit is exercised, when data or clock inputs change, additional power is consumed to charge and discharge capacitances (on-chip parasitic capacitances as well as load capacitances). Moreover, there is a short time during the transition when both the top and the bottom transistors are partially conducting. This dynamic power consumption is

PARAMETER	STANDARD TTL	74L	DTL	LOW POWER SCHOTTKY	F4000 CMOS 5 V SUPPLY	F4000 CMOS 10 V SUPPLY
PROPAGATION DELAY	10 ns	33 ns	30 ns	5 ns	40 ns	20 ns
FLIP-FLOP TOGGLE FREQUENCY	35 MHz	3 MHz	5 MHz	45 MHz	8 MHz	16 MHz
QUIESCENT POWER	10 mW	1 mW	8.5 mW	2 mW	10 nW	10 nW
NOISE IMMUNITY	1 V	1 V	1 V	0.8 V	2 V	4 V
FAN OUT	10	10	8	20	50*	50*

*OR AS DETERMINED BY ALLOWABLE PROPAGATION DELAY

Fig. 2-1 CMOS COMPARED TO OTHER LOGIC FAMILIES

obviously proportional to the frequency at which the circuit is exercised, to the load capacitance and to the square of the supply voltage. As shown in *Figure 2-2,* the power consumption of a CMOS gate exceeds that of a Low Power Schottky gate somewhere between 500 kHz and 2 MHz of actual output frequency.

At 100 transitions per second, the dynamic power consumption is far greater than the static dissipation; at one million transitions per second, it exceeds the power consumption of LS-TTL. Comparing the power consumption of more complex devices (MSI) in various technologies may show a different result. In any complex design, only a small fraction of the gates actually switch at the full clock frequency, most gates operate at a much lower average rate and consume, therefore, much less power.

A realistic comparison of power consumption between different technologies involves a thorough analysis of the average switching speed of each gate in the circuit. The small static supply current, I_{DD} is specified on individual data sheets for 5, 10 and 15 V. The dynamic power dissipation for 5, 10 and 15 V, 15 and 50 pF may be found in graph form for frequencies of 100 Hz to 10 MHz. The total power may be calculated, $P_T = (I_{DD} \times V_{DD}) +$ dynamic power dissipation.

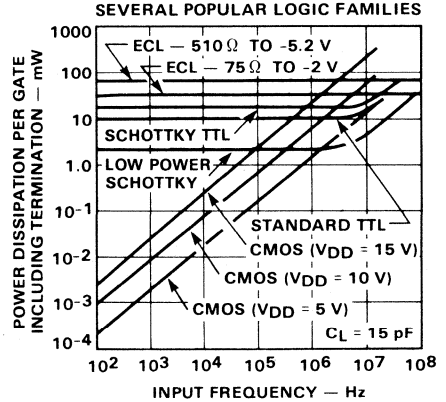
SUPPLY VOLTAGE RANGE

CMOS is guaranteed to function over the unprecedented range of 3 to 15 V supply voltage. Characteristics are guaranteed for 5, 10 and 15 V operation and can be extrapolated for any voltage in between. Operation below 4.5 V is not very meaningful because of the increase in delay (loss of speed), the increase in output impedance and the loss of noise immunity. Operation above 15 V is not recommended because of high dynamic power consumption and risk of noise spikes on the power supply exceeding the breakdown voltage (typ >20 V), causing SCR-latch-up and destroying the device unless the current is externally limited.

The lower limit of power supply voltage, including ripple, is determined by the required noise immunity, propagation delay or interface to TTL. The upper limit of supply voltage, including ripple and transients, is determined by power dissipation or direct interface to TTL. The F4049, F4050 and F4104 provide level translation between TTL and CMOS when CMOS supply voltages over 5 V are used. While devices are usable to 18 V, operation above 12 V is discouraged for reasons of power dissipation.

Low static power consumption combined with wide supply voltage range make CMOS the ideal logic family for battery operated equipment.

Fig. 2-2
TYPICAL POWER DISSIPATION VERSUS INPUT FREQUENCY FOR SEVERAL POPULAR LOGIC FAMILIES



PROPAGATION DELAY

Compared to TTL and LS-TTL, all CMOS devices are slow and very sensitive to capacitive loading. See *Figure 2-3.* The Fairchild F4000 family uses both advanced processing (Isoplanar) and improved circuit design (buffered gates) to achieve propagation delays and output rise times that are superior to any other junction-isolated CMOS design. (Silicon-on-sapphire, SOS, can achieve similar performance but at a substantial cost penalty).

Isoplanar processing achieves lower parasitic capacitances which reduce the on-chip delay and increase the maximum toggle frequency of flip-flops, registers and counters. Buffering all outputs, even on gates, results in lower output impedance and thus reduces the effect of capacitive loading.

Propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

Capacitive Loading Effect

Historically, semiconductor manufacturers have always specified the propagation delay at an output load of 15 pF, not because anybody considers this a representative systems environment, but rather because it was the lowest practical test-jig capacitance. It also generated the most impressive specifications. TTL with an output impedance less than 100 Ω is little affected by an increase in capacitive loading; a 100 pF load increases the delay by only about 4 ns. CMOS, however, with an output impedance of 1 kΩ (worst case at 5 V) is 10 times more sensitive to capacitive loading. *Figure 2-4* shows the positive- and negative-going delays as a function of load capacitance. It should be noted that the older, unbuffered gates have an even higher output impedance, a larger dependence on output loading, and do not show the same symmetry.

Fig. 2-3
NORMALIZED PROPAGATION DELAY VERSUS LOAD CAPACITANCE FOR TTL AND CMOS

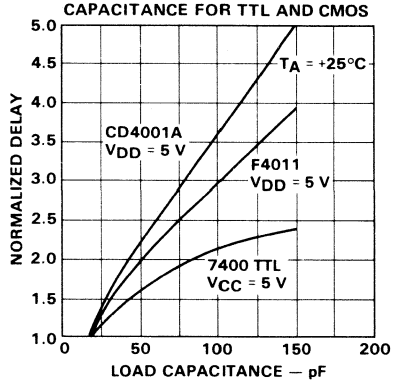


Fig. 2-4a
POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

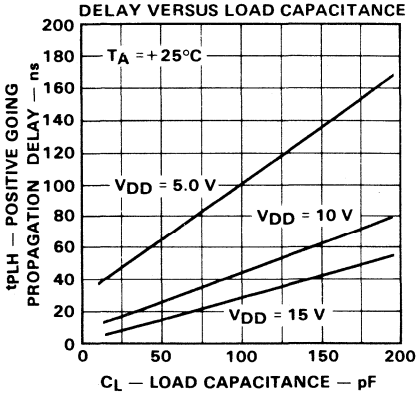
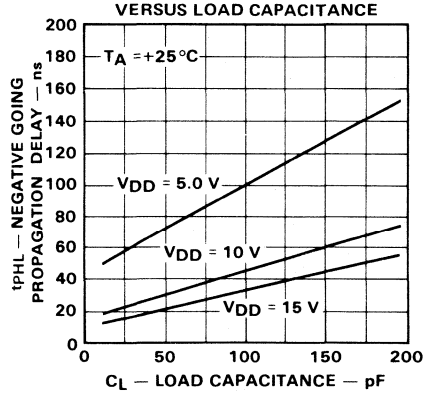


Fig. 2-4b
NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE



Supply Voltage Effect

Figure 2-5 shows propagation delay as a function of supply voltage and again indicates the symmetry of the positive- and negative-going delays. Increasing the supply voltage from 5 to 10 V more than doubles the speed of CMOS gates. Increasing the supply voltage to 15 V almost doubles the speed again, but, as mentioned before, results in a significant increase in dynamic power dissipation.

The best choice for slow applications is 5 V. For reasonably fast systems, choose 10 or 12 V. Any application requiring 15 V to achieve short delays and fast operation should be investigated for excessive power dissipation and should be weighed against an LS-TTL approach.

Fig. 2-5a
POSITIVE-GOING PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE

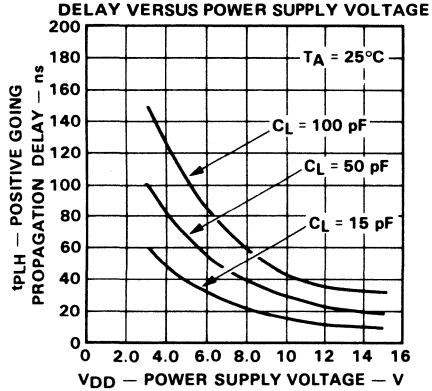
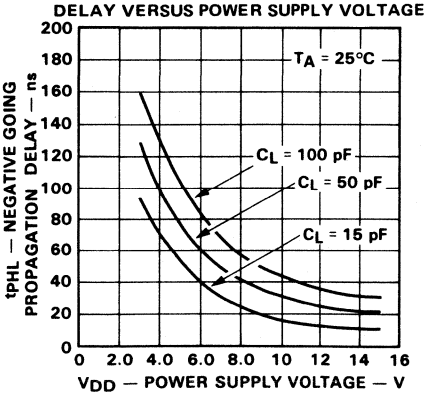


Fig. 2-5b
NEGATIVE-GOING PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



Temperature Effect

Figure 2-6 shows propagation delay as a function of ambient temperature. The temperature dependence of CMOS is much simpler than with TTL, where three factors contribute—increase of beta with temperature, increase of resistor value with temperature, and decrease of junction forward voltage drop with increasing temperature. In CMOS, essentially only the carrier mobility changes, thus increasing the impedance and hence the delay with temperature. For F4000 devices, this temperature dependence is less than 0.3% per °C, practically linear over the full temperature range. Note that the commercial temperature range is −40 to +85°C rather than the usual 0 to +75°C.

Fig. 2-6a
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE WITH V_{DD} = 5 V

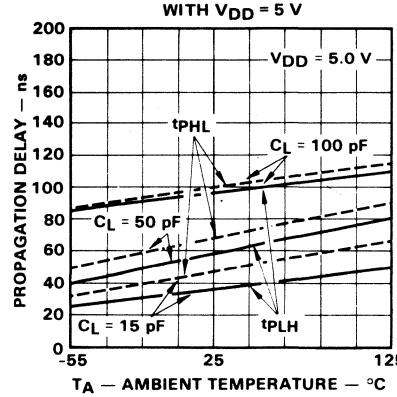
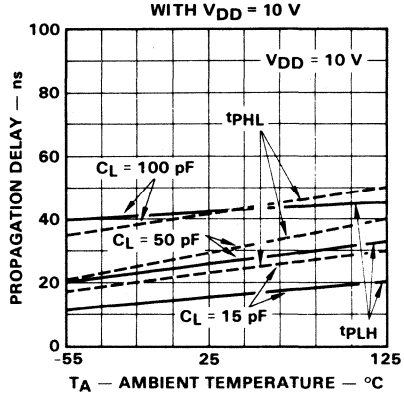


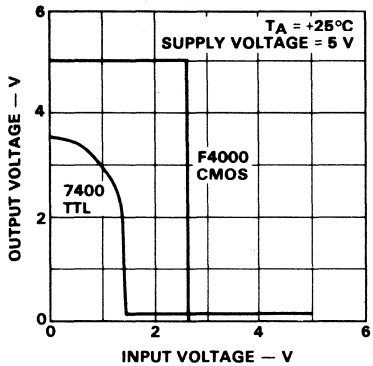
Fig. 2-6b
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE WITH V_{DD} = 10 V



CMOS delays increase with temperature. They are very sensitive to capacitive loading but can be reduced by increasing the supply voltage to 10 or even 15 V.

To determine propagation delays, the effects of capacitive loading, supply voltage, manufacturing tolerances and ambient temperature must be considered. Start with the values of t_{PLH} (propagation delay, a LOW-to-HIGH output transition) and t_{PHL} (propagation delay, a HIGH-to-LOW output transition) given in the individual data sheets. Delay values for V_{DD} at 5, 10 and 15 V and output capacity of 15 and 50 pF are provided. Manufacturing tolerances account for the differences between MIN, TYP and MAX. Starting with the nearest applicable delay value, correct for effects of capacitive loading, ambient temperature and supply voltage using the general family characteristics of Section 3.

Fig. 2-7
TYPICAL TRANSFER CHARACTERISTICS FOR TTL AND CMOS



NOISE IMMUNITY

One of the most advertised and also misunderstood CMOS features is noise immunity. The input threshold of a CMOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, CMOS can claim very good voltage noise immunity, typically 45% of the supply voltage, *i.e.*, 2.25 V in a 5 V system, 4.5 V in a 20V system. Compare this with the TTL transfer curve in *Figure 2-7* and its resultant 1 V noise immunity in a lightly loaded system and only 0.4 V worst case.

Since CMOS output impedance, output voltage and input threshold are symmetrical with respect to the supply voltage, the LOW and HIGH level noise immunities are practically equal. Therefore, a CMOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1 V, even in a 5 V system. Moreover, the inherent CMOS delays act as a noise filter; 10 ns spikes tend to disappear in a chain of CMOS gates, but are amplified in a chain of TTL gates. Because of these features, CMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically "polluted" environment.

Unfortunately these impressive noise margin specifications disregard one important fact: the output impedance of CMOS is 10 to 100 times higher than that of TTL. CMOS interconnections are therfore less "stiff" and much more susceptible to capacitively coupled noise. In terms of such current injected crosstalk from high noise voltages through small coupling capacitances, CMOS has about six times *less* noise margin than TTL. It takes more than 20 mA to pull a TTL output into the threshold region, but it takes only 3 mA to pull a CMOS output into the threshold of a 5 V system.

The nearly ideal transfer characteristic and the slow response of CMOS circuits make them insensitive to low voltage, magnetically coupled noise. The high output impedance, however, results in a poor rejection of capacitively coupled noise.

INTERFACE TO TTL

When CMOS is operated with a 5 V power supply, interface to TTL is straightforward. The input impedance of CMOS is very high, so that any form of TTL will drive CMOS without loss of fan out in the LOW state. Unfortunately, most TTL has insufficient HIGH state voltage (typically 3.5 V) to drive CMOS reliably. A pull up resistor (1 kΩ to 10 kΩ) from the output of the TTL device to the 5 V power supply will effectively pull the HIGH state level to 4.5 V or above. Alternately, DTL Hex inverters may be used between the TTL and CMOS. 9LS Low Power Schottky and 93L00 Low Power TTL/MSI utilize the unique output configuration shown in *Figure 2-8* to pull its output to $V_{CC}-V_{BC}$ or approximately 4.3 V when lightly loaded.

All F4000 logic elements will drive a single 9LS Low Power Schottky input fan in directly. A 9LS Hex inverter such as the 9LS04 makes an excellent low cost TTL buffer with a fan out of 20 into 9LS or 5 into standard TTL. Alternately, the F4049 and F4050 Hex buffers may be used to drive a fan out of 8 into 9LS or 2 into standard TTL.

When operating CMOS at voltages higher than 5 V, direct interface to TTL cannot be used. The F4104 Quad Level Translator converts TTL levels to high voltage CMOS up to 15 V. The F4049 and F4050 Hex Buffers will accept high voltage CMOS levels up to 15 V and drive 2 standard TTL loads.

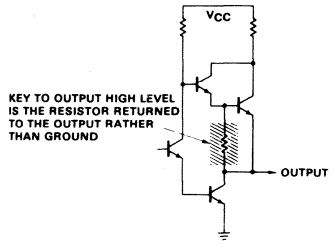


Fig. 2-8
THE 93L00 AND 9LS00 TTL FAMILIES WILL DRIVE CMOS DIRECTLY WITHOUT RESISTORS AS LONG AS THERE ARE ONLY CMOS DEVICES BEING DRIVEN FROM THE OUTPUT.

INPUT/OUTPUT CAPACITY

CMOS devices exhibit input capacities in the 1.5 to 5 pF range and output capacity in the 3 to 7 pF range.

OUTPUT IMPEDANCE

All F4000 logic devices employ standardized output buffers. Section 3 details output characteristics. It should be noted that these impedances do not change with input pattern as do conventional CMOS gates. Buffers, analog switches and analog multiplexers employ special output configurations which are detailed in individual data sheets.

INPUT PROTECTION

The gate input to any MOS transistor appears like a small (<1 pF) very low leakage ($<10^{-12}$ A) capacitor. Without special precautions, these inputs could be electrostatically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all CMOS inputs are protected by a combination of series resistor and shunt diodes. Various manufacturers have used different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

Each member of the F4000 family utilizes a series resistor, nominally 200 Ω, and two diodes, one to V_{DD}, and the other to V_{SS} *(Figure 2-9)*. The resistor is a poly-silicon "true resistor" without a parasitic substrate diode. This ensures that the input impedance is always at least 200 Ω under all biasing conditions, even when V_{DD} is short circuited to V_{SS}. A parasitic substrate diode would represent a poorly defined shunt to V_{SS} in this particular case.

The diodes exhibit typical forward voltage drops of 0.9 V at 1 mA and reverse breakdowns of 20 V for D1 and 20 V for D2. For certain special applications such as oscillators, the diodes actually conduct during normal operation. However, currents must be limited to 10 mA.

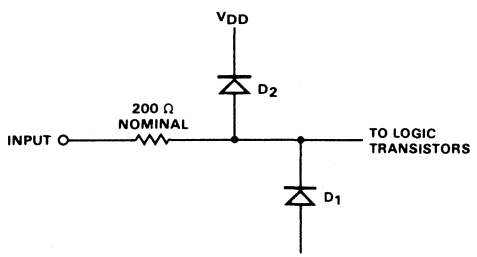


Fig. 2-9
F4000 SERIES CMOS
INPUT PROTECTION CIRCUIT

HANDLING PRECAUTIONS

All MOS devices are subject to damage by large electrostatic charges. All F4000 devices employ the input protection described in *Figure 2.9*, however, electrostatic damage can still occur. The following handling precautions should be observed.

1. All F4000 devices are shipped in conducting foam or tubes. They should be removed for inspection or assembly using proper precautions.
2. Ionized air blowers are recommended when automatic incoming inspection is performed.
3. F4000 devices, after removal from their shipping material, should be placed leads down on a grounded surface. Conventional cookie tins work well. Under no circumstances should they be placed in polystyrene foam or plastic trays used for shipment and handling of conventional ICs.
4. Individuals and tools should be grounded before coming in contact with F4000 devices.
5. Do not insert or remove devices in sockets with power applied. Ensure power supply transients, such as occur during power turn-on or off; do not exceed maximum ratings.
6. In the system, all unused inputs must be connected to either a logic HIGH or logic LOW level such as V_{SS}, V_{DD} or the output of a logic element.
7. After assembly on PC boards, ensure that static discharge cannot occur during storage or maintenance. Boards may be stored with their connectors surrounded with conductive foam. Board input/output pins may be protected with large value resistors (10 MΩ) to ground.
8. In extremely hostile environments, an additional series input resistor (10 to 100 kΩ) provides even better protection at a slight speed penalty.

A WORD TO THE TTL DESIGNER

Designing with CMOS is generally an easy transition and allows the designer to discard many of the old design inhibitions for new found freedoms. A few of these are:

Fan out—It is practically unlimited from a dc point of view and is restricted only by delay and rise time considerations.

Power Supply Regulation—Anything between 3 V and 15 V goes, as long as all communicating circuits are fed from the same voltage.

Ground and V_{CC} Line Drops—The currents are normally so small that there is no need for heavy supply line bussing.

V_{CC} Decoupling—It can be reduced to a few capacitors per board.

Heat Problems—They do not exist, unless an attempt is made to run CMOS very fast and from more than 10 V.

It should also be noted that there are a few warnings called for when designing with CMOS and that many of the hard-earned good engineering basics cannot be forgotten. A few of the new design challenges include:

Unused Inputs—They must be connected to V_{SS} or V_{DD} (V_{CC} or ground) lest they generate a logical "maybe". The bad TTL habit of leaving unused inputs open is definitely out.

Oscillations—Slowly rising or falling input signals can lead to oscillations and multiple triggering. A poorly regulated and decoupled power supply magnifies this problem since the CMOS input threshold varies with the supply voltage.

Timing Details—Even slow systems require a careful analysis of worst case timing delays, derated for maximum temperature, minimum supply voltage and maximum capacitive loading. Many CMOS flip-flops, registers and latches have a real hold time requirement, *i.e.*, inputs must remain stable even after the active clock edge; some require a minimum clock rise time. This hasn't been a problem with TTL. CMOS systems, even slow ones, are prone to unsuspected clock skew problems, especially since a heavily loaded clock generator can have a poor rise time.

Compatibility—The TTL designer knows that devices sold by different manufacturers under the same generic part number are electrically almost identical. The same electrical compatibility is not yet achieved in CMOS. Many semiconductor houses manufacture 4000-type devices with wide variations in output drive capability and speed. Sometimes even the functions are different and incompatible; two cases in point are the 1-of-10 decoder (CD4028A and MC14028) and the magnitude comparator (MC14585 and MM74C85).

Data Sheet Format—The original CD4000 series data sheets may appear confusing to the TTL user because a range of input voltage requirements is not specified. Rather, this information is contained in a "noise immunity" specification and is not immediately obvious.

Both TTL and CMOS tolerate deviations from the ideal LOW and HIGH input voltages. TTL is therefore specified as follows:

	MIN	MAX	
V_{IH}	2.0		V
V_{IL}		0.8	V

Any voltage below 0.8 V is considered LOW; any voltage above +2.0 V is considered HIGH. The actual threshold is somewhere in between these values, depending on manufacturing tolerances, supply voltage, and temperature.

Fairchild's F4000 CMOS is specified in a similar way. For $V_{DD} = 5$ V;

	MIN	MAX	
V_{IH}	3.5		V
V_{IL}		1.5	V

The CD4000 data sheets, on the other hand, do not call out V_{IH} and V_{IL} but specify a "noise immunity" which is somewhat arbitrarily defined relative to the appropriate supply voltage.

$$V_{NL} = V_{IL}$$
$$V_{NH} = V_{DD} - V_{IH}$$

For $V_{DD} = 5$ V, therefore
$V_{NL} = 1.5$ V min is equivalent to $V_{IL} = 1.5$ V max
$V_{NH} = 1.4$ V min is equivalent to $V_{IH} = 3.6$ V min, etc.

Systems Oriented MSI—Available CMOS circuits, especially the original 4000 series, are not as well suited for synchronous systems as are the 9300/7400 TTL families. Control polarities are inconsistent; many circuits cannot be cascaded or extended synchronously without additional gates, etc. This will improve as more good synchronous building blocks, like the F40160 are introduced.

SELECTOR GUIDE BY FUNCTION

SELECTOR GUIDE BY FUNCTION

Counters (Cont'd)

Registers

Decoders and Demultiplexers

Digital Multiplexers

Analog Switches and Multiplexers/Demultiplexers

Latches

Translators

Arithmetic Operators

SELECTOR GUIDE BY FUNCTION

Arithmetic Operators (Cont'd)

Memories

Frequency Generator

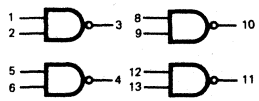
Multivibrators, Phase-Locked Loops

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			NAND GATES	
7400 9002	Quad 2-Input NAND Gate	F4011	Different Pinout, Functionally Identical	4-52
7410 9003	Triple 3-Input NAND Gate	F4023	Different Pinout, Functionally Identical	4-77
7420 9004	Dual 4-Input NAND Gate	F4012	Different Pinout, Functionally Identical	4-52
7430 9007	8-Input NAND Gate	F4068	Different Pinout, Functionally Identical	4-128
			AND GATES	
7408	Quad 2-Input AND Gate	F4081	Different Pinout, Functionally Identical	4-140
74LS11	Triple 3-Input AND Gate	F4073	Different Pinout, Functionally Identical	4-134
74LS21	Dual 4-Input AND Gate	F4082	Different Pinout, Functionally Identical	4-141
			NOR GATES	
7402	Quad 2-Input NOR Gate	F4001	Different Pinout, Functionally Identical	4-44
7427	Triple 3-Input NOR Gate	F4025	Different Pinout, Functionally Identical	4-81
7425	Dual 4-Input NOR Gate	F4002	Different Pinout. The 7425 has a Strobe input on each gate; the F4002 does not.	4-44
	8-Input NOR Gate	F4078	No TTL Equivalent	4-138
			OR GATES	
7432	Quad 2-Input OR Gate	F4071	Different Pinout, Functionally Identical	4-132
	Triple 3-Input OR Gate	F4075	No TTL Equivalent	4-135
	Dual 4-Input OR Gate	F4072	No TTL Equivalent	4-133
			INVERTERS AND BUFFERS	
7404 9016	Hex Inverter	F4069	Same Pinout, Functionally Identical	4-129
7416 7404 9016	Hex Buffer, Inverting	F4049	Different Pinout. The F4049 has an active pull-up and pull-down output. The 7416 has an open collector output. The 7404 and 9016 have an active pull-up and pull-down output.	4-114
7417	Hex Buffer, Non-Inverting	F4050	Different Pinout. The F4050 has an active pull-up and pull-down output. The 7417 has an open collector output.	4-114
74367 8097	Hex Buffer, Non-Inverting, 3-State Outputs	F40097	Same Pinout, Functionally Identical	4-259
74368 8098	Hex Buffer, Inverting, 3-State Outputs	F40098	Same Pinout, Functionally Identical	4-259
	Dual Complementary Pair Plus Inverter	F4007	No TTL Equivalent	4-48
	Quad True/ Complement Buffer	F4041	No TTL Equivalent	4-101

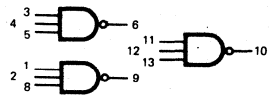
TTL TO CMOS FUNCTION SELECTOR GUIDE

F4011



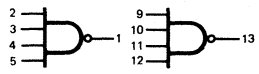
V_{DD} = Pin 14
V_{SS} = Pin 7

F4023



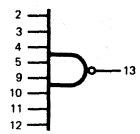
V_{DD} = Pin 14
V_{SS} = Pin 7

F4012



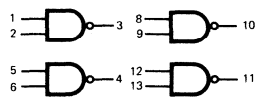
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 6, 8

F4068



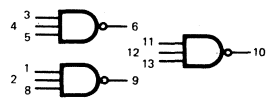
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

F4081



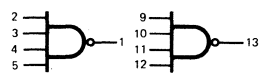
V_{DD} = Pin 14
V_{SS} = Pin 7

F4073



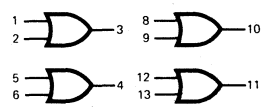
V_{DD} = Pin 14
V_{SS} = Pin 7

F4082



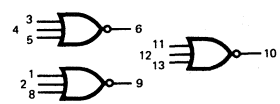
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 6, 8

F4001



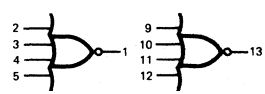
V_{DD} = Pin 14
V_{SS} = Pin 7

F4025



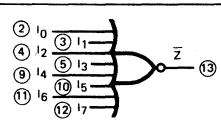
V_{DD} = Pin 14
V_{SS} = Pin 7

F4002



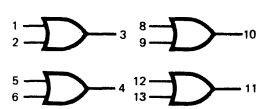
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 6, 8

F4078



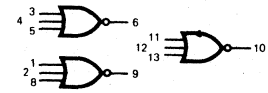
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

F4071



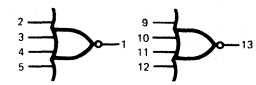
V_{DD} = Pin 14
V_{SS} = Pin 7

F4075



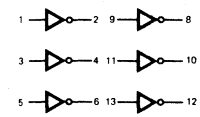
V_{DD} = Pin 14
V_{SS} = Pin 7

F4072



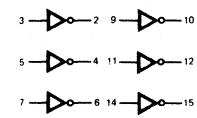
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 6, 8

F4069



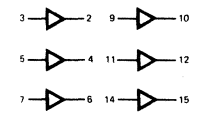
V_{DD} = Pin 14
V_{SS} = Pin 7

F4049



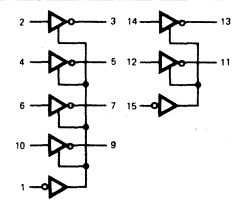
V_{DD} = Pin 1
V_{SS} = Pin 8
NC = Pins 13, 16

F4050



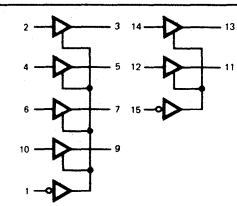
V_{DD} = Pin 1
V_{SS} = Pin 8
NC = Pins 13, 16

F40097



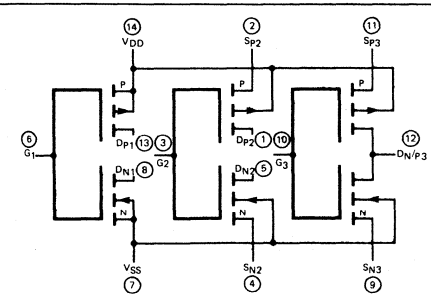
V_{DD} = Pin 16
V_{SS} = Pin 8

F40098

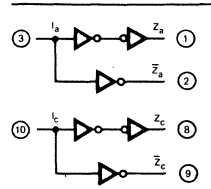


V_{DD} = Pin 16
V_{SS} = Pin 8

F4007



F4041



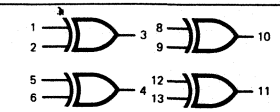
V_{DD} = Pin 14
V_{SS} = Pin 7

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			COMPLEX GATES	
74L86	Quad Exclusive-OR Gate	F4030/ F4070	Same Pinout, Functionally Identical	4-92 4-131
74LS266	Quad Exclusive-NOR Gate	F4077	Same Pinout, Functionally Identical	4-137
7450 9005	Dual 2-Wide, 2-Input AND-OR-INVERT Gate	F4085	Different Pinout. The F4085 has an extra input which can be used as either an expander input or an inhibit input by connecting it to any standard CMOS output. Only one-half of a 7450 and 9005 can be expanded by connecting ti to a special expander circuit. The 7450 and 9005 do not have an inhibit capability.	4-142
7453	4-Wide, 2-Input AND-OR-INVERT Gate	F4086	Different Pinout. The F4086 has two additional inputs which can be used as either expander inputs or inhibit inputs by connecting them to any standard CMOS output. The 7453 can be expanded only by connecting it to a special expander circuit. The 7453 does not have an inhibit capability.	4-144
			FLIP-FLOPS	
7474	Dual D Flip-Flop	F4013	Different Pinout. The 7474 has active LOW S_D and C_D inputs; the F4013 has active HIGH S_D and C_D inputs.	4-54
74109 9024	Dual JK Flip-Flop, Edge-Triggered	F4027	Different Pinout. The 74109 and 9024 have active LOW S_D, C_D, and K inputs; the F4027 has active HIGH S_D, C_D and K inputs.	4-82
74175	Quad D Flip-Flop	F40175	Same Pinout, Functionally Identical	4-272
74173	Quad D Flip-Flop With 3-State Outputs	F4076	Same Pinout, Functionally Identical	4-136
74174	Hex D Flip-Flop	F40174	Same Pinout, Functionally Identical	4-269
			COUNTERS	
93S10 9310 74160	Synchronous, BCD Up Counter, Asynchronous Master Reset	F40160	Same Pinout. The F40160 and 93S10 are fully edge-triggered. The 74160 and 9310 are "opposite state catching" on the Count Enable and Parallel Enable inputs. The Terminal Count is fully decoded on the F40160, 9310 and 93S10 ($TC = CET \bullet Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$); but is not fully decoded on the 74160 ($TC = CET \bullet Q_0 \bullet Q_3$). For the count sequence above 9, the F40160 is the same as the 74160, different than the 9310 and 93S10.	4-263
93S16 9316 74161	Synchronous, Binary Up Counter, Asynchronous Master Reset	F40161	Same Pinout. The F40161 is fully edge-triggered; the 74161 and 9316 are "opposite state catching" on the Count Enable and Parallel Enable inputs. The F40161 is functionally identical to the 93S16.	4-263
74162	Synchronous, BCD Up Counter, Synchronous Reset	F40162	Same Pinout. The F40162 is fully edge-triggered and the Terminal Count is fully decoded ($TC = CET \bullet Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$); the 74162 is "opposite state catching" on the Count Enable, Parallel Enable and Synchronous Reset inputs and the Terminal Count is not fully decoded ($TC = CET \bullet Q_0 \bullet Q_3$).	4-263
74163	Synchronous Binary Up Counter, Synchronous Reset	F40163	Same Pinout. The F40163 is fully edge-triggered; the 74163 is "opposite state catching" on the Count Enable, Parallel Enable and Synchronous Reset inputs.	4-263
74490	Dual BCD Up Counter	F4518	Different Pinout. The F4518 has two clock inputs per counter and is fully synchronous internally. The 74490 has a single clock input per counter, has a "set to nine" input and is a ripple counter internally.	4-169
74393	Dual Binary Up Counter	F4520	Different Pinout. The F4520 has two clock inputs per counter and is fully synchronous internally. The 74393 has a single clock input per counter and is internally organized as a ripple counter.	4-173
	Programmable 4-Bit BCD Down Counter	F4522	No TTL Equivalent	4-175
	Programmable 4-Bit Binary Down Counter	F4526	No TTL Equivalent	4-175

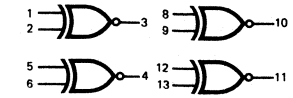
TTL TO CMOS FUNCTION SELECTOR GUIDE

F4030 AND F4070



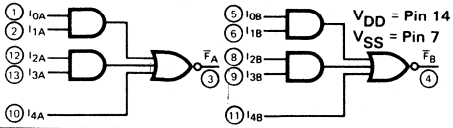
V_{DD} = Pin 14
V_{SS} = Pin 7

F4077



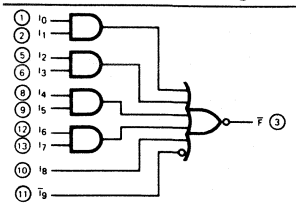
V_{DD} = Pin 14
V_{SS} = Pin 7

F4085



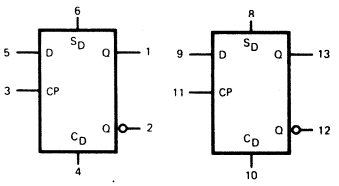
V_{DD} = Pin 14
V_{SS} = Pin 7

F4086



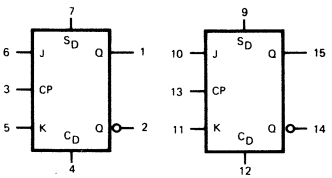
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 4

F4013



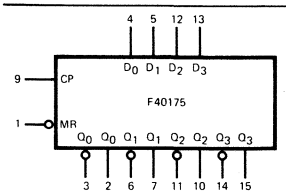
V_{DD} = Pin 14
V_{SS} = Pin 7

F4027



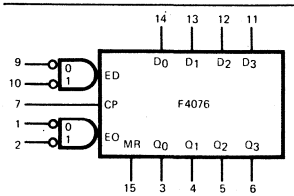
V_{DD} = Pin 16
V_{SS} = Pin 8

F40175



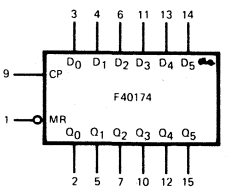
V_{DD} = Pin 16
V_{SS} = Pin 8

F4076



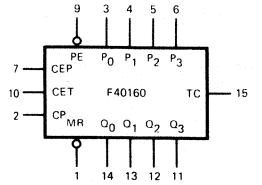
V_{DD} = Pin 16
V_{SS} = Pin 8

F40174



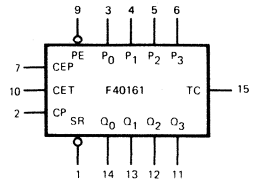
V_{DD} = Pin 16
V_{SS} = Pin 8

F40160



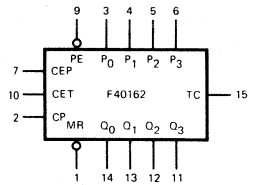
V_{DD} = Pin 16
V_{SS} = Pin 8

F40161



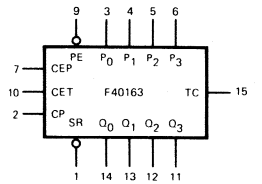
V_{DD} = Pin 16
V_{SS} = Pin 8

F40162



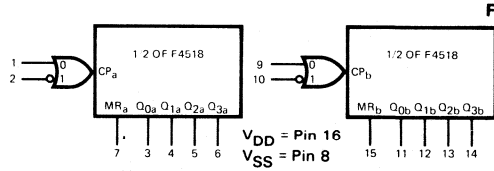
V_{DD} = Pin 16
V_{SS} = Pin 8

F40163



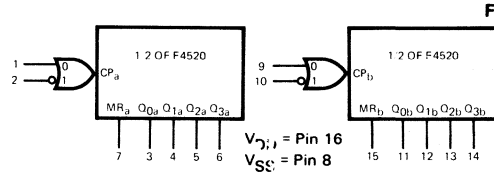
V_{DD} = Pin 16
V_{SS} = Pin 8

F4518



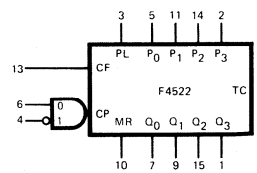
V_{DD} = Pin 16
V_{SS} = Pin 8

F4520



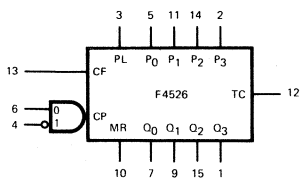
V_{DD} = Pin 16
V_{SS} = Pin 8

F4522



V_{DD} = Pin 16
V_{SS} = Pin 8

F4526



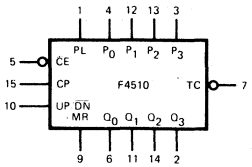
V_{DD} = Pin 16
V_{SS} = Pin 8

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			COUNTERS (Cont'd)	
74190	Up/Down Decade Counter	F4510	Different Pinout. The F4510 is fully edge-triggered, has an active HIGH Parallel Load input, and active HIGH Master Reset input, an Up/$\overline{\text{Dn}}$ input, and an active LOW Terminal Count output which is enabled only if $\overline{\text{CE}}$ = LOW. The 74190 is not fully edge-triggered, has an active LOW Parallel Load input, no Master Reset input, an $\overline{\text{Up}}$/Dn input and an active HIGH Terminal Count output which is independent of $\overline{\text{CE}}$. The 74190 has a Ripple Clock output in lieu of a Master Reset input.	4-149
74191	Up/Down Binary Counter	F4516	Different Pinout. The F4516 is fully edge-triggered, has an active HIGH Parallel Load input, and active HIGH Master Reset input, an Up/$\overline{\text{Dn}}$ input, and an active LOW Terminal Count output which is enabled only if $\overline{\text{CE}}$ = LOW. The 74191 is not fully edge-triggered, has an active LOW Parallel Load input, no Master Reset input, an $\overline{\text{Up}}$/Dn input and an active HIGH Terminal Count output which is independent of $\overline{\text{CE}}$. The 74191 has a Ripple Clock output in lieu of a Master Reset input.	4-165
	Synchronous Binary/ Decade, Up/Down Counter	F4029	No TTL Equivalent	4-87
74192	BCD, Up/Down Counter	F40192	Same Pinout, Functionally Identical	4-274
74193	Binary, Up/Down Counter	F40193	Same Pinout, Functionally Identical	4-274
	4-Stage Divide-by-8 Johnson Counter	F4022	No TTL Equivalent	4-76
	Presettable Divide-by-N Counter	F4018	No TTL Equivalent	4-68
74142	Divide-by-10 Counter with Decoded Outputs	F4017	Different Pinout. The 74142 is a BCD Counter/Latch/Decoder. The decoded outputs are active LOW and can have decoding spikes. The F4017 is a 5-stage Johnson decade counter with active HIGH, glitchless decoded outputs.	4-65
74393	7-Stage Binary Counter	F4024	Different Pinout. The 74393, a dual 4-bit counter, can be connected as a 7-stage counter.	4-78
	12-Stage Binary Counter	F4040	No TTL Equivalent	4-98
	14-Stage Binary Counter	F4020	No TTL Equivalent	4-71
			REGISTERS	
74195 9300	4-Bit Shift Register	F40195	Same Pinout, Functionally Identical	4-282
74LS194	4-Bit Shift Register; Shift Left, Shift Right, Parallel Load and Hold Modes	F40194	Same Pinout, Functionally Identical	4-278
74195 9300	4-Bit Shift Register, SI/PI/SO/PO, Output Polarity Control	F4035	Different Pinout. The F4035 has an output polarity control and active HIGH Parallel Enable and Master Reset inputs. The 74195 and 9300 do not have output polarity control but they give the true and complement of Q_3. They have active LOW Parallel Enable and Master Reset inputs.	4-95
	Dual 4-Bit Shift Register, SI/SO/PO	F4015	No TTL Equivalent	4-59
74166	8-Bit Shift Register, SI/PI/SO	F4014	Different Pinout. The 74168 has two Clock inputs and a Master Reset input. It does not have the Q_5 and Q_6 outputs available. The Parallel Enable input is active LOW. The F4014 has a single Clock input and does not have a Master Reset input. It has the Q_5 and Q_6 outputs available. The Parallel Enable input is active HIGH.	4-57
74165	8-Bit Shift Register, SI/PI/SO	F4021	Different Pinout. The 74165 has two Clock inputs and a $\overline{Q}_7$ output. It does not have the Q_5 and Q_6 outputs available. The Parallel Load input is active LOW. The F4021 has a single Clock input and does not have a $\overline{Q}_7$ output. It has the Q_5 and Q_6 outputs available. The Parallel Load input is active HIGH.	4-74

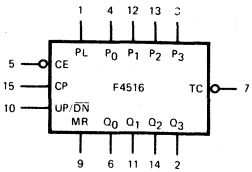
TTL TO CMOS FUNCTION SELECTOR GUIDE

F4510



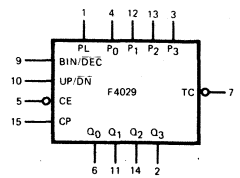
V_{DD} = Pin 16
V_{SS} = Pin 8

F4516



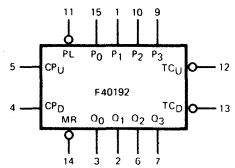
V_{DD} = Pin 16
V_{SS} = Pin 8

F4029



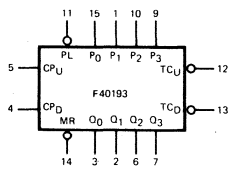
V_{DD} = Pin 16
V_{SS} = Pin 8

F40192



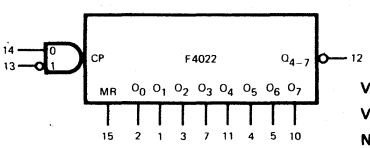
V_{DD} = Pin 16
V_{SS} = Pin 8

F40193



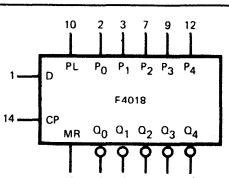
V_{DD} = Pin 16
V_{SS} = Pin 8

F4022



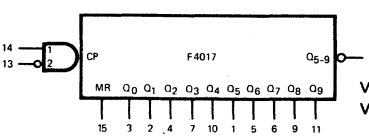
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 6, 9

F4018



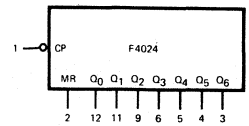
V_{DD} = Pin 16
V_{SS} = Pin 8

F4017



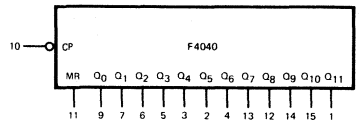
V_{DD} = Pin 16
V_{SS} = Pin 8

F4024



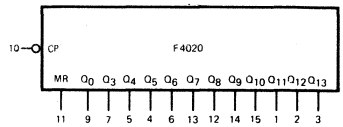
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10, 13

F4040



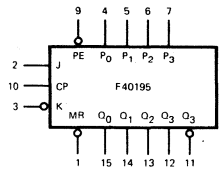
V_{DD} = Pin 16
V_{SS} = Pin 8

F4020



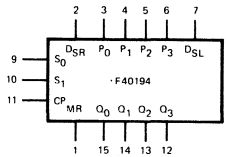
V_{DD} = Pin 16
V_{SS} = Pin 8

F40195



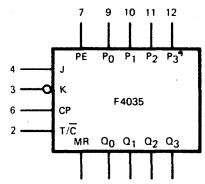
V_{DD} = Pin 16
V_{SS} = Pin 8

F40194



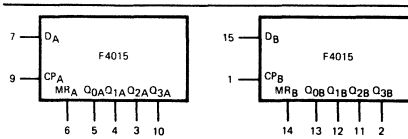
V_{DD} = Pin 16
V_{SS} = Pin 8

F4035



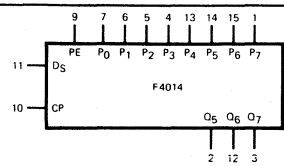
V_{DD} = Pin 16
V_{SS} = Pin 8

F4015



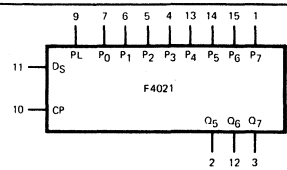
V_{DD} = Pin 16
V_{SS} = Pin 8

F4014



V_{DD} = Pin 16
V_{SS} = Pin 8

F4021



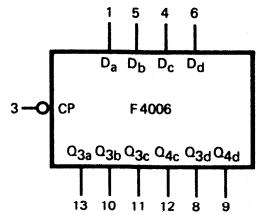
V_{DD} = Pin 16
V_{SS} = Pin 8

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			REGISTERS (Cont'd)	
	18-Stage Static Shift Register	F4006	No TTL Equivalent	4-46
	64-Stage Static Shift Register	F4031	No TTL Equivalent	4-93
	Quad 64-Bit Static Shift Register	F4731	No TTL Equivalent	4-253
			DECODERS/DEMULTIPLEXERS	
74LS139 9321	Dual 1-of-4 Decoder, Active LOW Outputs	F4556	Same Pinout, Functionally Identical	4-184
74LS139 9321	Dual 1-of-4 Decoder, Active HIGH Outputs	F4555	Same Pinout. The outputs of the F4555 are the complement of the outputs of the 74LS139 and 9321.	4-184
7442A 9301	1-of-10 Decoder, Active HIGH Outputs	F4028	Different Pinout. For input codes 0-9, the outputs of the F4028 are the complements of the outputs of the 7442A and 9301. For input codes 10-15, all outputs of the 7442A and the 9301 are HIGH. On the F4028, input codes 10, 12 and 14 generate a HIGH on O_8 a LOW on all other outputs, while input codes 11, 13 and 15 generate a HIGH on O_9, a LOW on all other outputs.	4-85
74154 9311	1-of-16 Decoder/ Demultiplexer with Input Latches	F4514	Different Pinout. The F4514 has an input latch, active HIGH outputs, one active LOW Enable input which forces all outputs LOW and a Latch Enable input. The 74154 and 9311 do not have an input latch, have active LOW outputs and have two active LOW Enable inputs which force all outputs HIGH.	4-159
74154 9311	1-of-16 Decoder/ Demultiplexer with Input Latches	F4515	Different Pinout. The F4515 has an input latch with an active HIGH Latch Enable, and an active LOW Enable input. The 74154 and 9311 do not have an input latch and have two active LOW Enable inputs.	4-162
9368	BCD-to-7-Segment Latch/Decoder/ Driver	F4511	Different Pinout. The F4511 has active LOW lamp test and Blanking inputs. The 9368 has a Ripple Blanking input and a Ripple Blanking output in lieu of the lamp test and Blanking inputs. The F4511 forces all segment outputs (a-f) LOW for input codes greater than nine, the 9368 generates the segment codes for a-f for input codes 10 to 15.	4-153
9368	BCD-to-7-Segment Latch/Decoder/ Driver	F4734	Different Package. The F4734 is in an 18-pin package; the 9368 is in a 16-pin package. The F4734 has active HIGH Ripple Blanking input and Ripple Blanking output; the 9368 has active LOW Ripple Blanking input and Ripple Blanking output. The F4734 has active LOW lamp test and Blanking inputs; the 9368 does not have these inputs. The F4734 forces all segment outputs (a-f) LOW for input codes greater than nine; the 9368 generates the segment codes for a-f for input codes 10 to 15.	4-255

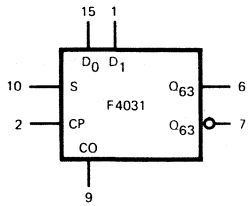
TTL TO CMOS FUNCTION SELECTOR GUIDE

F4006



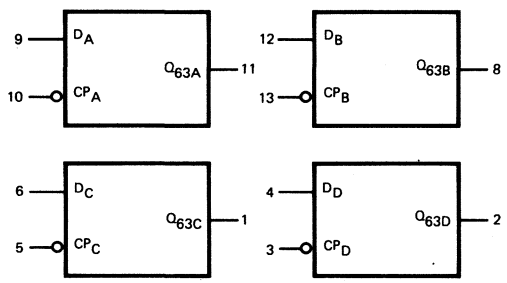
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2

F4031



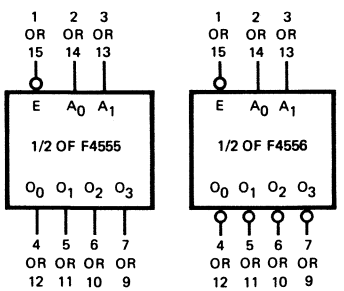
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pins 3,4,5,11, 12,13,14

F4731



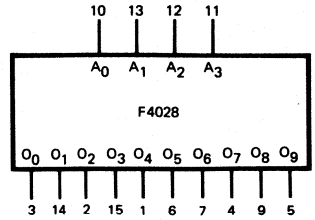
V_{DD} = Pin 14
V_{SS} = Pin 7

F4555 AND F4556



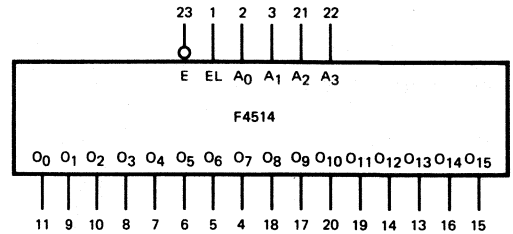
V_{DD} = Pin 16
V_{SS} = Pin 8

F4028



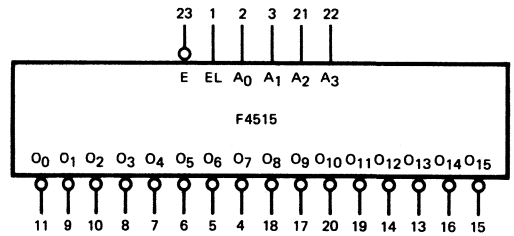
V_{DD} = Pin 16
V_{SS} = Pin 8

F4514



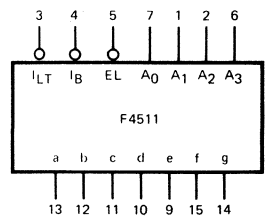
V_{DD} = Pin 24
V_{SS} = Pin 12

F4515



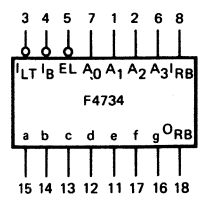
V_{DD} = Pin 24
V_{SS} = Pin 12

F4511



V_{DD} = Pin 16
V_{SS} = Pin 8

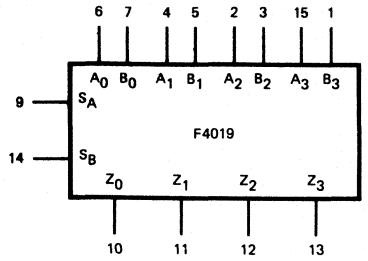
F4734



TTL TO CMOS FUNCTION SELECTOR GUIDE

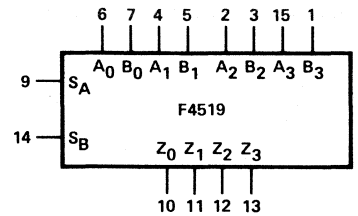
TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			MULTIPLEXERS	
74157 9322	Quad 2-Input Multiplexer	F4019	Different Pinout. The F4019 has two Select inputs which allow the choice of four possible outputs: O, A, B, A+B. The 74157 and 9322 have a single Select input which allows the selection of either A or B inputs, and an active LOW Enable input.	4-69
74157 9322	Quad 2-Input Multiplexer	F4519	Different Pinout. The F4519 has two Select inputs which allow the choice of four possible outputs: O, A, $\overline{B}$, A • B. The 74157 and 9322 have a single Select input which allows the selection of either A or B inputs and an active LOW Enable input.	4-171
74153	Dual 4-Input Multiplexer	F4539	Same Pinout, Functionally Identical	4-182
74251	8-Input Multiplexer 3-State Outputs	F4512	Different Pinout. The F4512 has an Enable input which forces all outputs LOW, but it does not have a $\overline{Z}$ output. The 74251 does not have an Enable input, but has both Z and $\overline{Z}$ outputs.	4-154
(74151 9312)			The 74151 and 9312 do not have 3-state outputs; they provide the $\overline{Z}$ output in lieu of the Output Enable input. The F4512 can perform the same function as the 74151 and 9312.	
			ANALOG SWITCHES AND MULTIPLEXERS/DEMULTIPLEXERS	
	Quad Bilateral Switch	F4016/ F4066	No TTL Equivalent. The F4016 and F4066 are "analog" switches.	4-62 4-124
	8-Channel Analog Multiplexer/Demultiplexer	F4051	No TTL Equivalent. The F4051 is an "analog" multiplexer/demultiplexer.	4-117
	Dual 4-Channel Analog Multiplexer/Demultiplexer	F4052	No TTL Equivalent. The F4052 is an "analog" multiplexer/demultiplexer.	4-120
	Triple 2-Channel Analog Multiplexer/ Demultiplexer	F4053	No TTL Equivalent. The F4053 is an "analog" multiplexer/demultiplexer.	4-123
	16-Channel Analog Multiplexer/Demultiplexer	F4067	No TTL Equivalent. The F4067 is an "analog" multiplexer/demultiplexer.	4-127

F4019



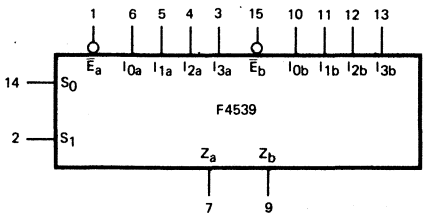
V_{DD} = Pin 16
V_{SS} = Pin 8

F4519



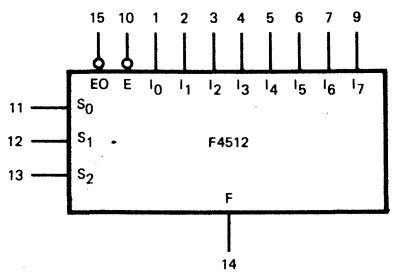
V_{DD} = Pin 16
V_{SS} = Pin 8

F4539



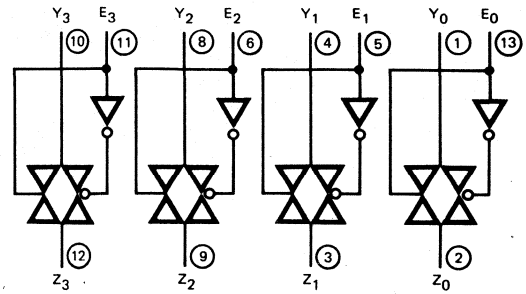
V_{DD} = Pin 16
V_{SS} = Pin 8

F4512



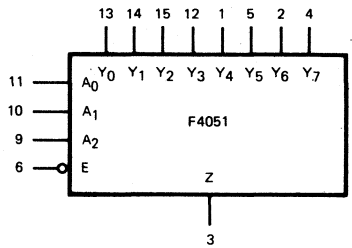
V_{DD} = Pin 16
V_{SS} = Pin 8

F4016 AND F4066



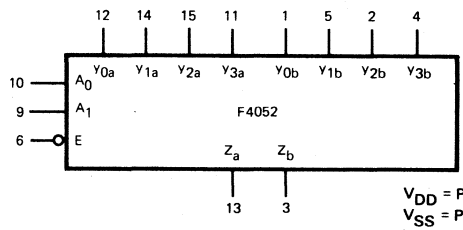
V_{DD} = Pin 14
V_{SS} = Pin 8

F4051



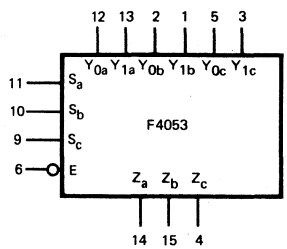
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

F4052



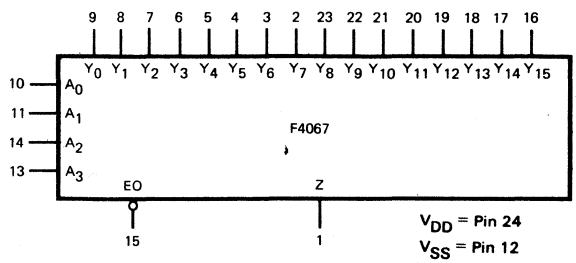
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

F4053



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

F4067



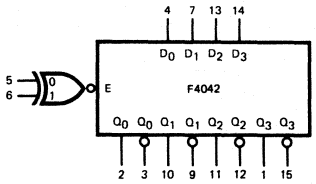
V_{DD} = Pin 24
V_{SS} = Pin 12

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			LATCHES	
7475	4-Bit Latch	F4042	Different Pinout. The 7475 has separate Enable inputs for bits 0,1 and 2,3. The F4042 has a Common Enable input for all four bits; but with the Exclusive-NOR Enable inputs, it is possible to have either an active HIGH or an active LOW Enable input.	4-102
74279	Quad R/S Latch with 3-State Outputs	F4043	Different Pinout. The F4043 has 3-state outputs and active LOW Set and Reset inputs. The 74279 does not have 3-state outputs and has two Set inputs on two of the latches.	4-105
74279	Quad R/S Latch with 3-State Outputs	F4044	Different Pinout. The F4044 has 3-state outputs and the Reset inputs override the Set inputs. The 74279 does not have 3-state outputs, has two Set inputs on two of the latches and the Set inputs override the Reset inputs.	4-108
9334 74259	8-Bit Addressable Latch	F4724	Same Pinout. The 9334 and 74259 have active LOW Clear inputs, the F4724 has an active HIGH Clear input.	4-247
	Dual 4-Bit Addressable Latch	F4723	No TTL Equivalent	4-244
			TRANSLATORS	
75367	Quad TTL-to-CMOS Converter, 3-State Outputs	F4104	Different Pinout. The F4104 has true and complement outputs and a common active HIGH Output Enable input. The 75367 has only the inverted outputs available and has individual active LOW Output Enable inputs.	4-146
			ARITHMETIC OPERATORS, ADDERS, COMPARATORS	
74L85	4-Bit Magnitude Comparator	F40085	Same Pinout, Functionally Identical	4-256
9348	13-Bit Parity Checker/Generator	F4531	Different Pinout. The F4531 is a 13-bit parity checker/generator with a single output. The 9348 is a 12-bit parity checker/generator with two outputs, odd parity and even parity.	4-177
74148 9318	8-Input Priority Encoder	F4532	Same Pinout. The F4532 has active HIGH inputs and outputs. The 74148 and 9318 have active LOW inputs and outputs.	4-179
74182 9342	Lookahead Carry Generator	F4582	Same Pinout, Functionally Identical	4-186
9404	Data Path Switch	F4704	Same Pinout, Functionally Identical	4-211
9405	Arithmetic Logic Register Stack	F4705	Same Pinout, Functionally Identical	4-215
9407	Data Access Register	F4707	Same Pinout, Functionally Identical	4-232

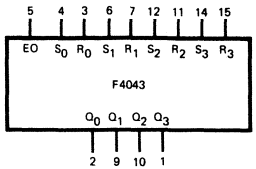
TTL TO CMOS FUNCTION SELECTOR GUIDE

F4042



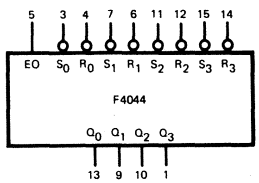
V_{DD} = Pin 16
V_{SS} = Pin 8

F4043



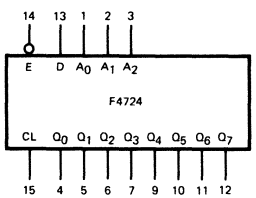
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 13

F4044



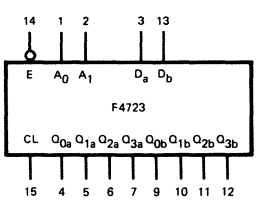
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 2

F4724



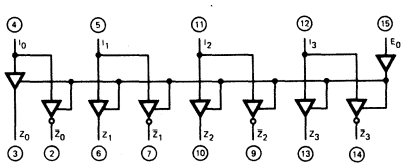
V_{DD} = Pin 16
V_{SS} = Pin 8

F4723



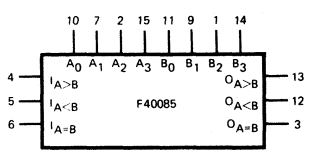
V_{DD} = Pin 16
V_{SS} = Pin 8

F4104



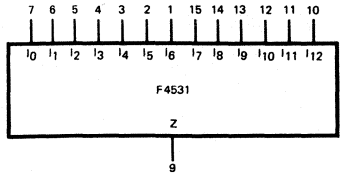
V_{DDO} = Pin 1
V_{DD1} = Pin 16
V_{SS} = Pin 8

F40085



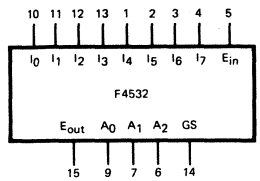
V_{DD} = Pin 16
V_{SS} = Pin 8

F4531



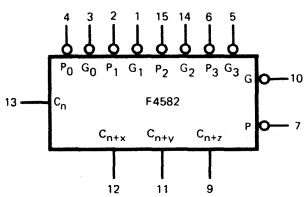
V_{DD} = Pin 16
V_{SS} = Pin 8

F4532



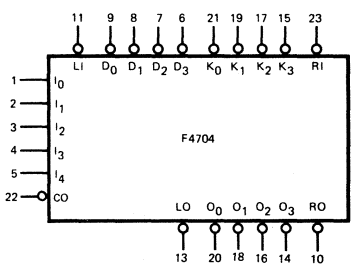
V_{DD} = Pin 16
V_{SS} = Pin 8

F4582



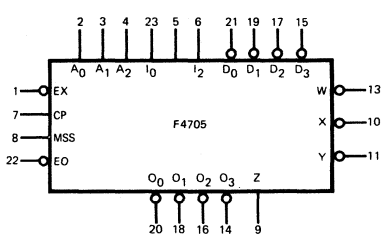
V_{DD} = Pin 24
V_{SS} = Pin 12

F4704



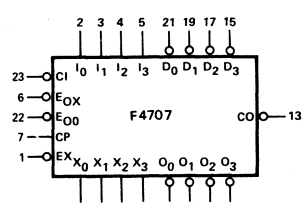
V_{DD} = Pin 24
V_{SS} = Pin 12

F4705



V_{DD} = Pin 24
V_{SS} = Pin 12

F4707



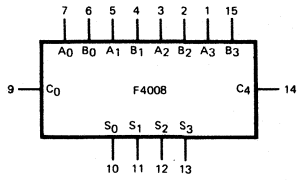
V_{DD} = Pin 24
V_{SS} = Pin 12

TTL TO CMOS FUNCTION SELECTOR GUIDE

TTL	FUNCTION	CMOS	FUNCTIONAL DIFFERENCES BETWEEN CMOS AND TTL	PAGE NO.
			ARITHMETIC OPERATORS, ADDERS, COMPARATORS (Cont'd)	
'7483A '74283	4-Bit Binary Full Adder	F4008	Different Pinout, Functionally Identical	4-50
'74283	4-Bit Binary Full Adder	F40283	Same Pinout, Functionally Identical	4-286
			LSI – SPECIAL FUNCTION	
	Programmable Bit Rate Generator	F4702	No TTL Equivalent	4-189
			PHASE-LOCKED LOOPS, MULTIVIBRATORS	
'9602	Dual Retriggerable Resettable Monostable Multivibrator	F4528	Same Pinout, Functionally Identical	4-176
	Low Power Monostable/Astable Multivibrator	F4047	No TTL Equivalent	4-113
	Micropower Phase-Locked Loop	F4046	No TTL Equivalent	4-111
			MEMORIES	
'4S189	16 x 4-Bit RAM with 3-State Outputs	F4725	Same Pinout, Functionally Identical	4-250
'9410	16 x 4-Bit Clocked RAM with 3-State Output Register	F4710	Same Pinout, Functionally Identical	4-238
'74200	256 x 2-Bit RAM with 3-State Outputs	F4720	Different Pinout. The 74200 has three Chip Select inputs but does not have a Q output. Write Enable is active LOW. The F4720 has only one Chip Select input but has both Q and $\overline{Q}$ outputs. Write Enable is active HIGH. The F4720 is transparent in the Write mode. The 74200 outputs are in the high impedance "OFF" state in the Write mode.	4-241
'9403	16 x 4 Parallel/ Serial FIFO	F4703	Same Pinout, Functionally Identical	4-197
'9406	Program Stack	F4706	Same Pinout, Functionally Identical	4-220

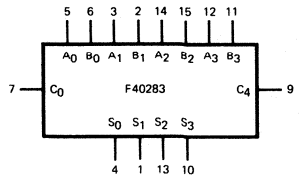
TTL TO CMOS FUNCTION SELECTOR GUIDE

F4008



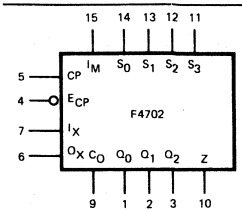
V_{DD} = Pin 16
V_{SS} = Pin 8

F40283



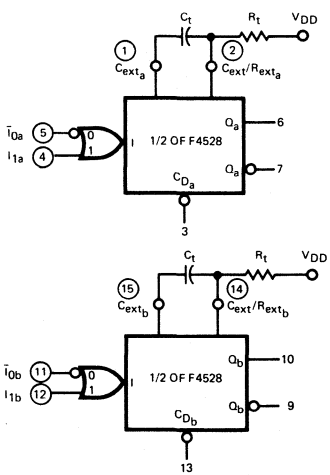
V_{DD} = Pin 16
V_{SS} = Pin 8

F4702



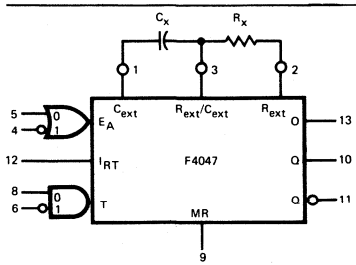
V_{DD} = Pin 16
V_{SS} = Pin 8

F4528



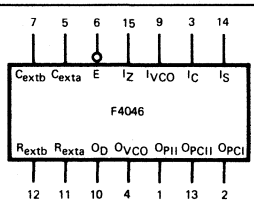
V_{DD} = Pin 16
V_{SS} = Pin 8

F4047



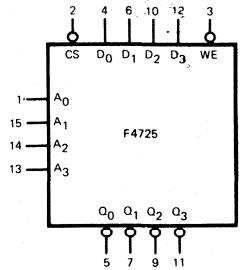
V_{DD} = Pin 14
V_{SS} = Pin 7

F4046



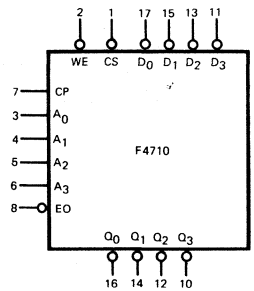
V_{DD} = Pin 16
V_{SS} = Pin 8

F4725



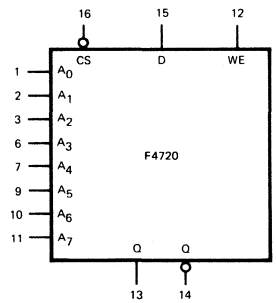
V_{DD} = Pin 16
V_{SS} = Pin 8

F4710



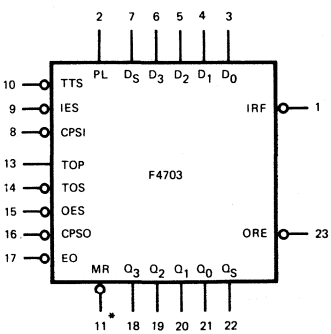
V_{DD} = Pin 18
V_{SS} = Pin 9

F4720



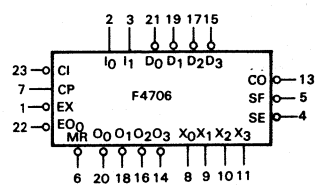
V_{DD} = Pin 5
V_{SS} = Pin 8
NC = Pin 4

F4703



V_{DD} = Pin 24
V_{SS} = Pin 12

F4706



V_{DD} = Pin 24
V_{SS} = Pin 12

CROSS REFERENCE GUIDE

Fairchild	RCA Series A	RCA* Series B	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments	Signetics
F4001	CD4001A		MC14001A	CD4001A	SCL4001A	CM4001A	HD4001A	TP4001A	4001A
F4002	CD4002A		MC14002A	CD4002A	SCL4002A	CM4002A	HD4002A	TP4002A	4002A
F4006	CD4006A		MC14006A	CD4006A	SCL4006A	CM4006A	HD4006A		4006A
F4007	CD4007A		MC14007A	CD4007A	SCL4007A	CM4007A	HD4007A	TP4007A	4007A
F4008	CD4008A		MC14008A		SCL4008A	CM4008A	HD4008A	TP4008A	4008A
F4011	CD4011A		MC14011A	CD4011A	SCL4011A	CM4011A	HD4011A	TP4011A	4011A
F4012	CD4012A		MC14012A	CD4012A	SCL4012A	CM4012A	HD4012A	TP4012A	4012A
F4013	CD4013A		MC14013A	CD4013A	SCL4013A	CM4013A	HD4013A	TP4013A	4013A
F4014	CD4014A		MC14014A	CD4014A	SCL4014A	CM4014A	HD4014A	TP4014A	4014A
F4015	CD4015A		MC14015A	CD4015A	SCL4015A		HD4015A	TP4015A	4015A
F4016	CD4016A		MC14016A	CD4016A	SCL4016A	CM4016A		TP4016A	4016A
F4017	CD4017A		MC14017A	CD4017A	SCL4017A	CM4017A	HD4017A	TP4017A	4017A
F4018	CD4018A			CD4018A	SCL4018A	CM4018A	HD4018A	TP4018A	4018A
F4019	CD4019A			CD4019A	SCL4019A	CM4019A	HD4019A	TP4019A	4019A
F4020	CD4020A		MC14020A	CD4020A	SCL4020A	CM4020A	HD4020A	TP4020A	4020A
F4021	CD4021A		MC14021A	CD4021A	SCL4021A	CM4021A	HD4021A	TP4021A	4021A
F4022	CD4022A		MC14022A	CD4022A	SCL4022A	CM4022A	HD4022A	TP4022A	4022A
F4023	CD4023A		MC14023A	CD4023A	SCL4023A	CM4023A	HD4023A	TP4023A	4023A
F4024	CD4024A		MC14024A	CD4024A	SCL4024A	CM4024A	HD4024A	TP4024A	4024A
F4025	CD4025A		MC14025A	CD4025A	SCL4025A	CM4025A	HD4025A	TP4025A	4025A
F4027	CD4027A		MC14027A	CD4027A	SCL4027A		HD4027A	TP4027A	4027A
F4028	CD4028A		MC14028A	CD4028A	SCL4028A		HD4028A	TP4028A	4028A
F4029	CD4029A			CD4029A	SCL4029A		HD4029A	TP4029A	4029A
F4030	CD4030A			CD4030A	SCL4030A		HD4030A	TP4030A	4030A
F4031	CD4031A			CD4031A					
F4035	CD4035A		MC14035A	CD4035A	SCL4035A		HD4035A	TP4035A	4035A
F4040	CD4040A		MC14040A	CD4040A	SCL4040A		HD4040A	TP4040A	4040A
F4041	CD4041A				SCL4041A	CM4041A		TP4041A	4041A
F4042	CD4042A		MC14042A	CD4042A	SCL4042A		HD4042A	TP4042A	4042A
F4043	CD4043A			CD4043A	SCL4043A	CM4043A	HD4043A	TP4043A	4043A
F4044	CD4044A			CD4044A	SCL4044A	CM4044A	HD4044A	TP4044A	4044A
F4046	CD4046A		MC14046A						
F4047	CD4047A					CM4047A			
F4049	CD4049A		MC14049A	CD4049A	SCL4049A		HD4049A	TP4049A	4049A
F4050	CD4050A		MC14050A	CD4050A	SCL4050A		HD4050A	TP4050A	4050A
F4051	CD4051A			CD4051A				TP4051A	4051A
F4052	CD4052A			CD4052A				TP4052A	4052A
F4053	CD4053A		MC14053A	CD4053A	SCL4053A		HD4053A	TP4053A	4053A
F4066	CD4066A			CD4066A			HD4066A		4066A
F4067		CD4067B							
F4068		CD4068B							4068B
F4069		CD4069B		CD4069B					4069B
F4070		CD4070B	MC14507	CD4070B					
F4071		CD4071B							4071B
F4072		CD4072B							4072B
F4073		CD4073B							4073B
F4075		CD4075B							4075B
F4076		CD4076B	MC14076B	CD4076B					
F4077		CD4077B					HD4811		
F4078		CD4078B							4078B

CROSS REFERENCE GUIDE

Fairchild	RCA Series A	RCA* Series B	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments	Signetics
F4081		CD4081B							4081B
F4082		CD4082B							4082B
F4085		CD4085B							
F4086		CD4086B							
F4104						CM4104			
F4510		CD4510B	MC14510		SCL14510				14510
F4511		CD4511B	MC14511	MM14511	SCL14511				
F4512			MC14512					TP4512A	
F4514		CD4514B	MC14514		SCL14514			TP4514A	
F4515		CD4515B	MC14515		SCL14515			TP4515A	
F4516		CD4516B	MC14516		SCL14516				14516
F4518		CD4518B	MC14518		SCL14518			TP4518A	14518
F4519			MC14519					TP4519A	
F4520		CD4520B	MC14520		SCL14520			TP4520A	14520
F4522			MC14522					TP4522A	
F4526			MC14526					TP4526A	
F4528			MC14528		SCL14528				14528
F4531			MC14531					TP4531A	
F4532		CD4532B	MC14532						
F4539			MC14539					TP4539A	
F4555		CD4555B	MC14555						
F4556		CD4556B	MC14556						
F4582			MC14582						
F4702									
F4703									
F4704									
F4705									
F4706									
F4707									
F4710									
F4720	**CD4061A								
F4723									
F4724		**CD4099B							
F4725									
F4731									
F4734			MC14513						
F40085			**MC14585	MM74C85					
F40097				MM80C97					
F40098				MM80C98					
F40160			MC14160	MM74C160			HD74C160	TP4360	
F40161			MC14161	MM74C161			HD74C161	TP4361	
F40162			MC14162	MM74C162			HD74C162	TP4362	
F40163			MC14163	MM74C163			HD74C163	TP4363	
F40174			MC14174	MM74C174			HD74C174		
F40175			MC14175	MM74C175					
F40192		CD40192B		MM74C192			HD74C192		
F40193		CD40193B		MM74C193			HD74C193		
F40194		CD40194B	MC14194						
F40195				MM74C195			HD74C195		
F40283									

CROSS REFERENCE GUIDE

PACKAGE CODE CROSS REFERENCE

Package	Fairchild	RCA	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments	Signetics
Plastic DIP	P	E	P	N	E	E	1	N	A, B, N
Ceramic DIP	D	D or F	L	D	D	D	1	J	E, F, Y
Ceramic Flatpak	F	K	–	F	F	–	9	–	J, Q, P, R

TEMPERATURE CODE CROSS REFERENCE

Temperature Range	Fairchild	RCA	Motorola	National	Solid State Scientific	Solitron	Harris	Texas Instruments	Signetics
Military (–55°C to +125°C)	M	D, K, F Packages Only	A	54CXX 70CXX M	D, F Packages Only	D Package Only	2	TF	S
Commercial (–40°C to +85°C)	C	E Package Only	C	C	E Package Only	E Package Only	4	TP	N
Commercial (0°C to +70°C)	–	–	–	74CXX 80CXX	–	–	5	TL	N

*These devices are members of the new RCA Series B CMOS. All Fairchild F4000 Series CMOS devices are direct pin-for-pin replacements for RCA's Series A and Series B CMOS.

**This device is a functional equivalent only.

***This device is a pin-for-pin compatible if leads 4 and 8 are tied together.

F4000
SERIES CMOS FAMILY CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (Non-operating) above which useful life may be impaired. All voltages are referenced to V_{SS}.

Supply Voltage V_{DD}	−0.5 to 18 V
Voltage on any Input	−0.5 to V_{DD} +0.5 V
Current into any Input	±10 mA
Maximum Power Dissipation	400 mW
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 s)	300°C

RECOMMENDED OPERATING CONDITIONS

Fairchild CMOS will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} equal to 5, 10 and 15 V. Where low power dissipation is required, the lowest power supply voltage, consistent with required speed, should be used. For larger noise immunity, higher power supply voltages should be specified. Because of its wide operating range, power supply regulation and filtering are less critical than with other types of logic. The lower limit of supply regulation is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic.

Unused inputs must be connected to V_{DD}, V_{SS} or another input.

Care should be used in handling CMOS devices; large static charges may damage the device.

Operating temperature ranges are −40°C to +85°C for Commercial and −55°C to +125°C for Military.

PARAMETER	F4000XC			F4000XM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage, V_{DD}	3		15	3		15	V
Operating Free Air Temperature Range	−40	+25	+85	−55	+25	+125	°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Ordering Information section.

DC CHARACTERISTICS FOR THE F4000 SERIES CMOS FAMILY – Parametric Limits listed below are guaranteed for the entire Fairchild CMOS Family unless otherwise specified on the individual data sheets.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage		4.99			V	MIN, 25°C	I_{OH} = 0 mA, Inputs at 0 or 5 V per	
			4.95				MAX	the Logic Function or Truth Table	
			4.0			V	All	I_{OH} = 0 mA, Inputs at 1.5 or 3.5 V	
V_{OL}	Output LOW Voltage				0.01	V	MIN, 25°C	I_{OL} = 0 mA, Inputs at 0 or 5 V per	
					0.05		MAX	the Logic Function or Truth Table	
					0.5	V	All	I_{OL} = 0 mA, Inputs at 1.5 or 3.5 V	
I_{IN}	Input Current	XC			0.1	μA	25°C	Lead under test at 0 or 5 V	
		XM			0.01			All other Inputs simultaneously at 0 or 5 V	
I_{OH}	Output HIGH Current		−1.5			mA	MIN, 25°C	V_{OUT} = 2.5 V	Inputs at 0 or 5 V per the Logic Function or Truth Table
			−1.0				MAX		
			−0.7			mA	MIN, 25°C	V_{OUT} = 4.5 V	
			−0.4				MAX		
I_{OL}	Output LOW Current		1.0			mA	MIN	V_{OUT} = 0.4 V	
			0.8				25°C		
			0.4				MAX		

F4000 SERIES CMOS FAMILY CHARACTERISTICS

DC CHARACTERISTICS: V_{DD} = 10 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		7.0			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				3.0	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		9.99			V	MIN, 25°C	I_{OH} = 0 mA, Inputs at 0 or 10 V per
			9.95				MAX	the Logic Function or Truth Table
			9.0			V	All	I_{OH} = 0 mA, Inputs at 3 or 7 V
V_{OL}	Output LOW Voltage				0.01	V	MIN, 25°C	I_{OL} = 0 or mA, Inputs at 0 or 10V per
					0.05		MAX	the Logic Function or Truth Table
					1.0	V	All	I_{OL} = 0 mA, Inputs at 3 or 7 V
I_{IN}	Input Current	XC			0.1	μA	25°C	Lead under test at 0 or 10 V
		XM			0.01			All other Inputs Simultaneously at 0 or 10 V
I_{OH}	Output HIGH Current		−1.4			mA	MIN, 25°C	V_{OUT} = 9.5 V; Inputs at 0 or 10 V per the Logic Function or Truth Table
			−0.8				MAX	
I_{OL}	Output LOW Current		2.6			mA	MIN	V_{OUT} = 0.5 V; Inputs at 0 or 10 V per the Logic Function or Truth Table
			2.0				25°C	
			1.2				MAX	

DC CHARACTERISTICS: V_{DD} = 15 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		10.5			V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				4.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		14.99			V	MIN, 25°C	I_{OH} = 0 mA, Inputs at 0 or 15 V per
			14.95				MAX	the Logic Function or Truth Table
			13.0			V	All	I_{OH} = 0 mA, Inputs at 4.5 or 10.5 V
V_{OL}	Output LOW Voltage				0.01	V	MIN, 25°C	I_{OL} = 0 mA, Inputs at 0 or 15 V per
					0.05		MAX	the Logic Function or Truth Table
					2.0	V	All	I_{OL} = 0 mA, Inputs at 4.5 or 10.5 V
I_{IN}	Input Current	XC			1.0	μA	25°C	Lead under test at 0 or 15 V
		XM			1.0			All other Inputs Simultaneously at 0 or 15 V
I_{OH}	Output HIGH Current		−2.2			mA	MIN, 25°C	V_{OUT} = 14.5 V; Inputs at 0 or 15 V per the Logic Function or Truth Table
			−1.4				MAX	
I_{OL}	Output LOW Current		3.6			mA	MIN, 25°C	V_{OUT} = 0.5 V; Inputs at 0 or 15 V per the Logic Function or Truth Table
			2.0				MAX	

TYPICAL F4000 SERIES CHARACTERISTICS

Fig. 3-1
POSITIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE

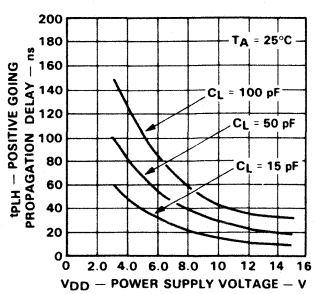


Fig. 3-2
NEGATIVE-GOING PROPAGATION DELAY VERSUS SUPPLY VOLTAGE

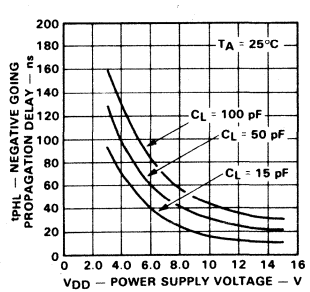


Fig. 3-3
POSITIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

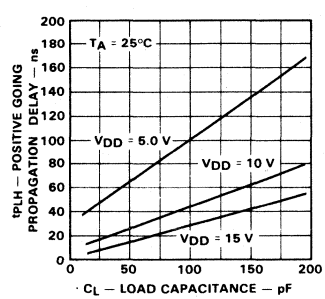


Fig. 3-4
NEGATIVE-GOING PROPAGATION DELAY VERSUS LOAD CAPACITANCE

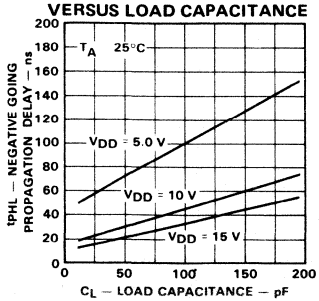


Fig. 3-5
VOLTAGE TRANSFER CHARACTERISTICS OVER −55°C TO +125°C RANGE

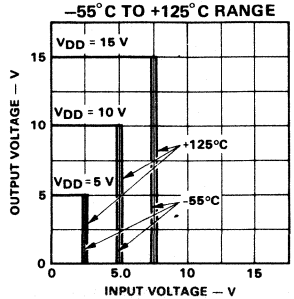


Fig. 3-6
GATE POWER DISSIPATION VERSUS FREQUENCY

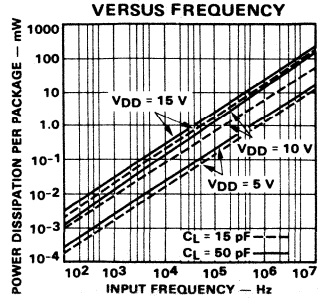


Fig. 3-7
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 5.0 V

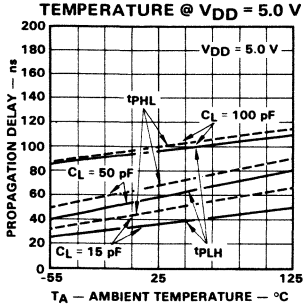


Fig. 3-8
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 10 V

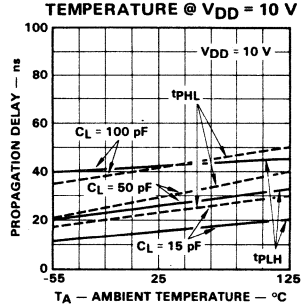


Fig. 3-9
PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE @ V_{DD} = 15 V

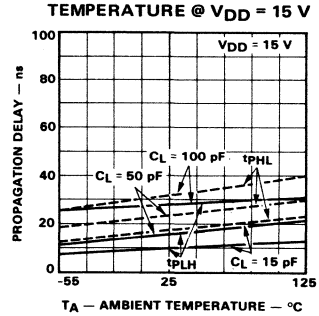


Fig. 3-10
p-CHANNEL DRAIN CHARACTERISTICS

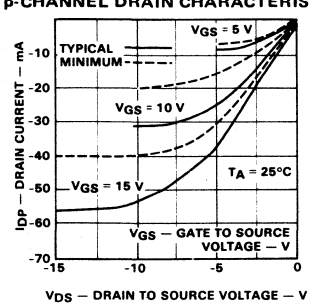


Fig. 3-11
n-CHANNEL DRAIN CHARACTERISTICS

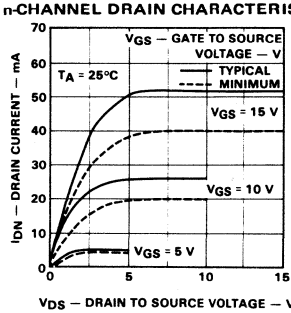


Fig. 3-12
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE

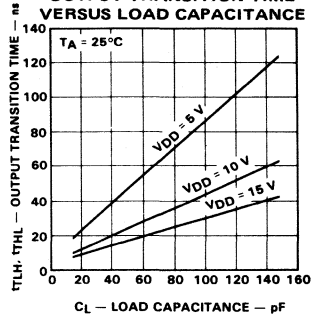
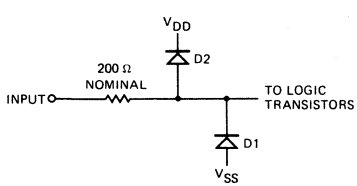


Fig. 3-13
INPUT PROTECTION CIRCUIT



INPUT CIRCUITRY

All inputs are protected by the network of Figure 3-13; a series input resistor plus diodes D1 and D2 clamp input voltages between V_{SS} and V_{DD}. Forward conduction of these diodes is typically 0.9 V at 1 mA. When V_{SS} or V_{DD} is not connected, avalanche breakdown of the diodes limit input voltage; D1 typically breaks down at 20 V, D2 at 20 V. In normal logic operation the diodes never conduct, but for certain special applications such as oscillators, circuit operation may actually depend on diode conduction. Operation in this mode is permissible so long as input currents do not exceed 10 mA.

Input capacitance is typically 5 pF across temperature for any input.

DEFINITION OF SYMBOLS AND TERMS USED IN DATA SHEETS

CURRENTS — Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{IN} — (Input Current) — The current flowing into a device at specified input voltage and V_{DD}.

I_{OH} — (Output HIGH Current) — The drive current flowing out of the device at specified HIGH output voltage and V_{DD}.

I_{OL} — (Output LOW Current) — The drive current flowing into the device at specified LOW output voltage and V_{DD}.

I_{DD} — (Quiescent Power Supply Current) — The current flowing into the V_{DD} lead at specified input and V_{DD} conditions.

I_{OZH} — (Output OFF Current HIGH) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{OZL} — (Output OFF Current LOW) — The leakage current flowing out of a 3-state device in the "OFF" state at a specified HIGH output voltage and V_{DD}.

I_{IL} — (Input Current LOW) — The current flowing into a device at a specified LOW level input voltage and a specified V_{DD}.

I_{IH} — (Input Current HIGH) — The current flowing into a device at a specified HIGH level input voltage and a specified V_{DD}.

I_{DDL} — (Quiescent Power Supply Current LOW) — The current flowing into the V_{DD} lead with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.

I_{DDH} — (Quiescent Power Supply Current HIGH) — The current flowing into the V_{DD} lead with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.

I_Z — (OFF State Leakage Current) — The leakage current flowing into the output of a 3-state device in the "OFF" state at a specified output voltage and V_{DD}.

VOLTAGES — All voltages are referenced to V_{SS} (or V_{EE}) which is the most negative potential applied to the device.

V_{DD} — (Drain Voltage) — The most positive potential on the device.

V_{IH} — (Input HIGH Voltage) — The range of input voltages that represents a logic HIGH level in the system.

V_{IL} — (Input LOW Voltage) — The range of input voltages that represents a logic LOW level in the system.

V_{IH} (min) — (Minimum Input HIGH Voltage) — The minimum allowed input HIGH level in a logic system.

V_{IL} (max) — (Maximum Input LOW Voltage) — The maximum allowed input LOW level in a system.

V_{OH} — (Output HIGH Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} — (Output LOW Voltage) — The range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

V_{SS} — (Source Voltage) — For a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages. Typically ground.

V_{EE} — (Source Voltage) — One of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supplies, the most negative power supply used as a reference level for other voltages.

ANALOG TERMS

R_{ON} — (ON Resistance) — The effective "ON" state resistance of an analog transmission gate, at specified input voltage, output load and V_{DD}.

ΔR_{ON} — ("Δ" ON Resistance) — The difference in effective "ON" resistance between any two transmission gates of an analog device at specified input voltage, output load and V_{DD}.

AC SWITCHING PARAMETERS

f_{MAX} — (Toggle Frequency/Operating Frequency) — The maximum rate at which clock pulses may be applied to a sequential circuit with the output of the circuit changing between 30% of V_{DD} and 70% of V_{DD}. Above this frequency the device may cease to function. See Figure 3-15.

t_{PLH} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level. See Figure 3-14.

t_{PHL} — (Propagation Delay Time) — The time between the specified reference points, normally 50% points on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level. See Figure 3-14.

t_{TLH} — (Transition Time, LOW to HIGH) — The time between two specified reference points on a waveform, normally 10% to 90% of V_{DD}, which is changing from LOW to HIGH. See Figure 3-14.

t_{THL} — (Transition Time, HIGH to LOW) — The time between two specified reference points on a waveform, normally 90% to 10% of V_{DD}, which is changing from HIGH to LOW. See Figure 3-14.

t_w — (Pulse Width) — The time between 50% amplitude points on the leading and trailing edges of pulse.

t_h — (Hold Time) — The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s — (Set-up Time) — The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} — (3-State Output Disable Time, HIGH to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} drop on the Output voltage waveform of a 3-state device, with the output changing from the defined HIGH level to a high impedance OFF state.

t_{PLZ} — (3-State Output Disable Time, LOW to Z) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing a 0.1 V_{DD} rise on the Output voltage waveform of a 3-state device, with the output changing from the defined LOW level to a high impedance OFF state.

t_{PZH} — (3-State Output Enable Time, Z to HIGH) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the Output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined HIGH level.

t_{PZL} — (3-State Output Enable Time, Z to LOW) — The time between the specified reference points, normally the 50% point on the Output Enable input voltage waveform and a point representing 0.5 V_{DD} on the Output voltage waveform of a 3-state device, with the output changing from a high impedance OFF state to the defined LOW level.

t_{rec} — (Recovery Time) — The time between the end of an overriding asynchronous input, typically a Clear or Reset input, and the earliest allowable beginning of a synchronous control input, typically a Clock input, normally measured at 50% points on both input voltage waveforms.

t_{CW} — (Clock Period) — The time between 50% amplitude points on the leading edges of a clock pulse.

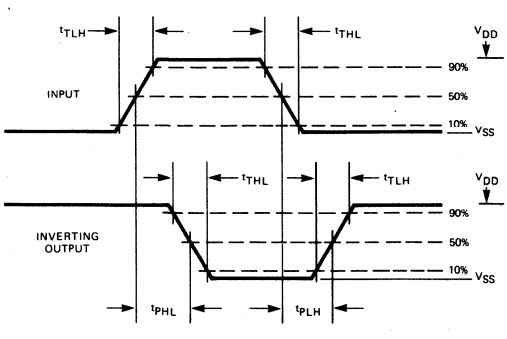


Fig. 3-14. Propagation Delay, Transition Time

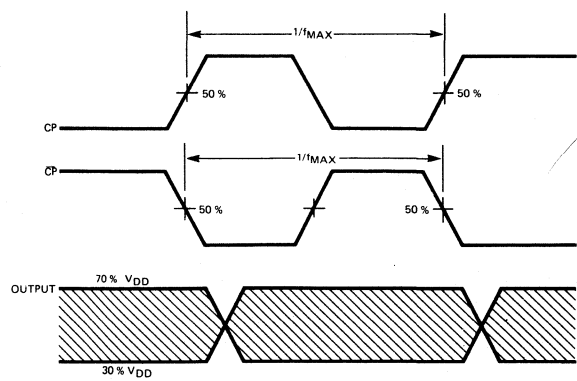
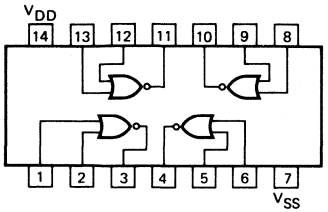


Fig. 3-15. Maximum Operating Frequency

F4001 QUAD 2-INPUT NOR GATE • F4002 DUAL 4-INPUT NOR GATE

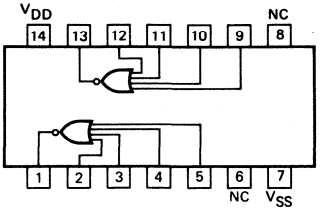
DESCRIPTION — These CMOS logic elements provide the positive input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

F4001
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-line Package.

F4002
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS See Note 1
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0	μA	MAX	
		XM			0.05			0.1		0.02		MIN, 25°C	
					3.0			6.0		1.2	μA	MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, F4001 only (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS See Note 2
t_{PLH}	Propagation Delay		40	75		20	40		15		ns	
t_{PHL}			40	75		20	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		25	75		10	40		8	25	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		25	75		10	40		8	25	ns	
t_{PLH}	Propagation Delay		60	110		25	60		20		ns	
t_{PHL}			60	110		25	60		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		60	135		30	70		20	45	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		60	135		30	70		20	45	ns	

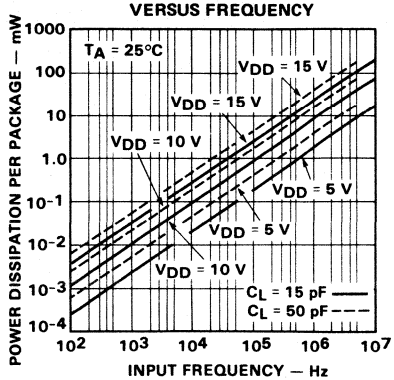
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, F4002 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS See Note 2
t_{PLH}	Propagation Delay		50	75		20	40		15		ns	
t_{PHL}			50	75		23	40		17		ns	C_L = 15 pF
t_{TLH}	Output Transition		30	75		15	40		11	25	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		25	75		10	40		7	25	ns	
t_{PLH}	Propagation Delay		65	110		30	60		20		ns	
t_{PHL}			70	110		30	60		23		ns	C_L = 50 pF
t_{TLH}	Output Transition		75	135		40	70		30	45	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		60	135		23	70		15	45	ns	

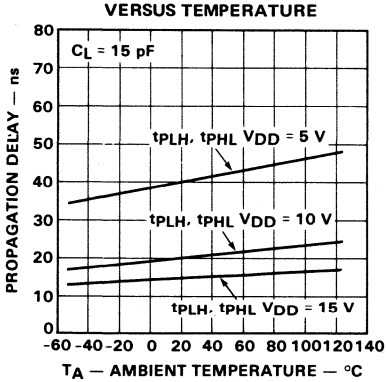
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

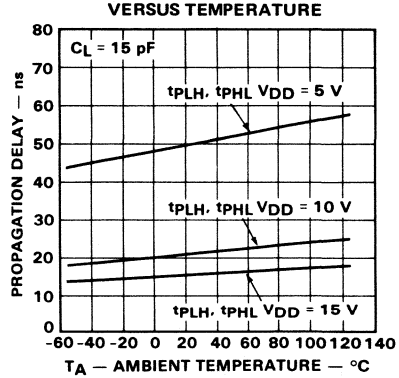
F4001 AND F4002
POWER DISSIPATION
VERSUS FREQUENCY



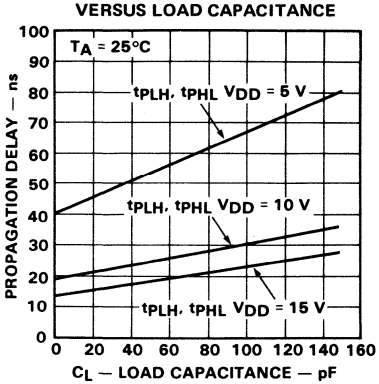
F4001
PROPAGATION DELAY
VERSUS TEMPERATURE



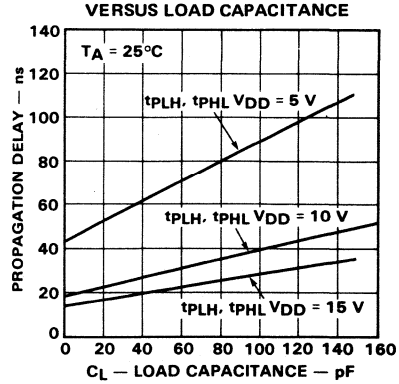
F4002
PROPAGATION DELAY
VERSUS TEMPERATURE



F4001
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



F4002
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



F4006/34006

18-STAGE STATIC SHIFT REGISTER

DESCRIPTION — The F4006 is an 18-stage Shift Register arranged as two 4-stage and two 5-stage shift regsiters with a common Clock Input ($\overline{CP}$). The two 4-stage shift registers, each have a Data Input (D_a, D_b) and a Data Output (Q_{3a}, Q_{3b}); the two 5-stage shift registers each have a Data Input (D_c, D_d) and Data Outputs from the fourth and fifth stages (Q_{3c}, Q_{4c}, Q_{3d}, Q_{4d}).

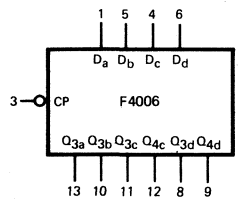
The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data is shifted into the first register position of each register from the Data Inputs (D_a-D_d) and all the data in each register is shifted one position to the right on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$).

- **CLOCK EDGE-TRIGGERED ON A HIGH-TO-LOW TRANSITION**
- **CASCADABLE**
- **SERIAL-TO-SERIAL DATA TRANSFER**

PIN NAMES

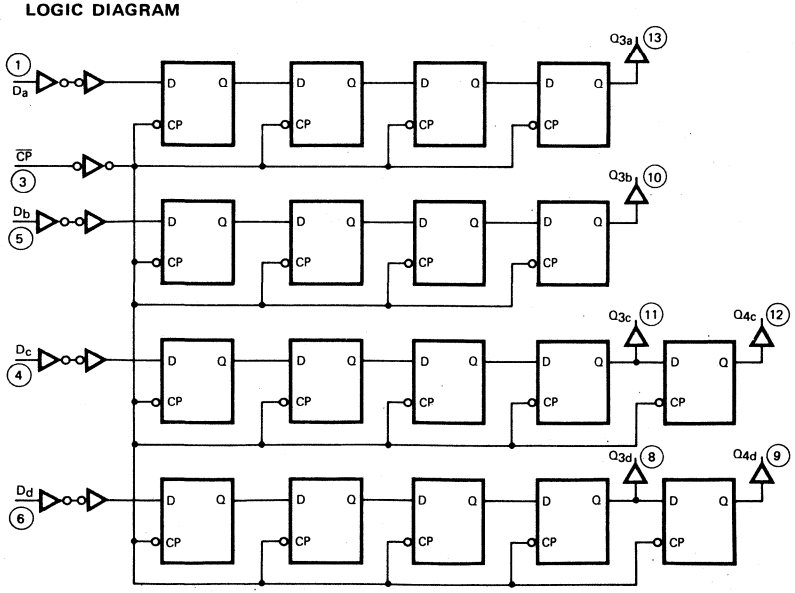
D_a-D_d	Data Inputs
$\overline{CP}$	Clock Input (H→L Edge-Triggered)
Q_{3a}-Q_{3d}, Q_{4c}, Q_{4d}	Data Outputs

LOGIC SYMBOL



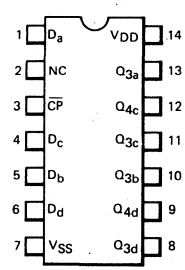
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pin 2
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

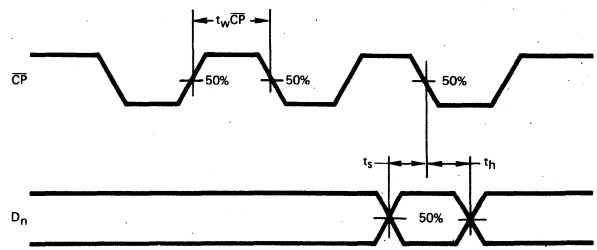
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			5			10		2		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					70			140		28			MAX	
		XM			0.5			1.0		0.2		μA	MIN, 25°C	
					30			60		12			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}$ to any Q_n		125 125			60 60			40 40		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{TLH} t_{THL}	Output Transition Time		30 30			20 20			15 15		ns ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to any Q_n		140 140			70 70			50 50		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{TLH} t_{THL}	Output Transition Time		60 60			30 30			20 20		ns ns	
$t_w\overline{CP}$	$\overline{CP}$ Minimum Pulse Width		50			30			20		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_s t_h	Set-Up Time D_n to $\overline{CP}$ Hold Time D_n to $\overline{CP}$		−30 50			−15 25			−10 15		ns ns	
f_{MAX}	Max. Input Clock Frequency (Note 4)		5			10					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s) Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{CP}$

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

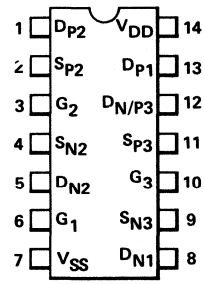
F4007/34007

DUAL COMPLEMENTARY PAIR PLUS INVERTER

DESCRIPTION – The F4007 is a Dual Complementary Pair and an Inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors. For proper operation $V_{SS} \leq V_1 \leq V_D$.

- **INPUT DIODE PROTECTION ON ALL INPUTS**
- **DRAINS AND SOURCES TO N- AND P-CHANNEL TRANSISTORS AVAILABLE**

CONNECTION DIAGRAM
DIP (TOP VIEW)

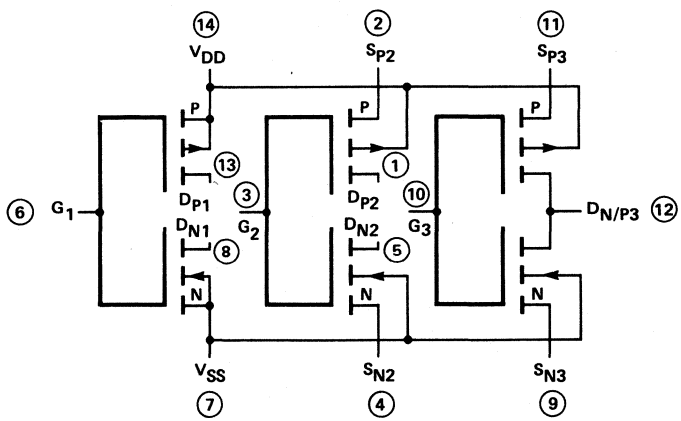


NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package,

PIN NAMES

S_{P2}, S_{P3}	Source Connection to Second and Third p-channel Transistors
D_{P1}, D_{P2}	Drain Connection from the First and Second p-channel Transistors
D_{N1}, D_{N2}	Drain Connection from the First and Second n-channel Transistors
S_{N2}, S_{N3}	Source Connection to the Second and Third n-channel Transistors
$D_{N/P3}$	Common Connection to the Third p-channel and n-channel Transistor Drains
G_1-G_3	Gate Connection to n- and p-channel Transistors 1, 2 and 3

LOGIC SYMBOL



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

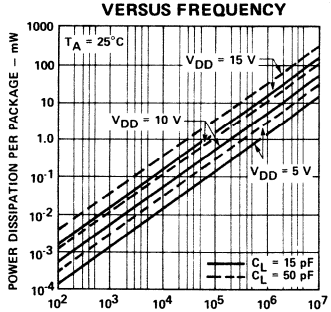
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

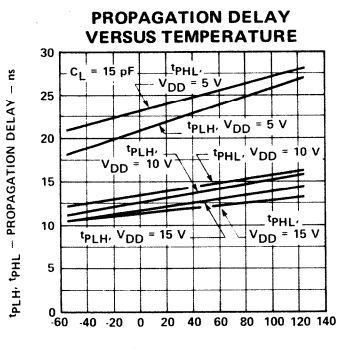
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		25	45		14	25		11		ns	C_L = 15 pF Input Transition Times ≤20 ns
t_{PHL}			25	45		14	25		11			
t_{TLH}	Output Transition Time		30	75		17	40		15	25	ns	
t_{THL}			30	75		17	40		15	25		
t_{PLH}	Propagation Delay		42	85		23	40		18		ns	C_L = 50 pF Input Transition Times ≤20 ns
t_{PHL}			42	85		23	40		18			
t_{TLH}	Output Transition Time		65	135		30	70		25	45	ns	
t_{THL}			65	135		30	70		25	45		

NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

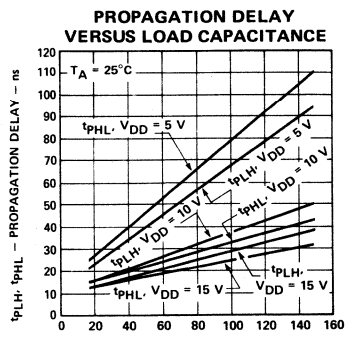
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



F4008/34008

4-BIT BINARY FULL ADDER

DESCRIPTION — The F4008 is a 4-Bit Binary Full Adder with two 4-bit Data Inputs (A_0-A_3, B_0-B_3); a Carry Input (C_0), four Sum Outputs (S_0-S_3) and a Carry Output (C_4).

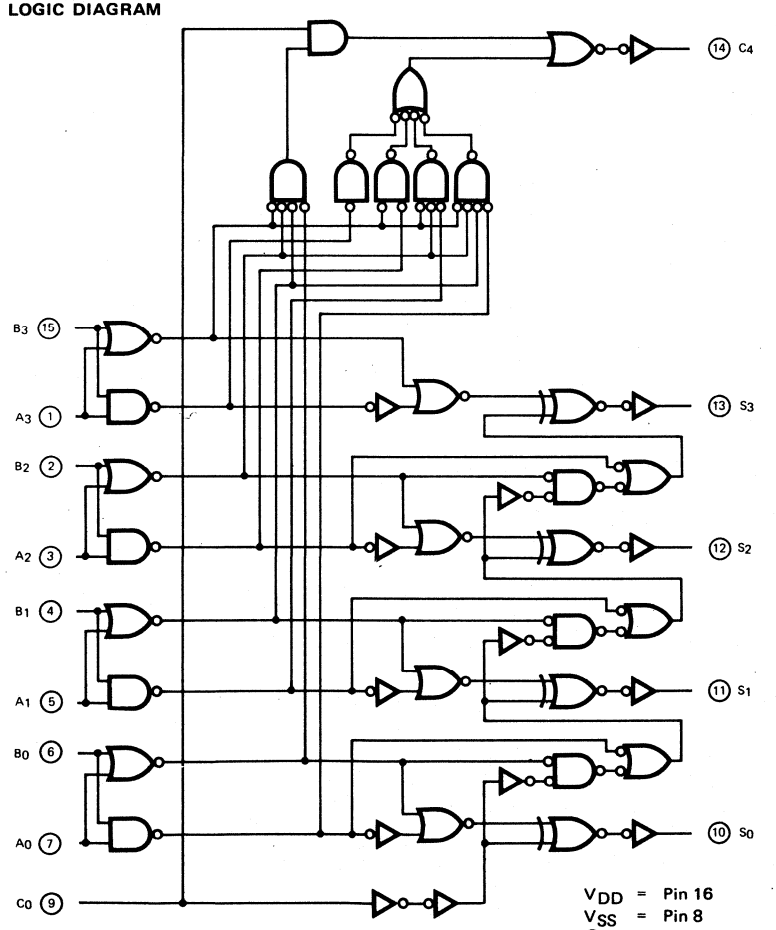
The F4008 uses full lookahead across 4-bits to generate the Carry Output (C_4). This minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

- **CARRY LOOKAHEAD BUFFERED OUTPUT**
- **EASILY CASCADED**

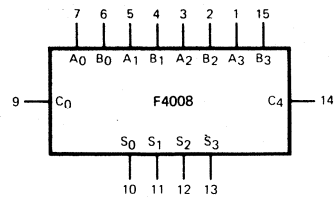
PIN NAMES

A_0-A_3, B_0-B_3	Data Inputs
C_0	Carry Input
S_0-S_3	Sum Outputs
C_4	Carry Output

LOGIC DIAGRAM

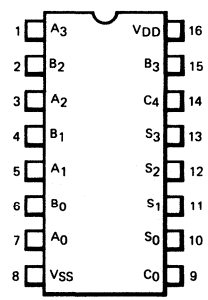


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP(TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2.0		μA	MIN, 25°C	
					300			600		120			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

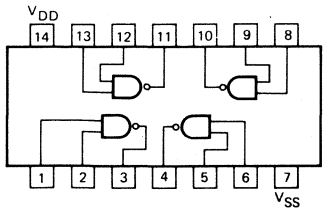
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A_n, B_n to S_n		210			85			62		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			210			85			62		ns	
t_{PLH}	Propagation Delay, A_n, B_n to C_4		125			57			45		ns	
t_{PHL}			125			57			45		ns	
t_{PLH}	Propagation Delay, C_0 to S_n		160			62			47		ns	
t_{PHL}			160			62			47		ns	
t_{PLH}	Propagation Delay, C_0 to C_4		57			25			20		ns	
t_{PHL}			57			25			20		ns	
t_{TLH}	Output Transition Time		30			17			13		ns	
t_{THL}			30			17			13		ns	
t_{PLH}	Propagation Delay, A_n, B_n to S_n		230			94			69		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			230			94			69		ns	
t_{PLH}	Propagation Delay, A_n, B_n to C_4		138			63			50		ns	
t_{PHL}			138			63			50		ns	
t_{PLH}	Propagation Delay, C_0 to S_n		178			69			52		ns	
t_{PHL}			178			69			52		ns	
t_{PLH}	Propagation Delay, C_0 to C_4		63			28			23		ns	
t_{PHL}			63			28			23		ns	
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4011 QUAD 2-INPUT NAND GATE • F4012 DUAL 4-INPUT NAND GATE

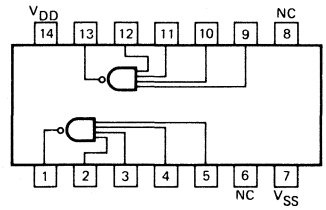
DESCRIPTION — These CMOS logic elements provide the positive input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

F4011
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-line Package.

F4012
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS (See Note 1)
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, F4011 only (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS (See Note 2)
t_{PLH}	Propagation Delay		40	75		20	40		15		ns	
t_{PHL}			40	75		20	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		25	75		10	40		8	25	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		25	75		10	40		8	25	ns	
t_{PLH}	Propagation Delay		60	110		25	60		20		ns	
t_{PHL}			60	110		25	60		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		60	135		30	70		20	45	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		60	135		30	70		20	45	ns	

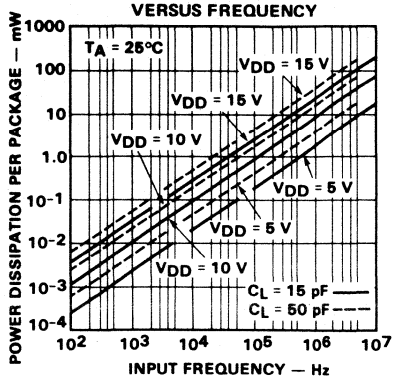
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, F4012 only

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS (See Note 2)
t_{PLH}	Propagation Delay		54	75		24	40		18		ns	
t_{PHL}			61	75		23	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		22	75		16	40		11	25	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		31	75		12	40		8	25	ns	
t_{PLH}	Propagation Delay		73	110		33	60		24		ns	
t_{PHL}			85	110		31	60		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		76	135		37	70		27	45	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		67	135		25	70		17	45	ns	

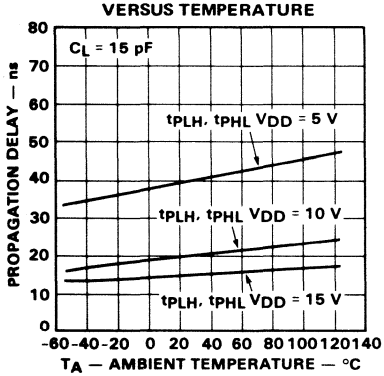
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

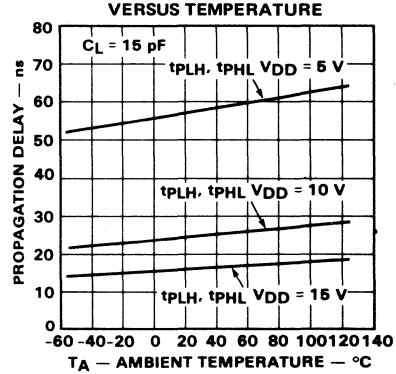
F4011 AND F4012
POWER DISSIPATION
VERSUS FREQUENCY



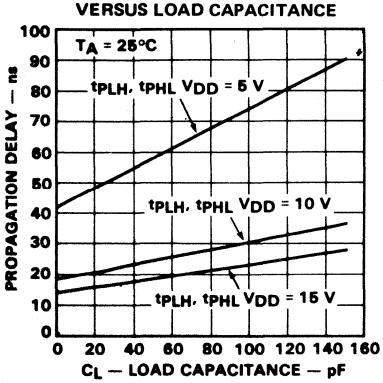
F4011
PROPAGATION DELAY
VERSUS TEMPERATURE



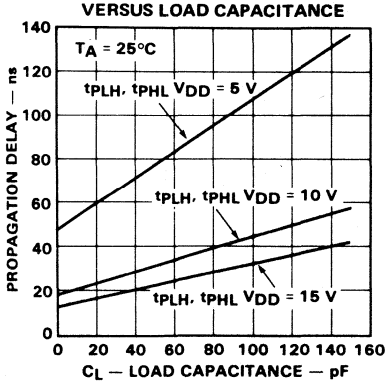
F4012
PROPAGATION DELAY
VERSUS TEMPERATURE



F4011
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



F4012
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



F4013/34013
DUAL D FLIP-FLOP

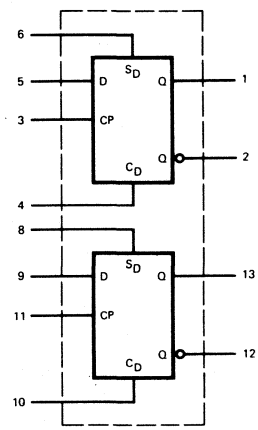
DESCRIPTION – The F4013 is a CMOS Dual D Flip-Flop which is edge-triggered and features independent Set Direct, Clear Direct, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct (C_D) and Set Direct (S_D) are independent and override the D or Clock inputs. The outputs are buffered for best system performance.

PIN NAMES

D	Data Input
CP	Clock Input (L→H Edge-Triggered)
S_D	Asynchronous Set Direct Input (Active HIGH)
C_D	Asynchronous Clear Direct Input (Active HIGH)
Q	True Output
$\overline{Q}$	Complement Output

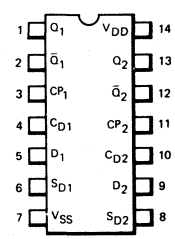
LOGIC SYMBOL

F4013



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4013 TRUTH TABLES

ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	L	L

SYNCHRONOUS INPUTS		OUTPUTS	
CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
⌐	L	L	H
⌐	H	H	L

Conditions: $S_D = C_D$ = LOW

L = LOW Level
H = HIGH Level
⌐ = Positive-Going Transition
X = Don't Care
Q_{n+1} = State After Clock Positive Transition

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

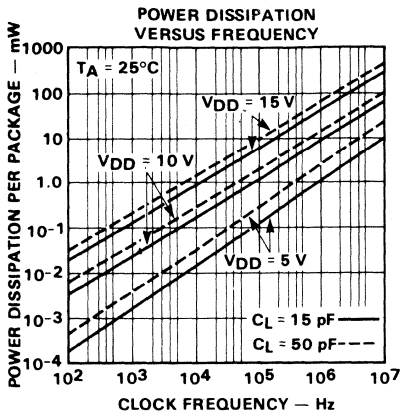
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

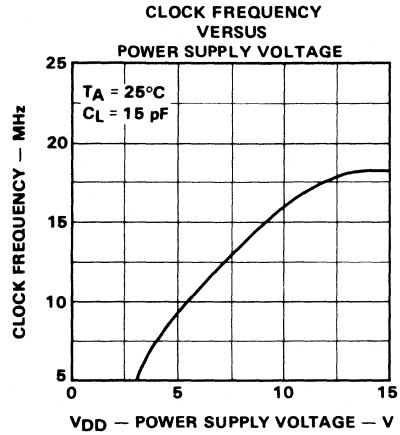
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 4)

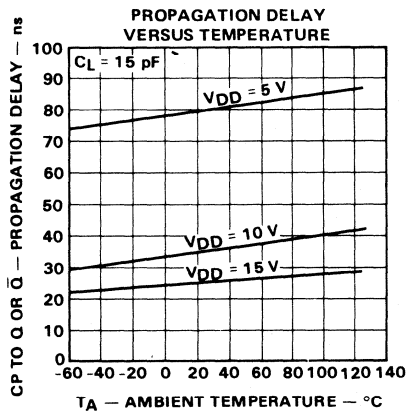
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q, $\overline{Q}$		80	150		35	66		25		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			80	150		35	66		25		ns	
t_{PLH}	Propagation Delay,		95	171		40	72		30		ns	
t_{PHL}	S_D or C_D to $\overline{Q}$		60	110		30	55		20		ns	
t_{PLH}	Propagation Delay,		100	170		45	80		30		ns	
t_{PHL}	S_D or C_D to Q		100	170		45	80		30		ns	
t_{TLH}	Output Transition		34	75		20	40		10	25	ns	
t_{THL}	Time		34	75		20	40		10	25	ns	
t_{PLH}	Propagation Delay, CP to Q, $\overline{Q}$		95	170		38	72		29		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			95	170		38	72		29		ns	
t_{PLH}	Propagation Delay,		130	220		45	90		32		ns	
t_{PHL}	S_D or C_D to $\overline{Q}$		75	135		35	65		20		ns	
t_{PLH}	Propagation Delay,		115	190		50	90		35		ns	
t_{PHL}	S_D or C_D to Q		115	190		50	90		35		ns	
t_{TLH}	Output Transition		60	135		30	70		20	45	ns	
t_{THL}	Time		60	135		30	70		20	45	ns	
t_s	Set-Up Time, Data to CP	80	30		40	15			8		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_h	Hold Time, Data to CP	0	-25		0	-12			-6		ns	
t_wCP(L)	Minimum Clock Pulse Width	100	55		55	30			18		ns	
t_w S_D(H)	Minimum S_D Pulse Width	60	30		30	15			10		ns	
t_w C_D(H)	Minimum C_D Pulse Width	60	30		30	15			10		ns	
t_{rec} S_D	Recovery Time for S_D	-20	-9		-10	-4			-2		ns	
t_{rec} C_D	Recovery Time for C_D	0	11		0	6			6		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	5	8		8	16					MHz	

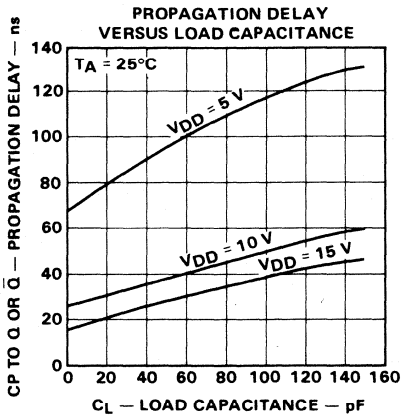
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

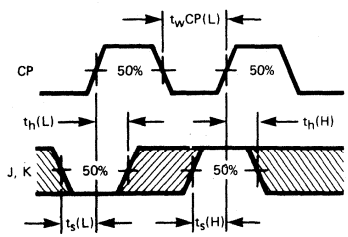




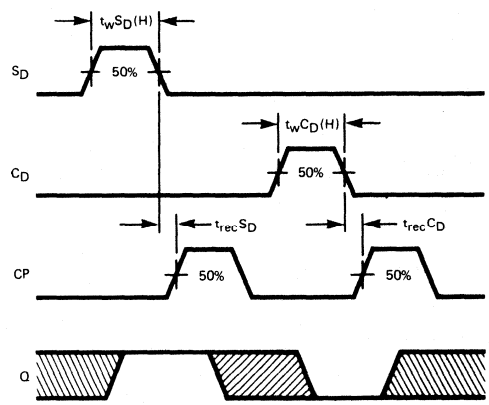




WAVEFORMS



SET-UP TIMES, HOLD TIMES,
AND MINIMUM CLOCK PULSE WIDTH



RECOVERY TIME FOR S_D, RECOVERY TIME FOR C_D,
MINIMUM S_D PULSE WIDTH, AND MINIMUM C_D PULSE WIDTH

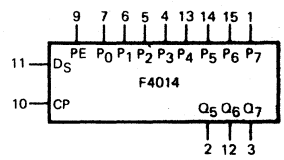
NOTE: Set-up Times and Hold Times are shown as positive values but may be specified as negative values.

F4014/34014
8-BIT SHIFT REGISTER

DESCRIPTION – The F4014 is a fully synchronous edge-triggered 8-Bit Shift Register with eight synchronous Parallel Inputs (P_0-P_7), a synchronous Serial Data Input (D_S), a synchronous Parallel Enable Input (PE), a LOW-to-HIGH edge-triggered Clock Input (CP) and Buffered Parallel Outputs from the last three stages (Q_5-Q_7).

Operation is synchronous and the device is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from the Parallel Inputs (P_0–P_7) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Input (D_S) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

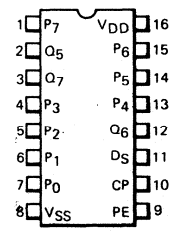
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **TYPICAL SHIFT FREQUENCY OF 14.7 MHz AT V_{DD} = 10 V**
- **PARALLEL OR SERIAL TO SERIAL DATA TRANSFER**
- **AVAILABLE OUTPUTS FROM THE LAST THREE STAGES**
- **FULLY SYNCHRONOUS**

CONNECTION DIAGRAM
DIP (TOP VIEW)

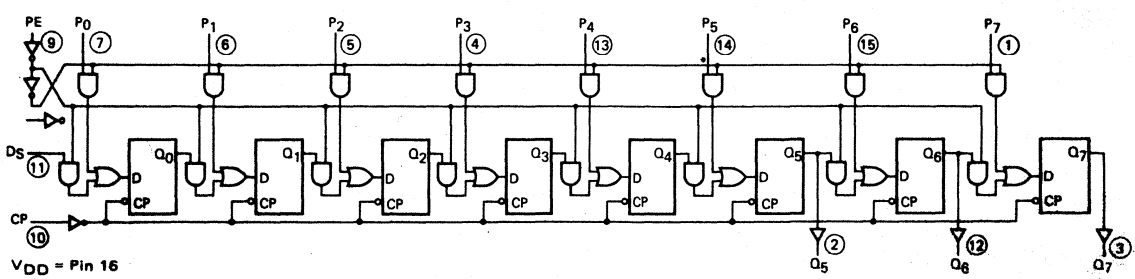


NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package

PIN NAMES

PE	Parallel Enable Input
P_0–P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5, Q_6, Q_7	Buffered Parallel Outputs from the Last Three Stages

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

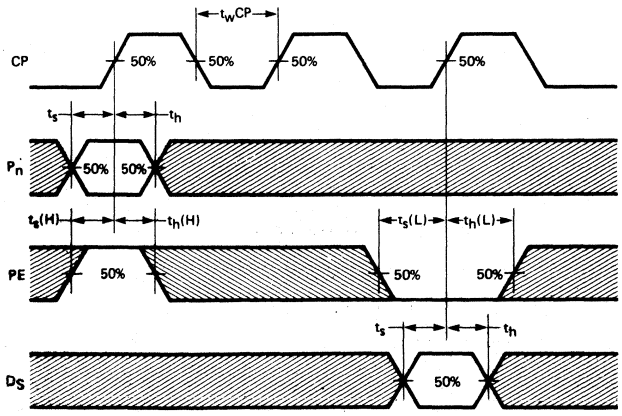
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHL}	Propagation Delay, CP to any Q		109			47			33		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			139			57			38		ns	
t_{TLH}	Output Transition Time		33			19			13		ns	
t_{THL}			37			19			15		ns	
t_{PLH}	Propagation Delay, CP to any Q		129			57			41		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			165			68			47		ns	
t_{TLH}	Output Transition Time		70			37			21		ns	
t_{THL}			77			34			21		ns	
t_wCP	CP Minimum Pulse Width		93			33			22		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_s	Set-Up Time PE to CP		118			44			29		ns	
t_h	Hold Time PE to CP		117			43			27		ns	
t_s	Set-Up Time D_S to CP		80			28			17		ns	
t_h	Hold Time D_S to CP		77			27			16		ns	
t_s	Set-Up Time P_n to CP		108			37			23		ns	
t_h	Hold Time P_n to CP		107			36			22		ns	
f_{MAX}	Max. Input Clock Frequency (Note 4)		5.8			14.7					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_W) do not vary with load capacitance.
4. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, PE TO CP, D_S TO CP, AND P_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4015/34015
DUAL 4-BIT STATIC SHIFT REGISTER

DESCRIPTION – The F4015 is a Dual Edge-Triggered 4-Bit Static Shift Register (Serial-to-Parallel Converter). Each Shift Register has a Serial Data Input (D), a Clock Input (CP), four fully buffered parallel Outputs (Q_0–Q_3) and an overriding asynchronous Master Reset Input (MR).

Information present on the serial Data Input (D) is shifted into the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

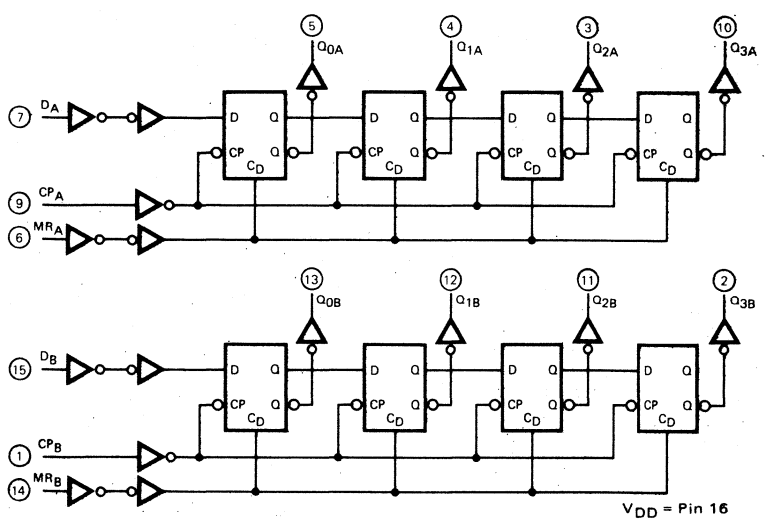
A HIGH on the Master Reset Input (MR) clears the register and forces the Outputs (Q_0 - Q_3) LOW, independent of the Clock and Data Inputs (CP and D).

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **SERIAL-TO-PARALLEL DATA TRANSFER**
- **FULLY BUFFERED OUTPUTS FROM EACH STAGE**

PIN NAMES

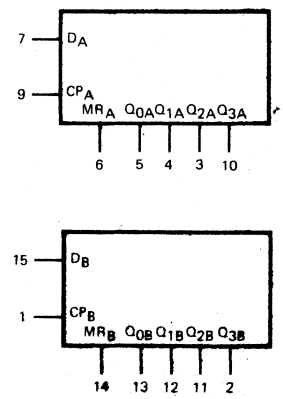
D_A, D_B	Serial Data Input
MR_A, MR_B	Master Reset Input (Active HIGH)
CP_A, CP_B	Clock Input (L→H Edge-Triggered)
Q_{0A}, Q_{1A}, Q_{2A}, Q_{3A}	Parallel Outputs
Q_{0B}, Q_{1B}, Q_{2B}, Q_{3B}	Parallel Outputs

LOGIC DIAGRAM

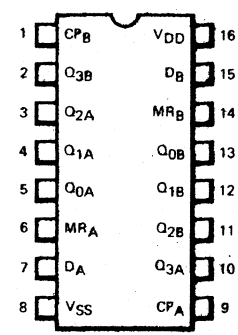


LOGIC SYMBOL

F4015



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					100			200		40			MAX	
		XM			1			2		0.4		µA	MIN, 25°C	
					30			60		12			MAX	

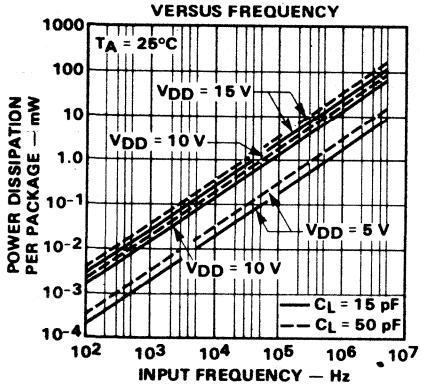
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q		140	250		75	135		45		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			140	250		75	135		45		ns	
t_{PHL}	Propagation Delay, MR to Q		150	300		85	150		60		ns	
t_{TLH}	Output Transition Time		50	100		25	60		20	40	ns	
t_{THL}			50	100		25	60		20	40	ns	
t_{PLH}	Propagation Delay, CP to Q		165	300		85	150		50		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			165	300		85	150		50		ns	
t_{PHL}	Propagation Delay, MR to Q		180	325		90	160		60		ns	
t_{TLH}	Output Transition Time		85	150		45	85		30	50	ns	
t_{THL}			85	150		45	85		30	50	ns	
t_s	Set-Up Time, D to CP	150	70		50	30			25		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_h	Hold Time, D to CP	0	-5		0	-20			-10		ns	
t_WCP(L)	Minimum Clock Pulse Width	120	60		70	35			25		ns	
t_WMR(H)	Minimum MR Pulse Width	75	40		45	25			20		ns	
t_{rec}	MR Recovery Time	300	160		120	60			45		ns	
f_{MAX}	Maximum CP Frequency (Note 4)	4	8		7	14					MHz	

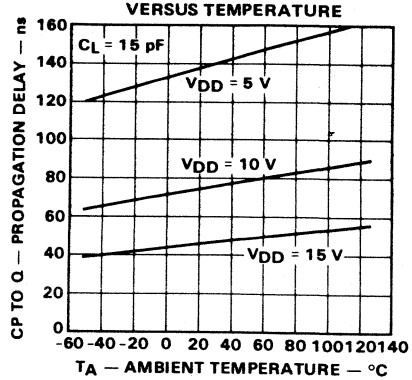
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_W) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 µs.

TYPICAL ELECTRICAL CHARACTERISTICS

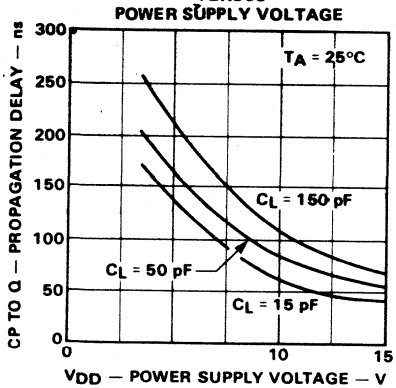
POWER DISSIPATION VERSUS FREQUENCY



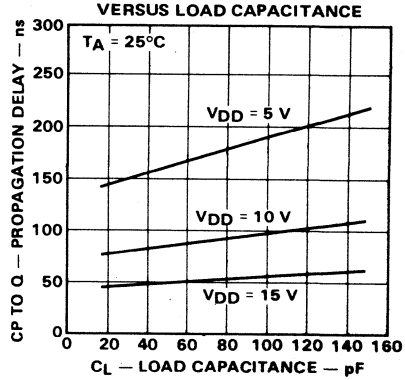
PROPAGATION DELAY VERSUS TEMPERATURE



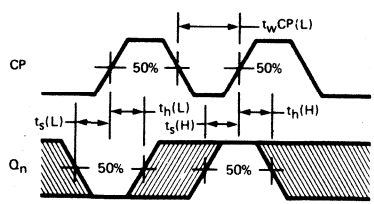
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



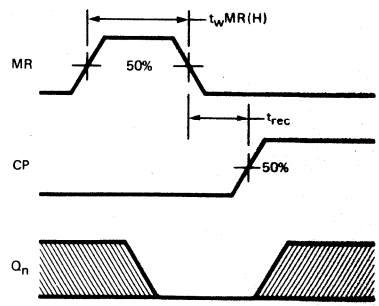
SWITCHING WAVEFORMS



SET-UP TIMES, HOLD TIMES AND MINIMUM CLOCK PULSE WIDTH

NOTE:

t_s and t_h are shown as positive values but may be specified as negative values.



RECOVERY TIME FOR MR AND MINIMUM MR PULSE WIDTH

F4016/34016
QUAD BILATERAL SWITCHES

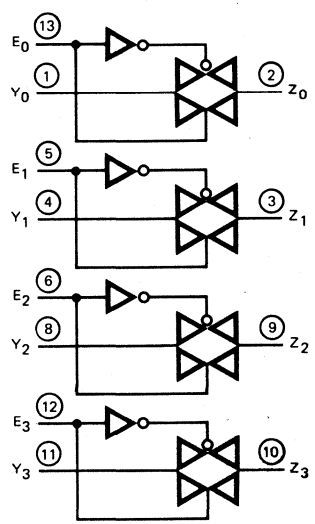
DESCRIPTION – The F4016 has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch and establishes a high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

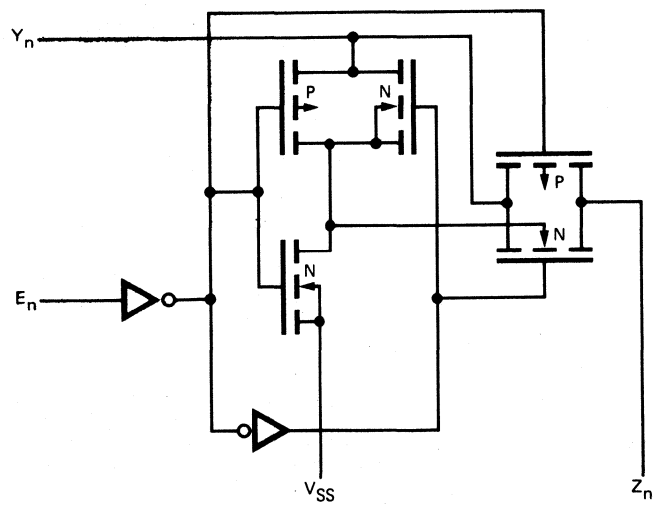
E_0 - E_3	Enable Inputs
Y_0 - Y_3	Input/Output Terminals
Z_0 - Z_3	Input/Output Terminals

LOGIC SYMBOL

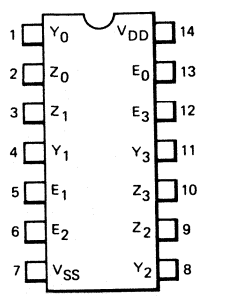


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A F4016)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS	
R_{ON}	ON Resistance	XC			610			610			370	Ω	MIN	$V_{is} = V_{DD}$	R_L = 10 kΩ, $E_n = V_{DD}$
					660			660			400		25°C		
					840			840			520		MAX		
								610			370	Ω	MIN	$V_{is} = V_{SS}$ +0.25 V	
								660			400		25°C		
								840			520		MAX		
					1900							Ω	MIN	V_{is} = 2.5 V	
					2000								25°C		
					2380								MAX		
								1750				Ω	MIN	V_{is} = 5.6 V	
								1800					25°C		
								2360					MAX		
											775	Ω	MIN	V_{IN} = 9.3 V	
											800		25°C		
											1020		MAX		
		XM						600			360	Ω	MIN	$V_{is} = V_{DD}$	R_L = 10 kΩ, $E_n = V_{DD}$
								660			400		25°C		
								960			600		MAX		
								600			360	Ω	MIN	$V_{is} = V_{SS}$ +0.25 V	
								660			400		25°C		
								960			600		MAX		
					1870							Ω	MIN	V_{is} = 2.5 V	
					2000								25°C		
					2600								MAX		
								1700				Ω	MIN	V_{is} = 5.6 V	
								1800					25°C		
								2000					MAX		
											750	Ω	MIN	V_{is} = 9.3 V	
											800		25°C		
											1200		MAX		
ΔR_{ON}	"Δ" ON Resistance Between Any Two Switches						15			10		Ω	25°C	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{DD}$, R_L = 10 kΩ	
I_Z	OFF State Leakage Current, Any Y to Z							125			200	nA	25°C	$V_{is} = V_{DD}$ or V_{SS}, $E_n = V_{SS}$	
I_{DD}	Quiescent Power Supply Current	XC			0.25			0.5		0.1		μA	MIN, 25°C	All inputs common and at V_{DD} or V_{SS}	
					7			8		1.6			MAX		
		XM			0.25			0.5		0.1		μA	MIN, 25°C		
					25			30		6			MAX		

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		4 3			1.5 1.5			1 1		ns ns	R_L = 10 kΩ, E_n = V_{DD} C_L = 15 pF Input Transition Times ≤ 20 ns V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		26 26			14 14			10 10		ns ns	E_n = V_{DD} (square wave) R_L = 10 kΩ, C_L = 15 pF Input Transition Times ≤ 20 ns V_{is} = V_{DD}
t_{PLZ} t_{PHZ}	Output Disable Time		160 160			170 170			182 182		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8			3 4			2 2.5		ns ns	R_L = 10 kΩ, E_n = V_{DD} C_L = 50 pF Input Transition Times ≤ 20 ns V_{is} = V_{DD} (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32			16 16			13 13		ns ns	R_L = 10 kΩ, C_L = 50 pF Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{is} = V_{DD}
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns ns	
	Distortion, Sine Wave Response		0.31			0.31			0.31		%	R_L = 10 kΩ, C_L = 15 pF Input Frequency = 1 kHz E_n = V_{DD} V_{is} = $V_{DD}/2$ (sine wave)
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ, E_A = V_{DD}, E_B = V_{SS} V_{is} = $V_{DD}/2$ sine wave at − 50 dB, 20 Log_{10} [V_{os} (B)/V_{is} (A)] = −50 dB
	Crosstalk, Enable Input to Output					50					mV	$R_{L(OUT)}$ = 10 kΩ, $R_{L(IN)}$ = 1 kΩ Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ E_n = V_{SS}, V_{is} = $V_{DD}/2$ sine wave 20 Log_{10} (V_{os}/V_{is}) = −50 dB
	ON State Frequency Response					90					MHz	R_L = 1 kΩ V_{is} = $V_{DD}/2$ sine wave E_n = V_{DD}, 20 Log_{10} (V_{os}/V_{is}) = −3 dB
f_{MAX}	Enable Input Frequency (Note 4)					10					MHz	R_L = 1 kΩ, C_L = 15 pF Input Transition Times ≤ 20 ns E_n = V_{DD} (square wave) V_{is} = V_{DD}

NOTES:
1. Additional DC Characteristics for the Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
3. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.

F4017/34017
5-STAGE JOHNSON COUNTER

DESCRIPTION – The F4017 is a 5-Stage Johnson Decade Counter with ten glitch free decoded active HIGH Outputs (O_0–O_9), an active LOW Output from the most significant flip-flop ($\overline{Q_{5-9}}$), active HIGH and active LOW Clock Inputs (CP_0, $\overline{CP_1}$) and an overriding asynchronous Master Reset Input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP_1}$ is LOW or a HIGH-to-LOW transition at $\overline{CP_1}$ while CP_0 is HIGH (see Functional Truth Table). When cascading F4017 counters, the $\overline{Q_{5-9}}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next F4017.

A HIGH on the Master Reset Input (MR) resets the counter to zero (O_0 = $\overline{Q_{5-9}}$ = HIGH, O_1–O_9 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP_1}$).

- **TYPICAL COUNT FREQUENCY OF 13.8 MHz AT V_{DD} = 10 V**
- **ACTIVE HIGH DECODED OUTPUTS**
- **TRIGGERS ON EITHER A HIGH-TO-LOW OR LOW-TO-HIGH TRANSITION**
- **CASCADABLE**

PIN NAMES

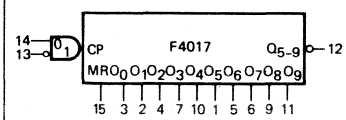
CP_0	Clock Input (L→H Triggered)
$\overline{CP_1}$	Clock Input (H→L Triggered)
MR	Master Reset Input
O_0–O_9	Decoded Outputs
$\overline{Q_{5-9}}$	Carry Output (Active LOW)

FUNCTIONAL TRUTH TABLE

MR	CP_0	$\overline{CP_1}$	OPERATION
H	X	X	$O_0 = \overline{Q_{5-9}}$ = H; O_1–O_9 = L
L	H	H→L	Counter Advances
L	L→H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L→H	No Change
L	H→L	L	No Change

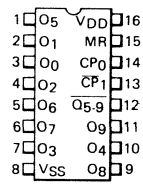
H = HIGH Level
L = LOW Level
L→H = LOW-to-HIGH Transition
H→L = HIGH-to LOW Transition
X = Don't Care

LOGIC SYMBOL



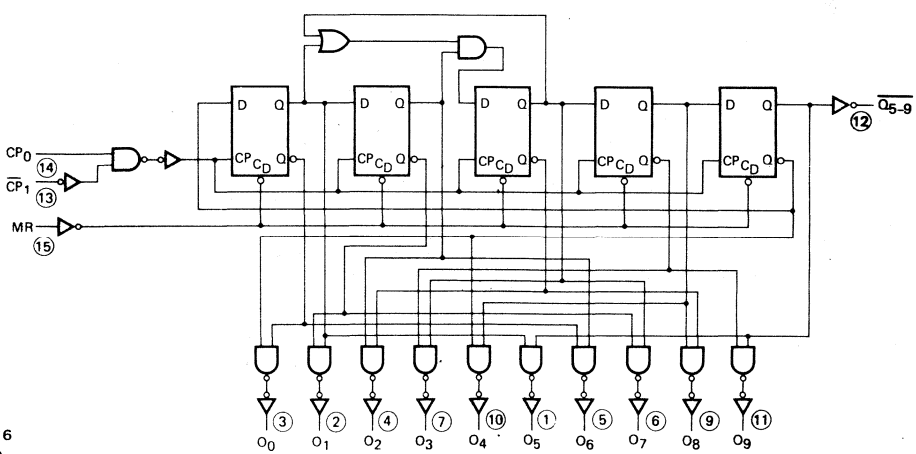
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

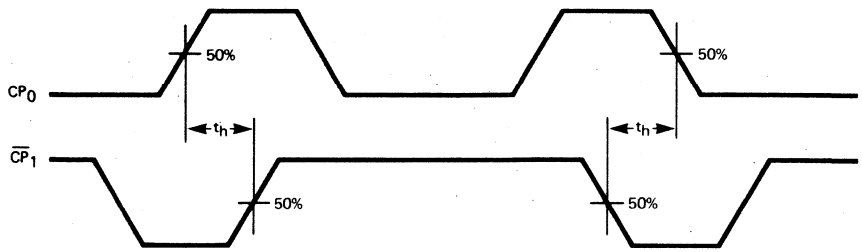
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP_0 or $\overline{CP}_1$ to O_n		262 197	650 500		104 86	260 215		76 61		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP_0 or $\overline{CP}_1$ to $\overline{Q}_{5-9}$		189 240	475 600		80 96	200 225		57 67		ns ns	
t_{PHL}	Propagation Delay, MR to O_n		151	380		62	150		45		ns	
t_{PLH}	Propagation Delay, MR to $\overline{Q}_{5-9}$		102	250		42	105		34		ns	
t_{TLH} t_{THL}	Output Transition Time		32 27	75 75		16 13	40 40		13 10	25 25	ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP_0 or $\overline{CP}_1$ to O_n		278 226	700 550		114 94	285 240		82 67		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP_0 or $\overline{CP}_1$ to $\overline{Q}_{5-9}$		205 261	525 650		87 105	225 250		63 73		ns ns	
t_{PHL}	Propagation Delay, MR to O_n		170	430		80	175		52		ns	
t_{PLH}	Propagation Delay, MR to $\overline{Q}_{5-9}$		125	300		65	130		40		ns	
t_{TLH} t_{THL}	Output Transition Time		59 63	135 135		31 26	70 70		23 19	45 45	ns ns	
t_wCP	Min. CP_0 or $\overline{CP}_1$ Pulse Width	200	85		70	37			28		ns	C_L = 15 pF Input Transition Times 20 ns
t_wMR	Minimum MR Pulse Width	130	52		55	22			18		ns	
t_{rec}	MR Recovery Time	50	16		25	6			3		ns	
t_h	Hold Time, CP_0 to $\overline{CP}_1$	200	90		90	39			26		ns	
t_h	Hold Time, $\overline{CP}_1$ to CP_0	200	89		90	39			22		ns	
f_{MAX}	Input Count Frequency (Note 4)	2.5	5.8		7	13.8					MHz	

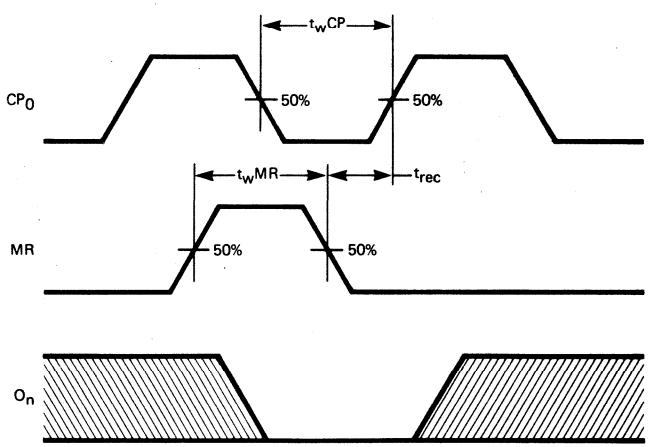
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to either Clock Input (CO_0 or $\overline{CP}_1$) be less than 15 μs.

SWITCHING WAVEFORMS



HOLD TIMES, CP_0 TO $\overline{CP}_1$ AND $\overline{CP}_1$ TO CP_0

Hold Times are shown as positive values, but may be specified as negative values.



MINIMUM PULSE WIDTHS FOR CP AND MR AND RECOVERY TIME FOR MR

CONDITIONS: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW-to-HIGH transition. t_wCP and t_{rec} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH-to-LOW transition.

F4018/34018

PRESETTABLE DIVIDE-BY-N COUNTER

DESCRIPTION — The F4018 is a 5-Stage Johnson Counter with a Clock Input (CP), a Data Input (D), an asynchronous Parallel Load Input (PL), five Parallel Inputs (P_0–P_4), five active LOW buffered Outputs ($\overline{Q}_0$–$\overline{Q}_4$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0–P_4) is asynchronously loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Data (D) Inputs. Data present in the counter is stored on the HIGH-to-LOW transition of the Parallel Load Input (PL). When the Parallel Load Input is LOW, the counter advances on the LOW-to-HIGH transition of the Clock Input (CP). By connecting the Outputs ($\overline{Q}_0$–$\overline{Q}_4$) to the Data Input (D), the counter operates as a divide-by-n counter ($2 \leq n \leq 10$); see below.

A HIGH on the Master Reset Input (MR) resets the counter ($\overline{Q}_0$–$\overline{Q}_4$ = HIGH) independent of all other inputs.

- **ASYNCHRONOUS MASTER RESET INPUT (ACTIVE HIGH)**
- **ACTIVE LOW FULLY BUFFERED DECODED OUTPUTS**
- **DIVIDE-BY-N WITH $2 \leq N \leq 10$**
- **CLOCK INPUT L→H EDGE-TRIGGERED**
- **ASYNCHRONOUS PARALLEL LOAD INPUT (ACTIVE HIGH)**

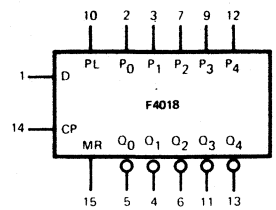
PIN NAMES

PL	Parallel Load Input
P_0–P_4	Parallel Inputs
D	Data Input
CP	Clock Input (L→H Edge-Triggered)
MR	Master Reset Input
$\overline{Q}_0$–$\overline{Q}_4$	Buffered Outputs (Active LOW)

DIVIDE-BY-N MODE SELECTION

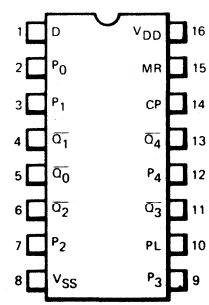
DIVIDE BY	D INPUT
2	$\overline{Q}_0$
3	$\overline{Q}_0 \cdot \overline{Q}_1$
4	$\overline{Q}_1$
5	$\overline{Q}_1 \cdot \overline{Q}_2$
6	$\overline{Q}_2$
7	$\overline{Q}_2 \cdot \overline{Q}_3$
8	$\overline{Q}_3$
9	$\overline{Q}_3 \cdot \overline{Q}_4$
10	$\overline{Q}_4$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4019/34019
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION – The F4019 provides four multiplexing circuits with common selection inputs; each circuit contains two inputs and one output. It may be used to select four bits of information from one of two sources. The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, output (Z_n) is the logical OR of the A_n and B_n inputs ($Z_n = A_n + B_n$). When S_A and S_B are LOW, output (Z_n) is LOW independent of the multiplexer inputs (A_n and B_n). The F4019 cannot be used to multiplex analog signals. The outputs utilize standard buffers for best performance.

PIN NAMES

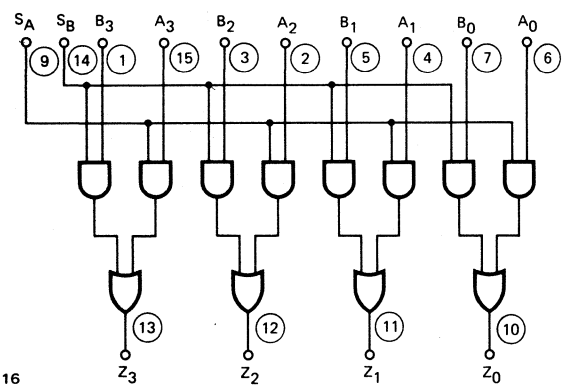
S_A, S_B	Select Inputs (Active HIGH)
$A_0 - A_3$, $B_0 - B_3$	Multiplexer Inputs
$Z_0 - Z_3$	Multiplexer Outputs

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S_A	S_B	A_n	B_n	Z_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

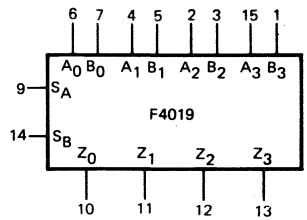
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

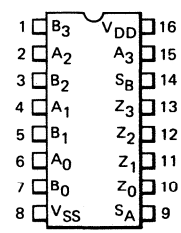
$Z_n = S_A A_n + S_B B_n$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			30			60		12		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		24			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					100			200		40			MAX	

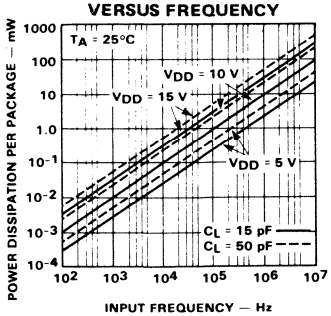
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		50	100		20	45		16		ns	
t_{PHL}	S_A, S_B, A_n or B_n to Z_n		50	110		25	55		20		ns	C_L = 15 pF
t_{TLH}	Output Transition		40	75		20	40		15	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		45	75		22	40		15	25	ns	
t_{PLH}	Propagation Delay,		75	150		35	70		24		ns	
t_{PHL}	S_A, S_B, A_n or B_n to Z_n		85	160		37	75		29		ns	C_L = 50 pF
t_{TLH}	Output Transition		80	135		42	70		32	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		90	135		40	70		30	45	ns	

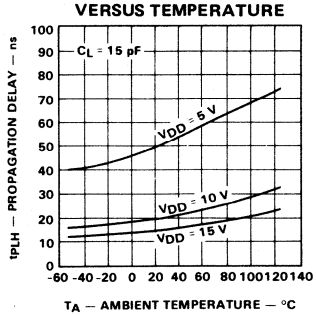
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

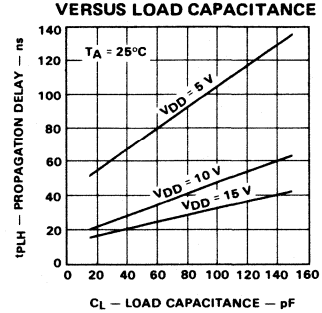
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



F4020/34020
14-STAGE BINARY COUNTER

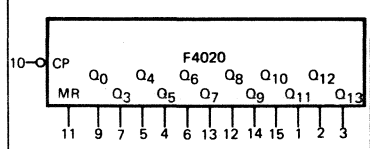
DESCRIPTION – The F4020 is a 14-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and twelve fully buffered Outputs (Q_0, Q_3–Q_{13}). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0, Q_3–Q_{13}) LOW, independent of the Clock Input ($\overline{CP}$).

- **25 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **COMMON ASYNCHRONOUS MASTER RESET**
- **FULLY BUFFERED OUTPUTS FROM THE FIRST STAGE AND THE LAST ELEVEN STAGES**

PIN NAMES

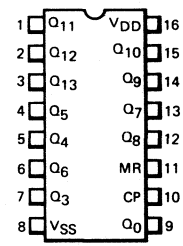
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input (Active HIGH)
Q_0, Q_3–Q_{13}	Parallel Outputs

LOGIC SYMBOL



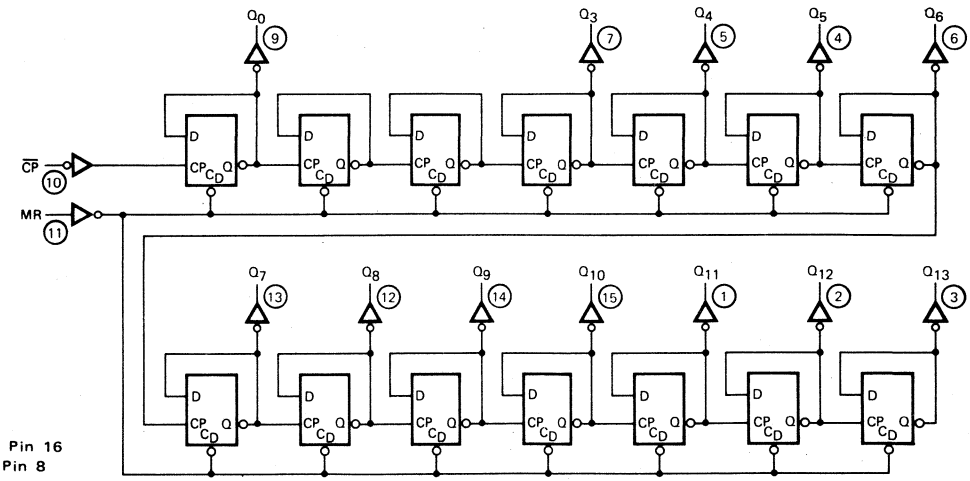
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		300			MAX	

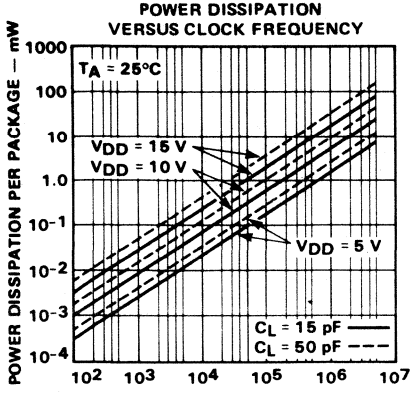
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		110	220		45	90		30		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			85	170		37	75		25		ns	
t_{PHL}	Propagation Delay, MR to Q_n		150	300		65	130		43		ns	
t_{TLH}	Output Transition Time		30	75		13	40		10	25	ns	
t_{THL}			30	75		13	40		10	25	ns	
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		130	260		55	110		37		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			110	220		45	90		33		ns	
t_{PHL}	Propagation Delay, MR to Q_n		180	360		75	150		50		ns	
t_{TLH}	Output Transition Time		65	135		35	70		25	45	ns	
t_{THL}			65	135		35	70		25	45	ns	
$t_w\overline{CP}(H)$	Minimum Clock Pulse Width	100	50		40	20			16		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
$t_wMR(H)$	Minimum MR Pulse Width	140	70		55	27			20		ns	
t_{rec}	Recovery Time for MR	85	43		35	17			12		ns	
f_{MAX}	Input Clock Frequency (Note 3)	5	10		12	25					MHz	

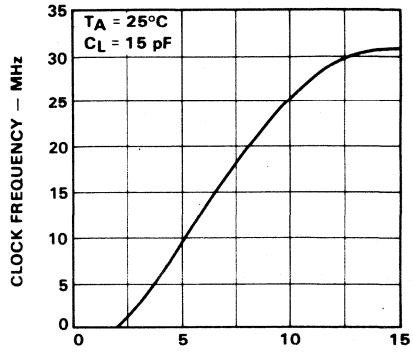
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

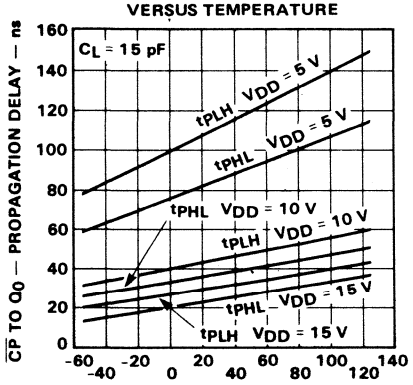
POWER DISSIPATION VERSUS CLOCK FREQUENCY



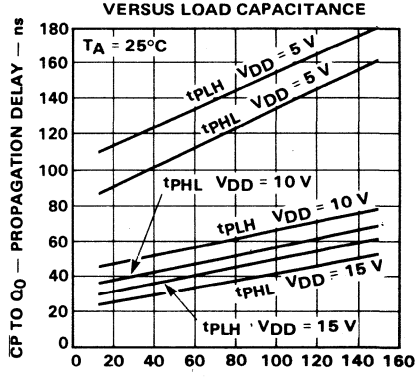
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



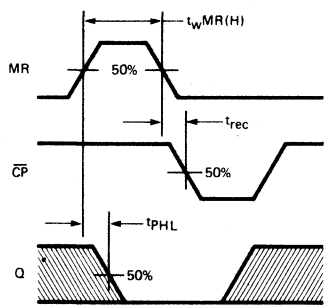
PROPAGATION DELAY VERSUS TEMPERATURE



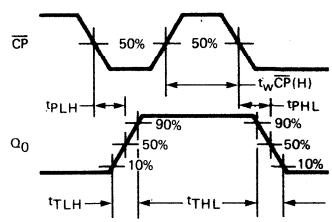
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



PROPAGATION DELAY MASTER RESET TO OUTPUT, MINIMUM MASTER RESET PULSE WIDTH AND RECOVERY TIME FOR MASTER RESET



PROPAGATION DELAY CLOCK TO OUTPUT Q_0, OUTPUT TRANSITION TIMES AND MINIMUM CLOCK PULSE WIDTH

F4021/34021
8-BIT SHIFT REGISTER

DESCRIPTION – The F4021 is an edge-triggered 8-Bit Shift Register (Parallel-to-Serial Converter) with a synchronous Serial Data Input (D_S), a Clock Input (CP), an asynchronous active HIGH Parallel Load Input (PL), eight asynchronous Parallel Data Inputs (P_0–P_7) and Buffered Parallel Outputs from the last three stages (Q_5–Q_7).

Information on the Parallel Data Inputs (P_0–P_7) is asynchronously loaded into the register while the Parallel Load Input (PL) is HIGH, independent of the Clock (CP) and Serial Data (D_S) inputs. Data present in the register is stored on the HIGH-to-LOW transition of the Parallel Load Input.(PL).

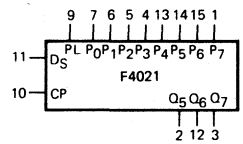
When the Parallel Load'Input is LOW, data on the Serial Data Input (D_S) is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP).

- **TYPICAL SHIFT FREQUENCY OF 18.1 MHz AT V_{DD} = 10 V**
- **PARALLEL-TO-SERIAL DATA TRANSFER**
- **BUFFERED OUTPUTS AVAILABLE LAST THREE STAGES**
- **CLOCK INPUT IS L → H EDGE-TRIGGERED**

PIN NAMES

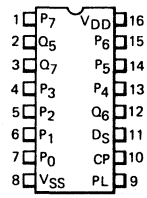
PL	Parallel Load Input
P_0–P_7	Parallel Data Inputs
D_S	Serial Data Input
CP	Clock Input (L→H Edge-Triggered)
Q_5–Q_7	Buffered Parallel Outputs from the Last Three Stages

LOGIC SYMBOL



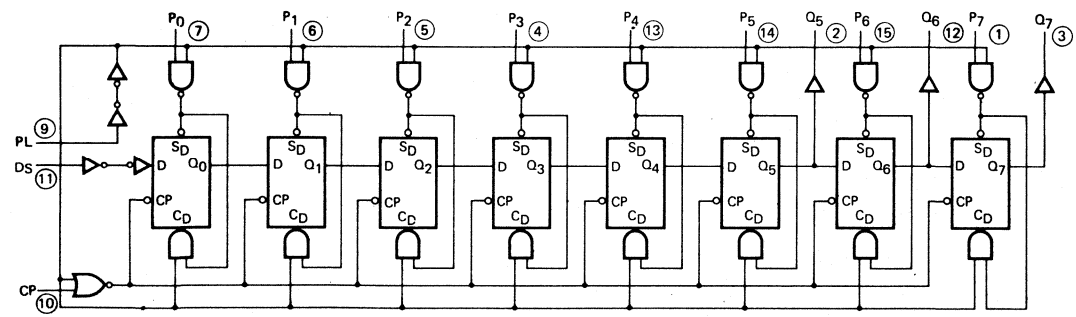
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

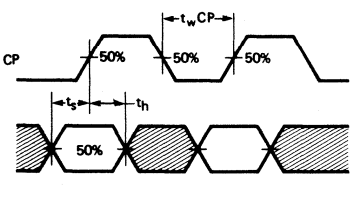
SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

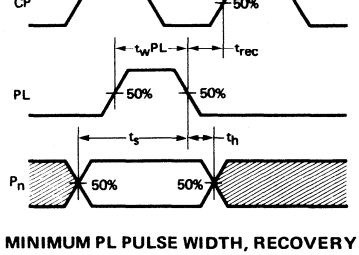
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, CP to Q_n		119			51			34		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			161			64			43		ns	
t_{PLH}	Propagation Delay, PL to Q_n		172			70			48		ns	
t_{PHL}			150			96			66		ns	
t_{TLH}	Output Transition Time		28			15			10		ns	
t_{THL}			32			14			9		ns	
t_{PLH}	Propagation Delay, CP to Q_n		134			59			40		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			184			74			49		ns	
t_{PLH}	Propagation Delay, PL to Q_n		188			78			54		ns	
t_{PHL}			274			105			72		ns	
t_{TLH}	Output Transition Time		58			31			22		ns	
t_{THL}			69			27			22		ns	
t_wCP	CP Minimum Pulse Width		61			21			14		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_wPL	PL Minimum Pulse Width		67			24			16		ns	
t_{rec}	PL Recovery Time		71			28			21		ns	
t_s	Set-Up Time D_S to CP		51			16			12		ns	
t_h	Hold Time D_S to CP		49			15			11		ns	
t_s	Set-Up Time P_n to PL		78			28			18		ns	
t_h	Hold Time, P_n to PL		72			26			16		ns	
f_{MAX}	Shift Frequency (Note 4)		7.8			18.1					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
4. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D_S TO CP



MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4022/34022

4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

DESCRIPTION – The F4022 is a 4-Stage Divide-by-8 Johnson Counter with eight glitch free active HIGH Decoded Outputs (O_0–O_7), an active LOW Output from the most significant flip-flop (Q_{4-7}), an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP_1}$) and an overriding asynchronous Master Reset Input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\overline{CP_1}$ is LOW or a HIGH-to-LOW transition at $\overline{CP_1}$ while CP_0 is HIGH (see Functional Truth Table). When cascading the counters, the $\overline{Q_{4-7}}$ Output (which is LOW while the counter is in states 4, 5, 6 and 7) can be used to drive the CP_0 Input of the next F4022. A HIGH on the Master Reset Input (MR) resets the counter to Zero ($O_0 = \overline{Q_{4-7}}$ = HIGH, $O_1 - O_7$ = LOW) independent of the Clock Inputs (CP_0, $\overline{CP_1}$).

- **CLOCK EDGE-TRIGGERED ON EITHER A LOW-TO-HIGH TRANSITION OR A HIGH-TO-LOW TRANSITION**
- **BUFFERED CARRY OUTPUT ($\overline{Q_{4-7}}$) AVAILABLE FOR CASCADING**
- **BUFFERED FULLY DECODED OUTPUTS**

PIN NAMES

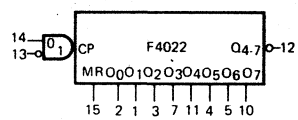
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP_1}$	Clock Input (H→L Edge-Triggered)
MR	Master Reset Input
O_0–O_7	Decoded Outputs
$\overline{Q_{4-7}}$	Carry Output (Active LOW)

FUNCTIONAL TRUTH TABLE

MR	CP_0	$\overline{CP_1}$	OPERATION
H	X	X	$O_0 = \overline{Q_{4-7}}$ = H; O_1–O_7 = L
L	H	H→L	Counter Advances
L	L→H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L→H	No Change
L	H→L	L	No Change

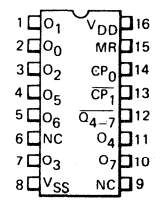
H = HIGH Level
L = LOW Level
L→H = LOW-to-HIGH Transition
H→L = HIGH-to-LOW Transition
X = Don't Care

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 6, 9

CONNECTION DIAGRAM
DIP(TOP VIEW)

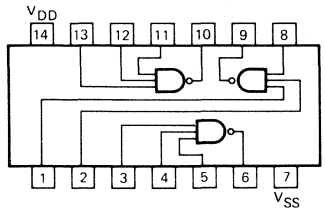


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

TRIPLE 3-INPUT NAND GATE

DESCRIPTION — This CMOS logic element provides a 3-input positive NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

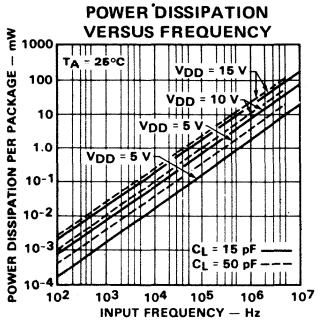
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		35	75		20	40		15		ns	
t_{PHL}			35	75		20	40		9		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		19	75		9	40		6	25	ns	Input Transition Times ≤ 20 ns
t_{THL}			19	75		7	40		5	25	ns	
t_{PLH}	Propagation Delay		45	110		25	60		19		ns	
t_{PHL}			51	110		25	60		12		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		45	135		18	70		17	45	ns	Input Transition Times ≤ 20 ns
t_{THL}			45	135		18	70		12	45	ns	

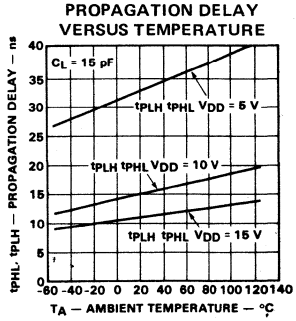
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

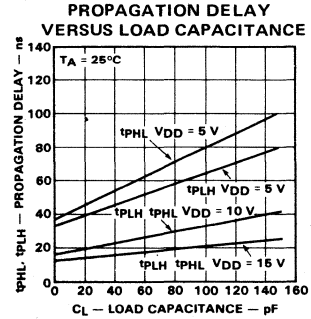
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



F4024/34024
7-STAGE BINARY COUNTER

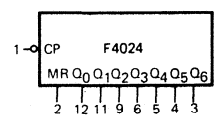
DESCRIPTION – The F4024 is a 7-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and seven fully Buffered Parallel Outputs (Q_0-Q_6). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0-Q_6) LOW, independent of the Clock Input ($\overline{CP}$).

- **TYPICAL COUNT FREQUENCY OF 30 MHz AT V_{DD} = 10 V**
- **CLOCK TRIGGERED ON THE HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **OUTPUTS AVAILABLE FROM ALL SEVEN STAGES**

PIN NAMES

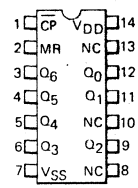
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input
Q_0-Q_6	Buffered Parallel Outputs

LOGIC SYMBOL

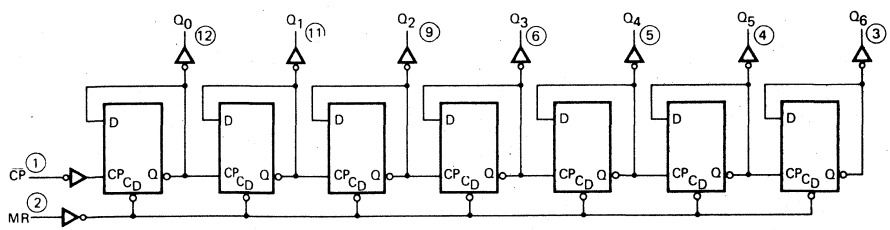


V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10 and 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 8, 10 and 13
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

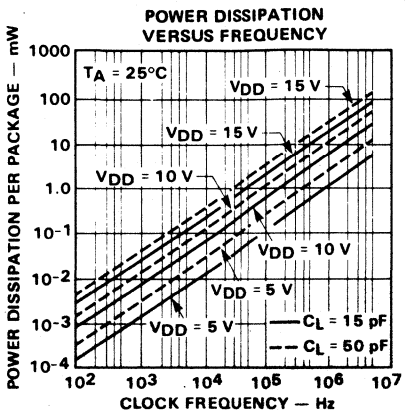
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

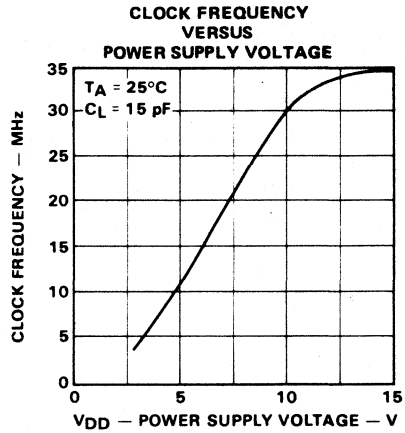
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

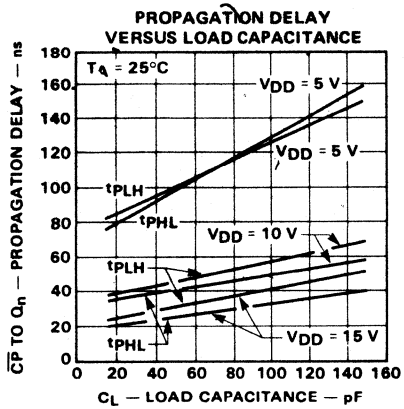
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		82	165		37	75		23		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			75	150		35	70		20		ns	
t_{PHL}	Propagation Delay, MR to Q_n		105	210		42	85		30		ns	
t_{TLH}	Output Transition Time		25	75		13	40		10	25	ns	
t_{THL}			25	75		13	40		10	25	ns	
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		100	200		45	90		30		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			97	195		40	80		25		ns	
t_{PHL}	Propagation Delay, MR to Q_n		130	260		50	100		35		ns	
t_{TLH}	Output Transition Time		60	130		30	70		25	45	ns	
t_{THL}			60	130		30	70		25	45	ns	
$t_w\overline{CP}$	$\overline{CP}$ Minimum Pulse Width	90	45		35	17			13		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_wMR	MR Minimum Pulse Width	80	40		30	15			12		ns	
t_{rec}	MR Recovery Time	60	30		25	12			9		ns	
f_{MAX}	Input Count Frequency (Note 4)	6	12		15	30					MHz	

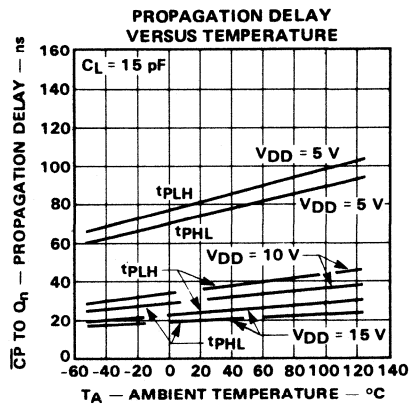
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}) and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

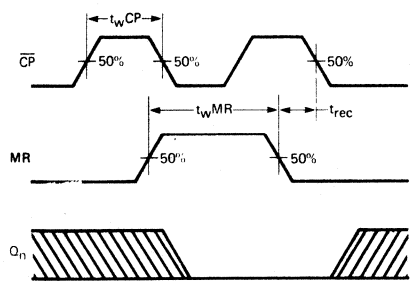








SWITCHING WAVEFORMS

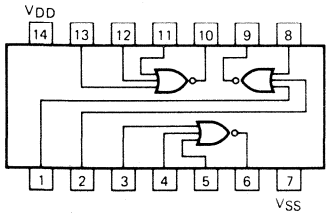


MINIMUM PULSE WIDTH
FOR $\overline{CP}$ AND MR AND MR RECOVERY TIME

TRIPLE 3-INPUT NOR GATE

DESCRIPTION — This CMOS logic element provides a 3-input positive NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

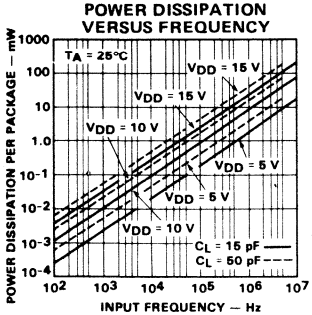
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		30	75		13	40		12		ns	
t_{PHL}			35	75		20	40		16		ns	C_L = 15 pF
t_{TLH}	Output Transition		15	75		8	40		6	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		16	75		6	40		4	25	ns	
t_{PLH}	Propagation Delay		45	110		20	60		15		ns	
t_{PHL}			47	110		25	60		21		ns	C_L = 50 pF
t_{TLH}	Output Transition		38	135		20	70		15	45	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		38	135		15	70		11	45	ns	

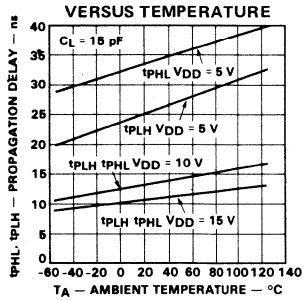
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

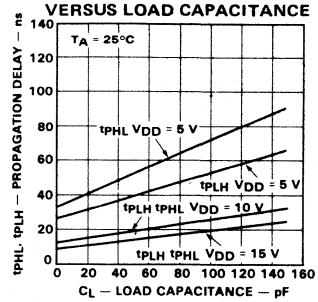
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



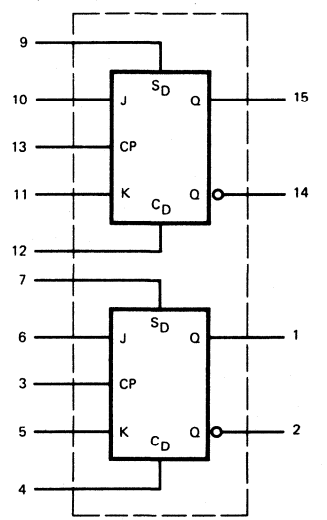
F4027/34027
DUAL JK FLIP-FLOP

DESCRIPTION — The F4027 is a Dual JK Flip-Flop which is edge-triggered and features independent Direct Set, Direct Clear, and Clock inputs. Data is accepted when the Clock is LOW and transferred to the output on the positive-going edge of the Clock. The active HIGH asynchronous Clear Direct (C_D) and Set Direct (S_D) are independent and override the J, K, or Clock inputs. The outputs are buffered for best system performance.

PIN NAMES

J, K	Synchronous Inputs
CP	Clock Input (L → H Edge-Triggered)
S_D	Asynchronous Direct Set Input (Active HIGH)
C_D	Asynchronous Direct Clear Input (Active HIGH)
Q	True Output
$\overline{Q}$	Complement Output

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLES

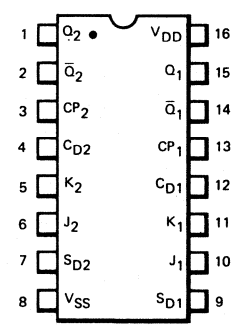
ASYNCHRONOUS INPUTS		OUTPUTS	
S_D	C_D	Q	$\overline{Q}$
L	H	L	H
H	L	H	L
H	H	H	H

SYNCHRONOUS INPUTS			OUTPUTS	
CP	J	K	Q_{n+1}	$\overline{Q}_{n+1}$
⎍	L	L	NO CHANGE	
⎍	H	L	H	L
⎍	L	H	L	H
⎍	H	H	$\overline{Q}_n$	Q_n

L = LOW Level
H = HIGH Level
⎍ = Positive-Going Transition
X = Don't Care
Q_{n+1} = State After Clock Positive Transition

Conditions: $S_D = C_D$ = LOW

CONNECTION DIAGRAMS
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

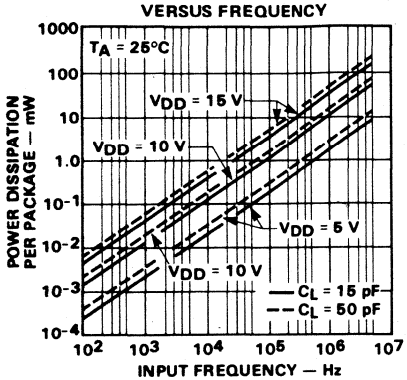
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 4)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q, $\overline{Q}$		75	150		35	75		25		ns	C_L = 15 pF
t_{PHL}			75	150		35	75		25		ns	
t_{PLH}	Propagation Delay, S_D to Q		160	300		80	150		60		ns	Input Transition
t_{PHL}	Propagation Delay, C_D to Q		160	300		80	150		60		ns	Times ≤ 20 ns
t_{TLH}	Output Transition Time		50	100		30	60		20	40	ns	
t_{THL}			50	100		30	60		20	40	ns	
t_{PLH}	Propagation Delay, CP to Q, $\overline{Q}$		100	200		45	85		30		ns	C_L = 50 pF
t_{PHL}			100	200		45	85		30		ns	
t_{PLH}	Propagation Delay, S_D to Q		180	350		90	175		75		ns	Input Transition
t_{PHL}	Propagation Delay, C_D to Q		180	350		90	175		75		ns	Times ≤ 20 ns
t_{TLH}	Output Transition Time		85	150		45	85		30	50	ns	
t_{THL}			85	150		45	85		30	50	ns	
t_s	Set-Up Time, J, K to CP	100	45		40	20			15		ns	
t_h	Hold Time, J, K to CP	0	-25		0	-10			-5		ns	
t_wCP(L)	Minimum Clock Pulse Width	150	75		70	35			25		ns	C_L = 15 pF
t_w S_D(H)	Minimum S_D Pulse Width	150	75		60	30			25		ns	Input Transition
t_w C_D(H)	Minimum C_D Pulse Width	150	75		60	30			25		ns	Times ≤ 20 ns
t_{rec} S_D	Recovery Time for S_D	0	-5		0	-4			-3		ns	
t_{rec} C_D	Recovery Time for C_D	0	-5		0	-4			-3		ns	
f_{MAX}	Maximum CP Frequency (Note 3)	4	8		8	16					MHz	

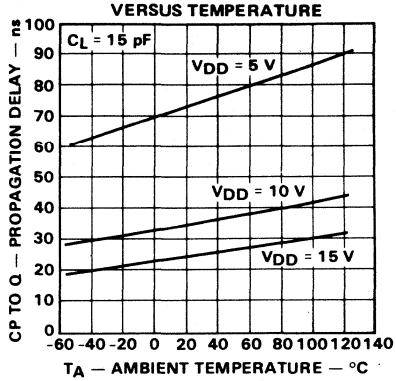
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

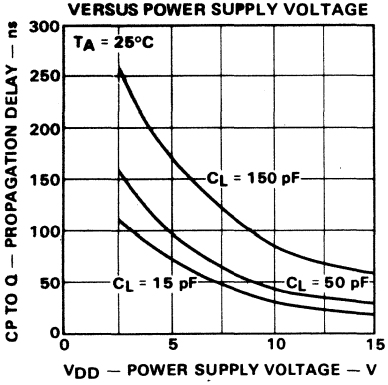
POWER DISSIPATION VERSUS FREQUENCY



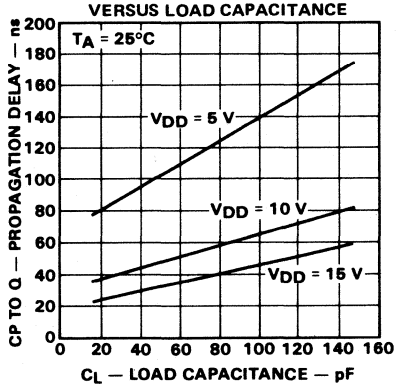
PROPAGATION DELAY VERSUS TEMPERATURE



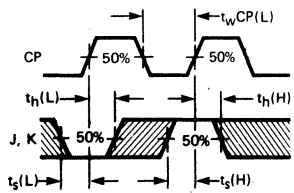
PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

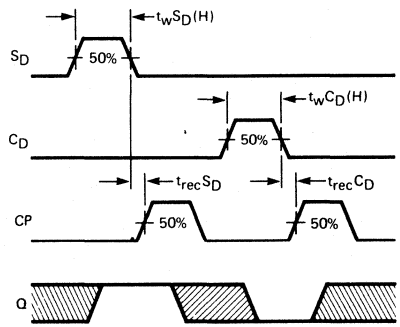


SWITCHING WAVEFORMS



NOTE:
t_s & t_h are shown as positive values but may be specified as negative values.

SET-UP TIMES, HOLD TIMES, AND MINIMUM CLOCK PULSE WIDTH



RECOVERY TIME FOR S_D, RECOVERY TIME FOR C_D, MINIMUM S_D PULSE WIDTH, AND MINIMUM C_D PULSE WIDTH

F4028/34028
1-OF-10 DECODER

DESCRIPTION – The F4028 is a CMOS 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A_0 through A_3 causes the selected output to be HIGH, the other nine will be LOW. If desired, the F4028 may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A_0, A_1, and A_2 selecting an output 0 through 7. Input A_3 then becomes an active LOW enable, forcing the selected output LOW when A_3 is HIGH. The F4028 may also be used as an 8-input demultiplexer with an active LOW data input. The outputs are fully buffered for best performance.

- **BCD TO 1-OF-10 DECODER**
- **1-OF-8 DECODER WITH ACTIVE LOW ENABLE**
- **8-INPUT DEMULTIPLEXER WITH ACTIVE LOW DATA INPUT**

PIN NAMES

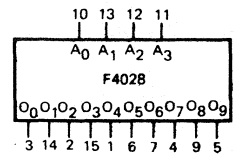
$A_0 - A_3$	Address Inputs, 1-2-4-8 BCD
$O_0 - O_9$	Outputs (Active HIGH)

TRUTH TABLE

INPUTS				OUTPUTS									
A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	H	L
H	L	H	H	L	L	L	L	L	L	L	L	L	H
H	H	L	L	L	L	L	L	L	L	L	L	H	L
H	H	L	H	L	L	L	L	L	L	L	L	L	H
H	H	H	L	L	L	L	L	L	L	L	L	H	L
H	H	H	H	L	L	L	L	L	L	L	L	L	H

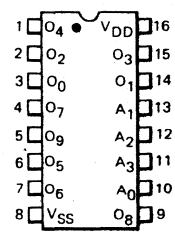
H = HIGH Level
L = LOW Level

LOGIC SYMBOL



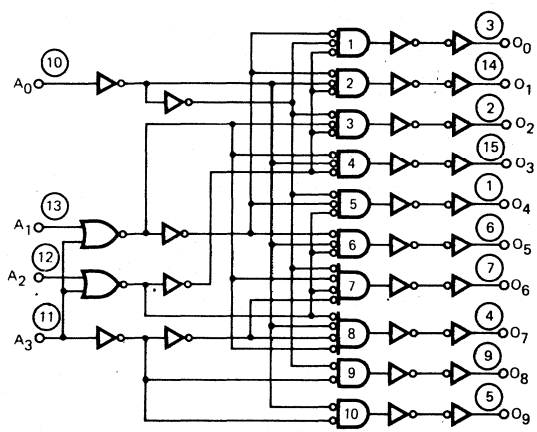
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			30			60		12		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		µA	MIN, 25°C	
					100			200		40			MAX	

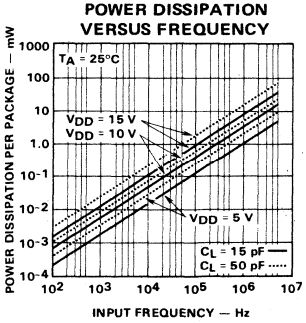
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		145	290		60	130		37		ns	
t_{PHL}	A_n to O_n		125	290		45	130		30		ns	C_L = 15 pF
t_{TLH}	Output Transition		40	100		20	60		15	40	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		40	100		20	60		15	40	ns	
t_{PLH}	Propagation Delay,		167	325		66	145		45		ns	
t_{PHL}	A_n to O_n		157	325		57	145		40		ns	C_L = 50 pF
t_{TLH}	Output Transition		85	200		40	100		31	70	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		110	200		37	100		25	70	ns	

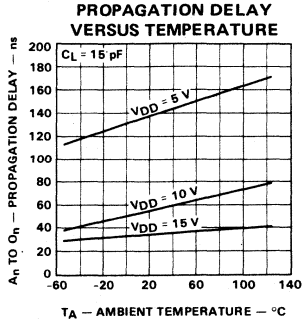
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

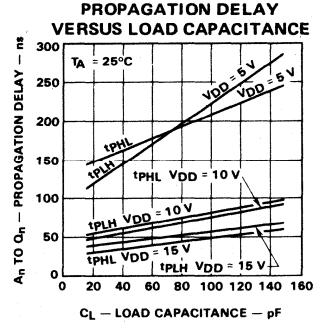
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



F4029/34029
SYNCHRONOUS UP/DOWN COUNTER

DESCRIPTION – The F4029 is a Synchronous Edge-Triggered Up/Down 4-Bit Binary/BCD Decade Counter with a Clock Input (CP), an active LOW Count Enable Input ($\overline{CE}$), an Up/Down Control Input (UP/$\overline{DN}$), a Binary/Decade Control Input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH Parallel Load Input (PL), four Parallel Data Inputs (P_0–P_3), four Parallel Buffered Outputs (Q_0–Q_3) and an active LOW Terminal Count Output ($\overline{TC}$).

Information on the Parallel Inputs (P_0–P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions. With the Parallel Load Input (PL) LOW, operation is synchronous and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). Operation is determined by the three synchronous Mode Control Inputs; UP/$\overline{DN}$, BIN/$\overline{DEC}$ and $\overline{CE}$ (see the Mode Selection Table). These inputs must be stable only during the set-up time prior to the LOW-to-HIGH transition of the Clock Input (CP) and the hold time after this clock transition. The Terminal Count Output ($\overline{TC}$) is LOW when the counter is at its terminal count, as determined by the counting mode, and the Count Enable Input ($\overline{CE}$) is LOW (see Logic Equation for $\overline{TC}$).

- **BINARY OR DECADE UP/DOWN COUNTER**
- **ASYNCHRONOUS PARALLEL LOAD**
- **ACTIVE LOW COUNT ENABLE**
- **CLOCK EDGE-TRIGGERED ON THE LOW-TO-HIGH TRANSITION**
- **ACTIVE LOW TERMINAL COUNT FOR CASCADING**
- **TYPICAL COUNT FREQUENCY OF 12 MHz AT V_{DD} = 10 V**

PIN NAMES

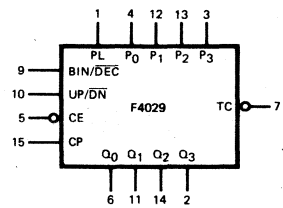
PL	Parallel Load Input
P_0–P_3	Parallel Data Inputs
BIN/$\overline{DEC}$	Binary/Decade Control Input
UP/$\overline{DN}$	Up/Down Control Input
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
$\overline{Q_0}$–Q_3	Buffered Parallel Outputs
$\overline{TC}$	Terminal Count Output (Active LOW)

MODE SELECTION TABLE

PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	X	H	X	No Change
L	L	L	L	⌐	Count Down, Decade
L	L	H	L	⌐	Count Up, Decade
L	H	L	L	⌐	Count Down, Binary
L	H	H	L	⌐	Count Up, Binary

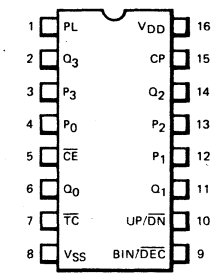
H = HIGH Level
L = LOW Level
X = Don't Care
⌐ = Positive-Going Transition

LOGIC SYMBOL



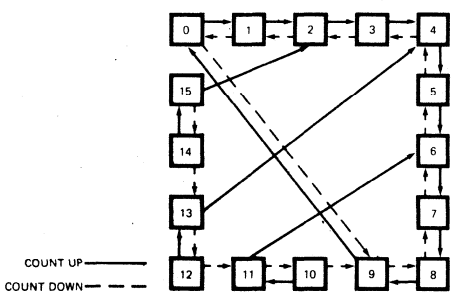
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

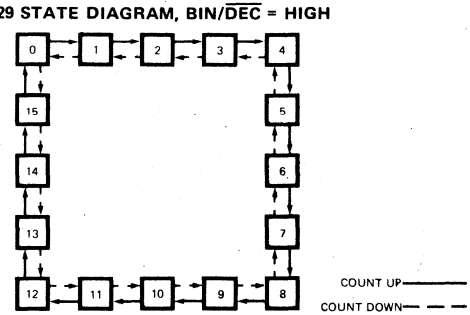


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4029 STATE DIAGRAM BIN/$\overline{DEC}$ = LOW



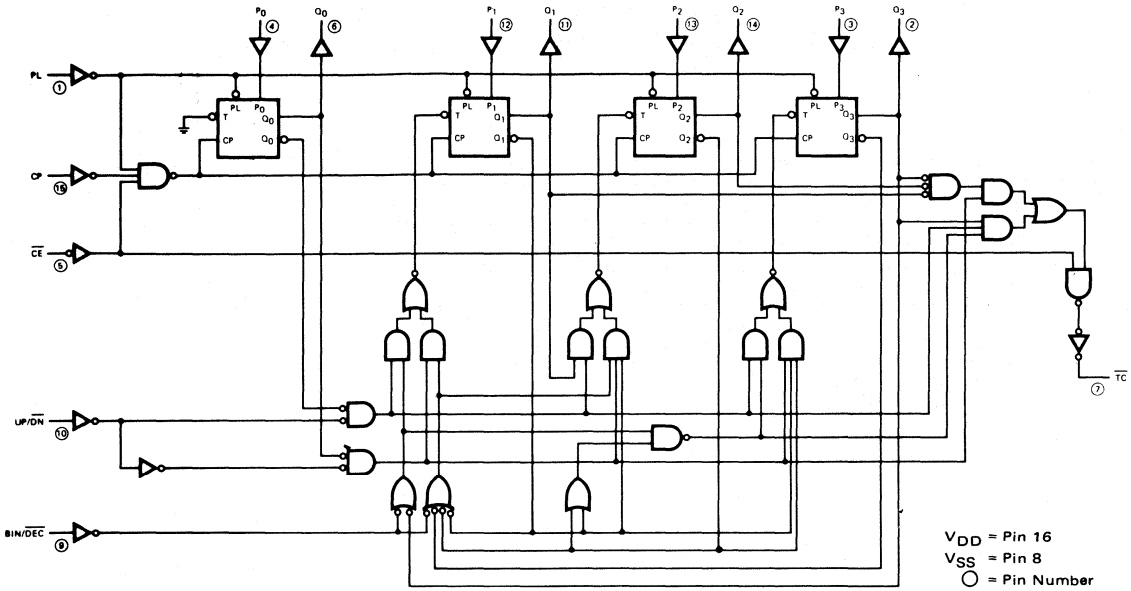
F4029 STATE DIAGRAM, BIN/$\overline{DEC}$ = HIGH

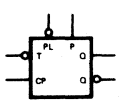


LOGIC EQUATION FOR TERMINAL COUNT

$$TC = CE \bullet [UP \bullet Q_0 \bullet Q_3 \bullet (\overline{BIN} + (Q_1 \bullet Q_2)) + (\overline{UP} \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)]$$

LOGIC DIAGRAM





$\overline{PL}$ (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when $\overline{PL}$ is LOW Overriding all Other Inputs
$\overline{T}$ (Toggle Input) — Forces the Q Output to Synchronously Toggle when a LOW is Placed on this Input.
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complimentary Outputs)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

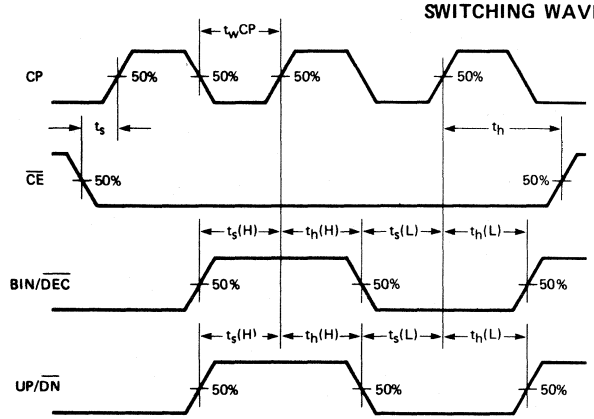
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

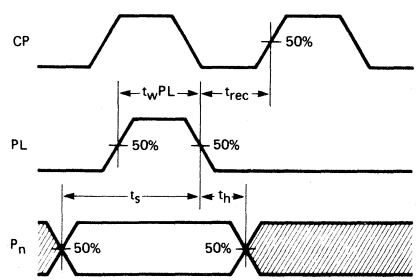
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n		135 135			54 50			35 33		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{TC}$		150 228			62 90			42 60		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, PL to Q_n		152 194			59 80			38 56		ns ns	
t_{TLH} t_{THL}	Output Transition Time		25 25			13 13			10 10		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n		150 150			62 59			41 39		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{TC}$		167 252			71 100			48 66		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, PL to Q_n		170 220			70 90			45 62		ns ns	
t_{TLH} t_{THL}	Output Transition Time		60 65			31 25			23 18		ns ns	
t_wCP	CP Minimum Pulse Width		50			21			14		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_wPL	PL Minimum Pulse Width		60			21			16		ns	
t_{rec}	PL Recovery Time		62			24			17		ns	
t_s t_h	Set-Up Time, BIN/$\overline{DEC}$ to CP Hold Time, BIN/$\overline{DEC}$ to CP		106 104			41 40			29 28		ns ns	
t_s t_h	Set-Up Time, UP/$\overline{DN}$ to CP Hold Time, UP/$\overline{DN}$ to CP		145 101			55 38			38 25		ns ns	
t_s t_h	Set-Up Time, $\overline{CE}$ to CP Hold Time, $\overline{CE}$ to CP		118 101			49 38			33 25		ns	
t_s t_h	Set-Up Time, P_n to PL Hold Time, P_n to PL		29 26			11 7			8 4		ns ns	
f_{MAX}	Input Clock Frequency (Note 4)		5			12					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



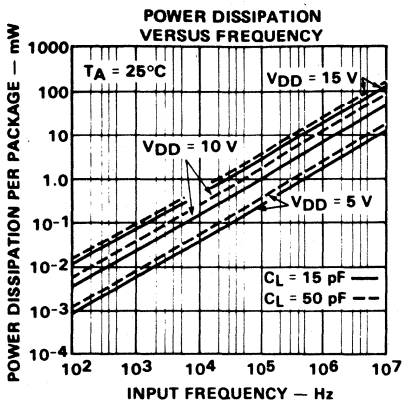
MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP, BIN/$\overline{DEC}$ TO CP AND UP/$\overline{DN}$ TO CP

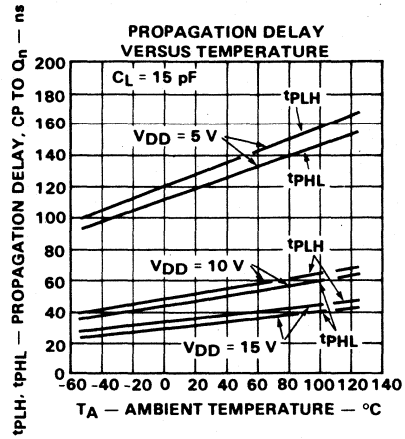


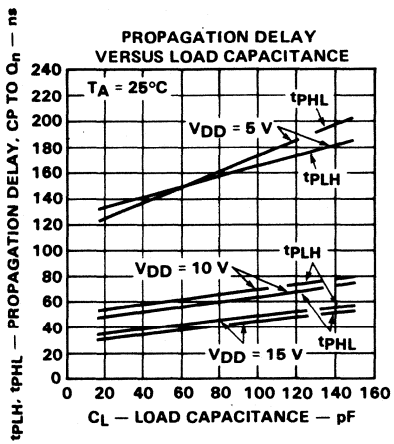
MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS







APPLICATIONS

Interconnection techniques for multistage counting are shown in Figures 1 through 4. When using the schemes shown in Figures 1, 3 and 4, the BIN/$\overline{\text{DEC}}$ and UP/$\overline{\text{DN}}$ Inputs may be changed only when the Clock Input to the first stage is HIGH. However, when using the scheme shown in Figure 2, UP/$\overline{\text{DN}}$, BIN/$\overline{\text{DEC}}$ and $\overline{\text{CE}}$ may be changed independent of the state of the Clock Input. The methods illustrated in Figures 1 and 3 will operate with long transition times at the Clock Input to the first counter; whereas, the other schemes require a fast transition at the Clock Input.

Figure 1 is a ripple clock expansion scheme in which the maximum counting frequency is limited only by the frequency capability of the first counter. The disadvantage of this technique is that the Outputs of the most significant stage do not change until the clock has rippled through all the preceding stages.

A fully synchronous expansion method is shown in Figure 2. Since the Clock Input is applied simultaneously to all stages, the Outputs of all stages change simultaneously. The maximum counting frequency is limited by the time required for the Count Enable to ripple through all the stages before the next Clock Input is applied.

The semi-synchronous technique illustrated in Figure 3 allows a higher counting frequency than the method shown in Figure 2 by allowing $\overline{\text{TC}}$ to take either 10 or 16 clock periods to ripple from the second stage to the most significant stage (10 clock periods when BIN/$\overline{\text{DEC}}$ = L, 16 clock periods when BIN/$\overline{\text{DEC}}$ = H). The Outputs of all stages, except the first, change simultaneously. The Outputs of the first stage change before the other stages.

The speed advantage of this scheme is lost if the count direction or count modulus is rapidly changed.

The method shown in Figure 4 is the same as in Figure 3 except an external gate is added to reduce the delay between the Clock Input to the first stage and the Clock Input to the following stages.

APPLICATIONS (Cont'd)

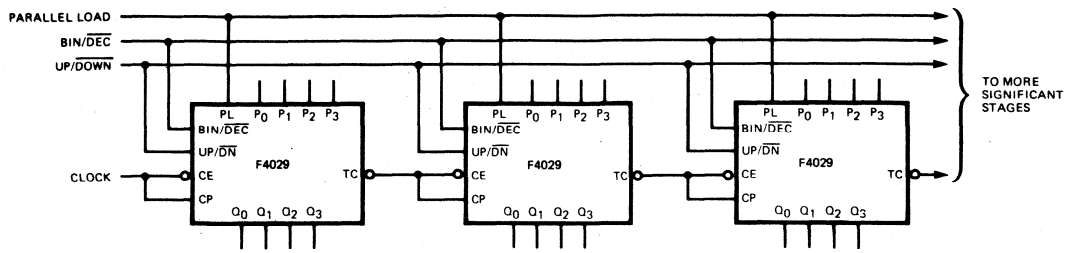


Fig. 1 RIPPLE CLOCK EXPANSION

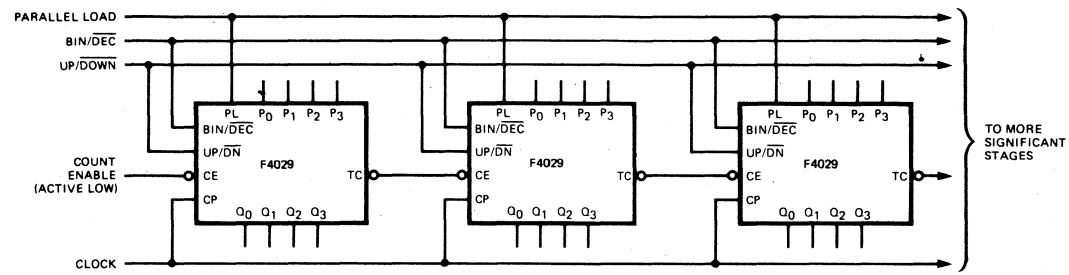


Fig. 2 PARALLEL CLOCK EXPANSION (FULLY SYNCHRONOUS)

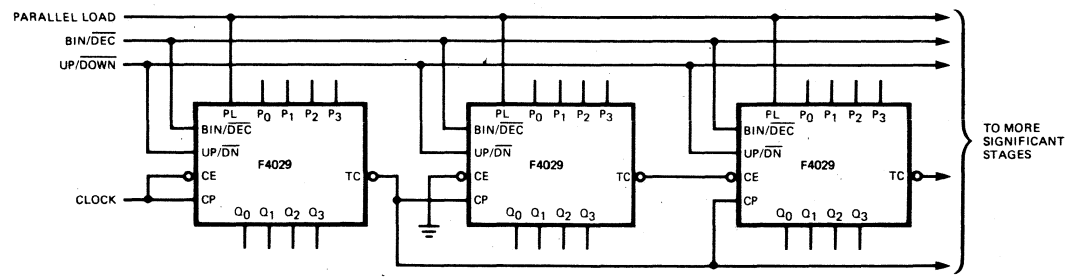


Fig. 3 SEMI-SYNCHRONOUS EXPANSION

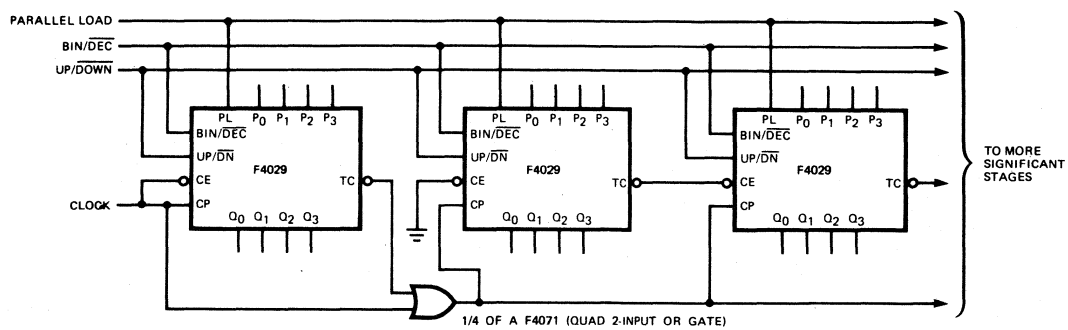
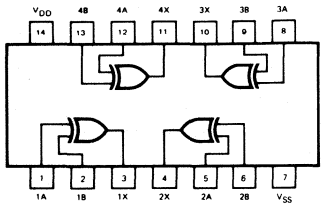


Fig. 4 HIGH SPEED SEMI-SYNCHRONOUS EXPANSION

QUAD EXCLUSIVE-OR GATE

DESCRIPTION – The F4030 CMOS logic element provides the Exclusive-OR function. The outputs are fully buffered for best performance.

F4030 QUAD EXCLUSIVE-OR GATE



$X = \overline{A}B + A\overline{B}$

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			5.0			10.0		2		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					70.0			140.0		28			MAX	
		XM			0.5			1.0		0.2		μA	MIN, 25°C	
					30.0			60.0		12			MAX	

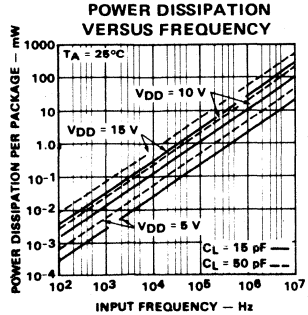
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		65	130		33	65		23		ns	
t_{PHL}	A or B to X		65	130		33	65		23		ns	C_L = 15 pF
t_{TLH}	Output Transition		23	45		10	25		8	20	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		23	45		10	25		8	20	ns	
t_{PLH}	Propagation Delay,		85	170		45	90		27		ns	
t_{PHL}	A or B to X		85	170		45	90		27		ns	C_L = 50 pF
t_{TLH}	Output Transition		50	100		23	50		17	35	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		50	100		23	50		17	35	ns	

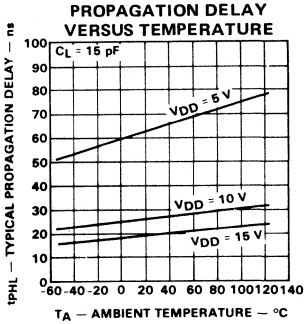
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

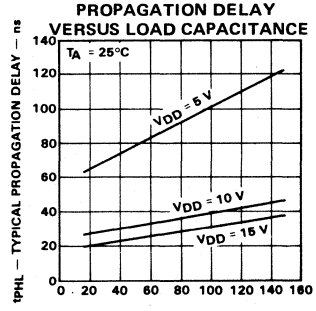
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



F4031/34031
64-STAGE STATIC SHIFT REGISTER

DESCRIPTION – The F4031 is an edge-triggered 64-Stage Static Shift Register with two Serial Data Inputs (D_0, D_1), a Data Select Input (S), a Clock Input (CP), a buffered Clock Output (CO) and buffered Outputs from the 64th bit position (Q_{63}, $\overline{Q_{63}}$).

Data from the selected Data Inputs (D_0 or D_1), as determined by the state of the Select Input (S), is shifted into the first shift register position and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP). D_0 is selected by a LOW on the Select Input (S) and D_1 is selected by a HIGH on the Select Input (S).

Registers can be cascaded by connecting all the Clock Inputs (CP) together or by driving the Clock Input (CP) of the right-most register with the system clock and connecting the Clock Output (CO) to the Clock Input (CP) of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store the Output (Q_{63}) of the right-most register until the left-most register is clocked.

- **CLOCK INPUT IS L→H EDGE-TRIGGERED**
- **DATA SELECT INPUT (S) ALLOWS DATA INPUT AT EITHER D_0 OR D_1 INPUTS**
- **EASILY CASCADED**
- **TRUE AND COMPLEMENTARY BUFFERED OUTPUTS AVAILABLE FROM 64TH STAGE**

PIN NAMES

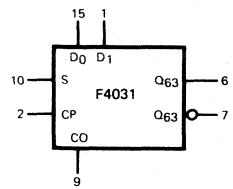
D_0, D_1	Data Inputs
S	Data Select Input
CP	Clock Input (L→H Edge-Triggered)
CO	Buffered Clock Output
Q_{63}	Buffered Output from the 64th Stage
$\overline{Q_{63}}$	Complementary Buffered Output from the 64th Stage

TRUTH TABLE

S	D_0	D_1	Data Into Flip-Flop 1
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

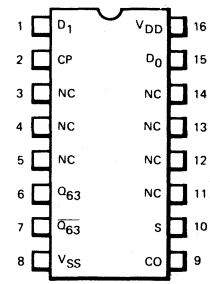
L = Low Level
H = High Level
X = Don't Care

LOGIC SYMBOL



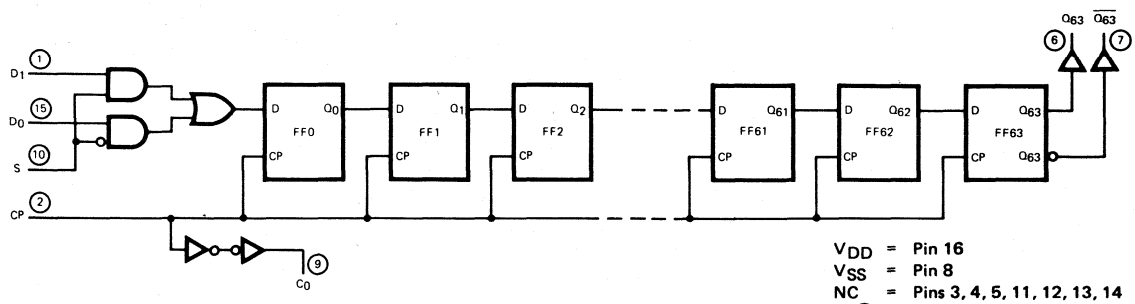
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pins 3,4,5,11,12,13,14

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pins 3, 4, 5, 11, 12, 13, 14
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

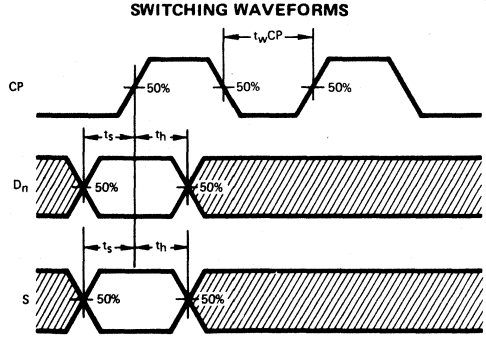
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			10			25		5		μA	MIN, 25°C	
					600			1500		300			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_{63}, $\overline{Q_{63}}$		100			50			35		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			100			50			35		ns	
t_{PLH}	Propagation Delay, CP to CO		40			20			15		ns	
t_{PHL}			40			20			15		ns	
t_{TLH}	Output Transition Time		35			20			10		ns	
t_{THL}			35			20			10		ns	
t_{PLH}	Propagation Delay, CP to Q_{63}, $\overline{Q_{63}}$		120			60			40		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			120			60			40		ns	
t_{PLH}	Propagation Delay, CP to CO		45			25			20		ns	
t_{PHL}			45			25			20		ns	
t_{TLH}	Output Transition Time		65			35			15		ns	
t_{THL}			65			35			15		ns	
t_wCP(L)	Minimum Clock Pulse Width		25			10			8		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_s	Set-Up Time, S to CP		75			40			30		ns	
t_h	Hold Time, S to CP		40			20			15		ns	
t_s	Set-Up Time, D_n to CP		75			40			30		ns	
t_h	Hold Time, D_n to CP		40			20			15		ns	
f_{MAX}	Maximum Clock Frequency (Note 4)		4			8					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
4. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH, SET-UP AND HOLD TIMES, D_n TO CP AND S TO CP

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

F4035/34035
4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION – The F4035 is a fully synchronous edge-triggered 4-Bit Shift Register with a Clock Input (CP), four synchronous Parallel Data Inputs (P_0–P_3), two synchronous Serial Data Inputs (J, $\overline{K}$), a synchronous Parallel Enable Input (PE), Buffered Parallel Outputs from all 4-bit positions (Q_0–Q_3), a True/Complement Input (T/$\overline{C}$) and an overriding asynchronous Master Reset Input (MR).

Operation is synchronous (except for Master Reset) and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from Parallel Inputs (P_0–P_3) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Inputs (J, $\overline{K}$) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP). D-type entry is obtained by tying the two Serial Data Inputs (J, $\overline{K}$) together.

The Outputs (Q_0–Q_3) are either inverting or non-inverting, depending on the True/Complement Input (T/$\overline{C}$). With the T/$\overline{C}$ Input HIGH, the Outputs (Q_0–Q_3) are non-inverting (Active HIGH). With the T/$\overline{C}$ Input LOW, the Outputs (Q_0–Q_3) are inverting (Active LOW).

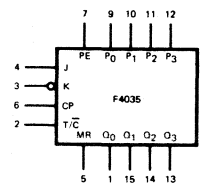
A HIGH on the Master Reset Input (MR) resets all four bit positions (Q_0–Q_3 = LOW if T/$\overline{C}$ = HIGH, Q_0–Q_3 = HIGH if T/$\overline{C}$ = LOW) independent of all other input conditions.

- **TYPICAL SHIFT FREQUENCY OF 12 MHz AT V_{DD} = 10 V**
- **J, $\overline{K}$ INPUTS TO THE FIRST STAGE**
- **T/$\overline{C}$ INPUT FOR TRUE OR COMPLEMENTARY OUTPUTS**
- **SYNCHRONOUS PARALLEL ENABLE**
- **CLOCK EDGE-TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **ASYNCHRONOUS MASTER RESET**

PIN NAMES

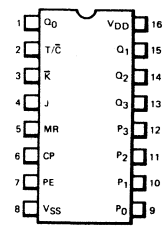
PE	Parallel Enable Input
P_0–P_3	Parallel Data Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
T/$\overline{C}$	True/Complement Input
MR	Master Reset Input
Q_0–Q_3	Buffered Parallel Outputs

LOGIC SYMBOL



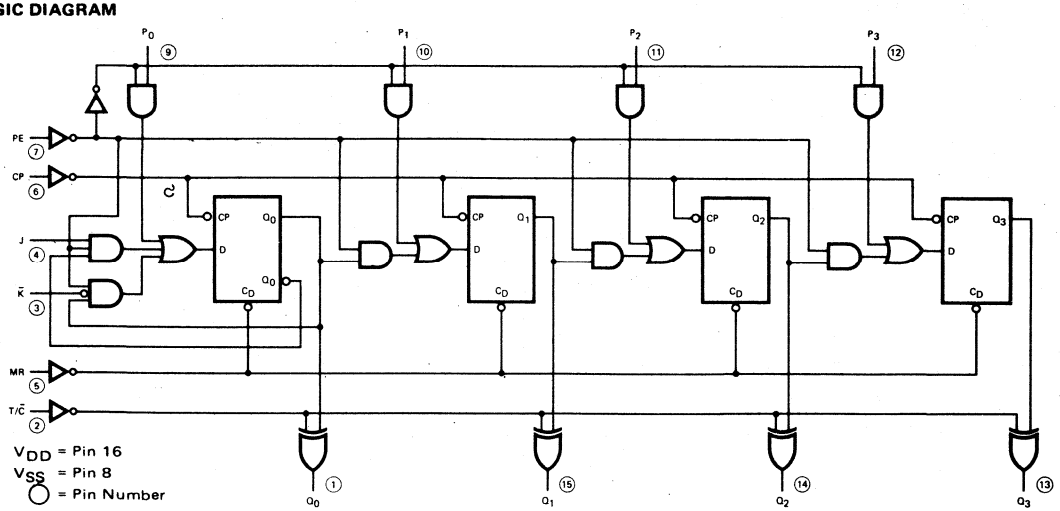
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

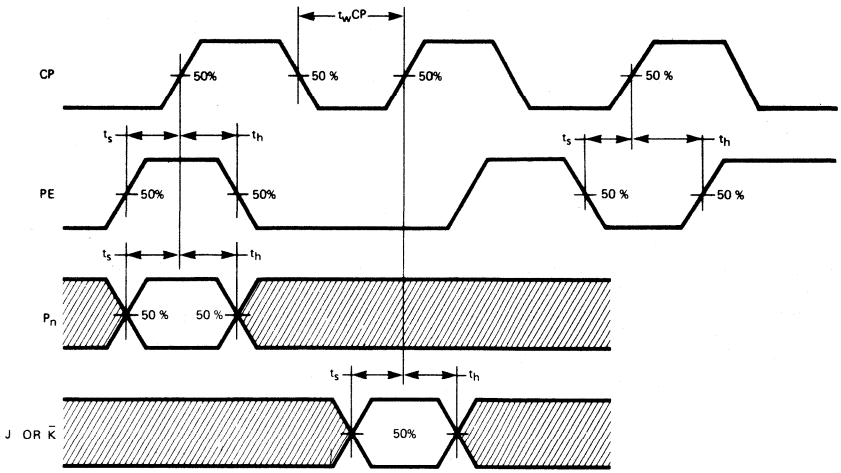
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					500			1000		200			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					40			80		16			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

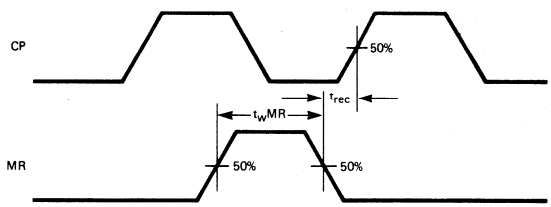
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n		180 180			80 80			50 50		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, MR to Q_n		225 225			100 100			60 60		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, T/C to Q_n		100 100			45 45			35 35		ns ns	
t_{TLH} t_{THL}	Output Transition Time		50 50			25 25			20 20		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n		200 200			90 90			60 60		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, MR to Q_n		250 250			120 120			75 75		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, T/C to Q_n		125 125			55 55			40 40		ns ns	
t_{TLH} t_{THL}	Output Transition Time		85 85			45 45			30 30		ns ns	
t_wCP	CP Minimum Pulse Width		75			30			20		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_wMR	MR Minimum Pulse Width		60			25			20		ns	
t_{rec}	MR Recovery Time		160			60			45		ns	
t_s t_h	Set-Up Time, P_n to CP Hold Time, P_n to CP		100 -10			40 -5			25 -5		ns ns	
t_s t_h	Set-Up Time, PE to CP Hold Time, PE to CP		100 -10			40 -5			25 -5		ns ns	
t_s t_h	Set-Up Time, J, K to CP Hold Time, J, K to CP		100 -10			40 -5			25 -5		ns ns	
f_{MAX}	Max. Input Clock Frequency (Note 4)		5			12					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CP PULSE WIDTH AND SET-UP AND HOLD TIMES, PE TO CP, P_n TO CP, AND J OR $\bar{K}$ TO CP



MR RECOVERY TIME AND MINIMUM MR PULSE WIDTH

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4040/34040
12-STAGE BINARY COUNTER

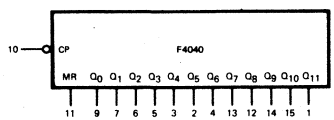
DESCRIPTION – The F4040 is a 12-Stage Binary Ripple Counter with a Clock Input ($\overline{CP}$), an overriding asynchronous Master Reset Input (MR) and twelve fully buffered Outputs (Q_0-Q_{11}). The counter advances on the HIGH-to-LOW transition of the Clock Input ($\overline{CP}$). A HIGH on the Master Reset Input (MR) clears all counter stages and forces all Outputs (Q_0-Q_{11}) LOW, independent of the Clock Input ($\overline{CP}$).

- **25 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **CLOCK IS H→L TRIGGERED**
- **COMMON ASYNCHRONOUS MASTER RESET**
- **FULLY BUFFERED OUTPUTS FROM ALL 12 STAGES**

PIN NAMES

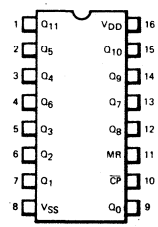
$\overline{CP}$	Clock Input (H→L Triggered)
MR	Master Reset Input (Active HIGH)
Q_0-Q_{11}	Parallel Outputs

LOGIC SYMBOL



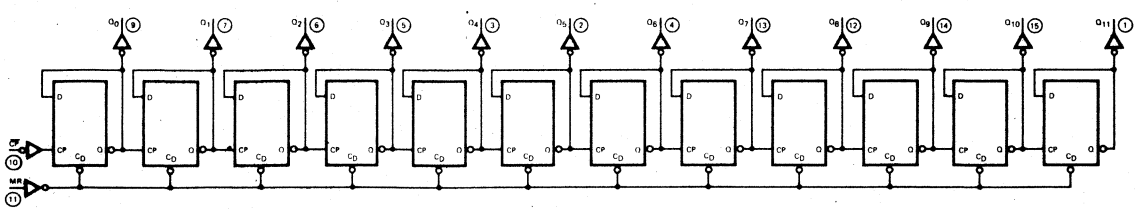
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		300			MAX	

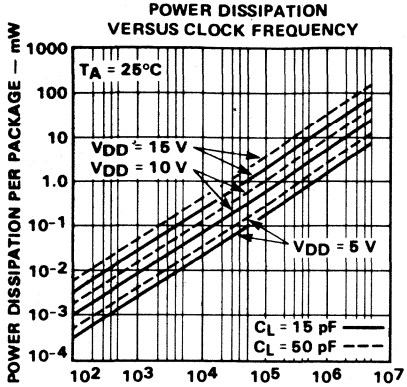
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		110	220		45	90		30		ns	C_L = 15 pF
t_{PHL}			85	170		37	75		25		ns	
t_{PHL}	Propagation Delay, MR to Q_n		150	300		65	130		43		ns	Input Transition
t_{TLH}	Output Transition Time		30	75		13	40		10	25	ns	Times ⩽ 20 ns
t_{THL}			30	75		13	40		10	25	ns	
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_0		130	260		55	110		37		ns	C_L = 50 pF
t_{PHL}			110	220		45	90		33		ns	
t_{PHL}	Propagation Delay, MR to Q_n		180	360		75	150		50		ns	Input Transition
t_{TLH}	Output Transition Time		65	135		35	70		25	45	ns	Times ⩽ 20 ns
t_{THL}			65	135		35	70		25	45	ns	
$t_W\overline{CP}(H)$	Minimum Clock Pulse Width	100	50		40	20			16		ns	C_L = 15 pF
$t_W MR(H)$	Minimum MR Pulse Width	140	70		55	27			20		ns	Input Transition
t_{rec}	Recovery Time for MR	85	43		35	17			12		ns	Times ⩽ 20 ns
f_{MAX}	Input Clock Frequency (Note 3)	5	10		12	25					MHz	

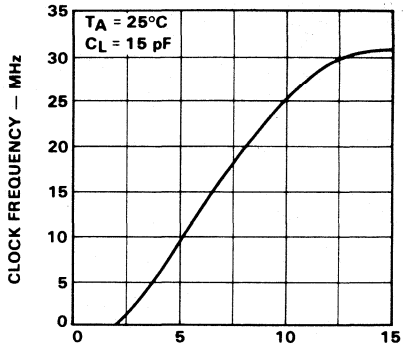
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}), and Minimum Pulse Widths (t_W) do not vary with load capacitance.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

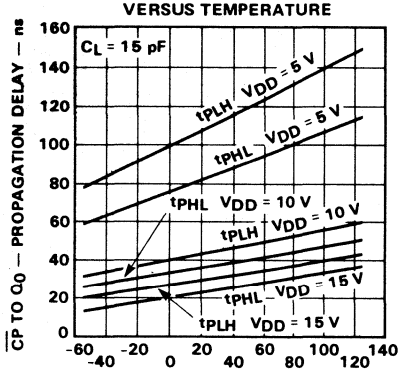
POWER DISSIPATION VERSUS CLOCK FREQUENCY



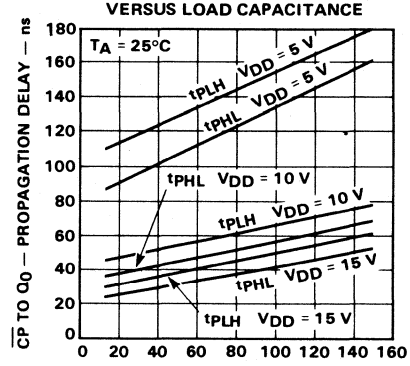
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



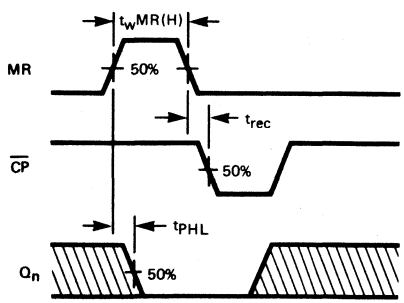
PROPAGATION DELAY VERSUS TEMPERATURE



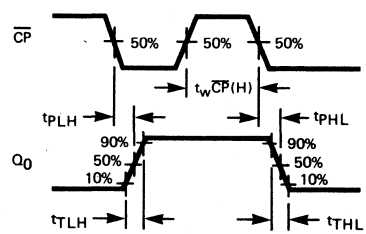
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



PROPAGATION DELAY MASTER RESET TO OUTPUT, MINIMUM MASTER RESET PULSE WIDTH AND RECOVERY TIME FOR MASTER RESET

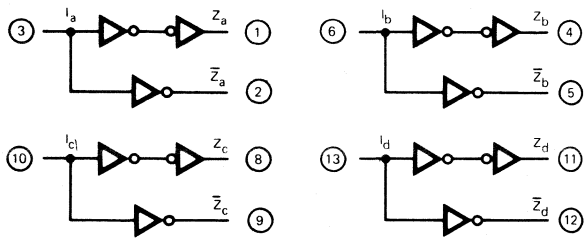


PROPAGATION DELAY CLOCK TO OUTPUT Q_0, OUTPUT TRANSITION TIMES AND MINIMUM CLOCK PULSE WIDTH

QUAD TRUE/COMPLEMENT BUFFER

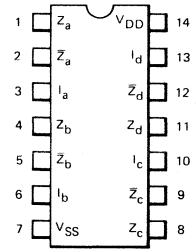
DESCRIPTION — The F4041 is a Quad True/Complement Buffer which provides both an inverted active LOW Output ($\overline{Z}$) and a non-inverted active HIGH Output (Z) for each Input (I).

LOGIC DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

I_a, I_b, I_c, I_d	Buffer Input
Z_a, Z_b, Z_c, Z_d	Buffered True Output
$\overline{Z}_a$, $\overline{Z}_b$, $\overline{Z}_c$, $\overline{Z}_d$	Buffered Complementary Output

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			10			20		4.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56.0			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24.0			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		40			20			15		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			40			20			15		ns	
t_{TLH}	Output Transition Time		25			10			8		ns	
t_{THL}			25			10			8		ns	
t_{PLH}	Propagation Delay		60			25			20		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			60			25			20		ns	
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4042/34042

QUAD D LATCH

DESCRIPTION – The F4042 is a 4-Bit Latch with four Data Inputs (D_0-D_3), four buffered Latch Outputs (Q_0-Q_3), four buffered Complementary Latch Outputs ($\overline{Q}_0$-$\overline{Q}_3$) and two Common Enable Inputs (E_0 and E_1). Information on the Data Inputs (D_0-D_3) is transferred to the Outputs (Q_0-Q_3) while both Enable Inputs (E_0, E_1) are in the same state, either HIGH or LOW. The Outputs (Q_0-Q_3) follow the Data Inputs (D_0-D_3) as long as both Enable Inputs (E_0, E_1) remain in the same state. When the two Enable Inputs (E_0, E_1) are different, the Data Inputs (D_0-D_3) do not affect the Outputs (Q_0-Q_3) and the information in the latch is stored. The $\overline{Q}_0$-$\overline{Q}_3$ Outputs are always the complement of the Q_0-Q_3 Outputs. The Exclusive-OR input structure allows the choice of either polarity for the Enable Input. With one Enable Input HIGH, the other Enable Input is active HIGH; with one Enable Input LOW, the other Enable Input is active LOW.

The last moment prior to the trailing end of the enable condition that the Latch Outputs can still be affected by the inputs is specified as a set-up time. A negative set-up time, as typically exhibited by this device, means that the latches respond to input changes after the end of the enable condition. Following established industry practice, a hold time is specified, defining the time after the end of the enable condition, that the inputs must be held stable, so that they do not affect the state of the latches. It follows from this definition, that the hold time is identical with the negative set-up time. Set-up and hold times have a tolerance, due to manufacturing process variations, temperature and supply voltage changes. For predictable operation the data input levels must be held stable over the full spread of this timing window starting with the earliest set-up time (largest positive or smallest negative value) to the latest hold time.

- **ACTIVE HIGH OR ACTIVE LOW ENABLE**
- **TRUE AND COMPLEMENTARY OUTPUTS (Q & $\overline{Q}$)**

PIN NAMES

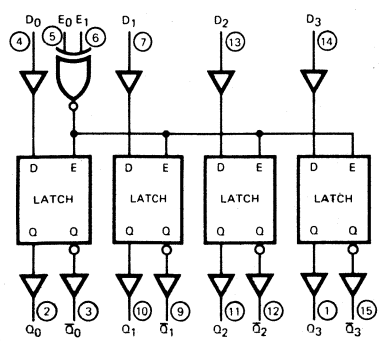
D_0-D_3	Data Inputs
E_0, E_1	Enable Inputs
Q_0-Q_3	Parallel Latch Outputs
$\overline{Q}_0$-$\overline{Q}_3$	Complementary Parallel Latch Outputs

TRUTH TABLE

E_0	E_1	LATCH CONDITION
L	L	Enabled
L	H	Not Enabled
H	L	Not Enabled
H	H	Enabled

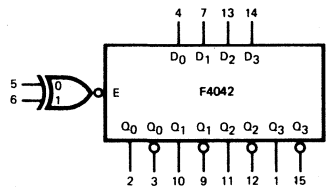
L = LOW Level
H = HIGH Level

LOGIC DIAGRAM



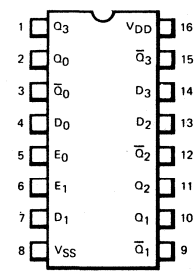
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

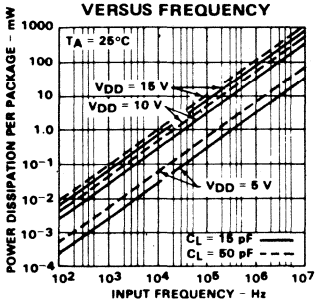
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		85	170		36	72		27		ns	
t_{PHL}	Data to Output		80	160		35	70		26		ns	C_L = 15 pF
t_{PLH}	Propagation Delay,		135	270		55	110		41		ns	Input Transition
t_{PHL}	Enable to Output		115	230		45	90		35		ns	Times ⩽ 20 ns
t_{TLH}	Output Transition		29	75		15	40		11	25	ns	
t_{THL}	Time		27	75		15	40		10	25	ns	
t_{PLH}	Propagation Delay,		101	200		45	90		33		ns	
t_{PHL}	Data to Output		99	200		44	88		33		ns	C_L = 50 pF
t_{PLH}	Propagation Delay,		156	310		66	132		47		ns	Input Transition
t_{PHL}	Enable to Output		137	275		58	116		41		ns	Times ⩽ 20 ns
t_{TLH}	Output Transition		65	135		31	70		25	45	ns	
t_{THL}	Time		60	135		26	70		20	45	ns	
t_s	Set-Up Time, D_n to E_0 or E_1	10	-12		10	-6			-4		ns	C_L = 15 pF
t_h	Hold Time, D_n to E_0 or E_1	50	25		25	13			7		ns	Input Transition
t_wE_n	Minimum Enable Pulse Width	80	40		32	16			12		ns	Times ⩽ 20 ns

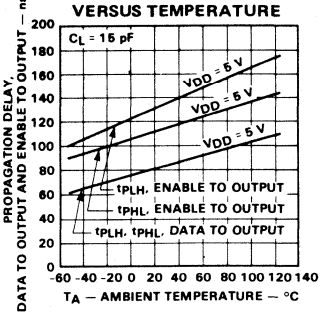
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

TYPICAL ELECTRICAL CHARACTERISTICS

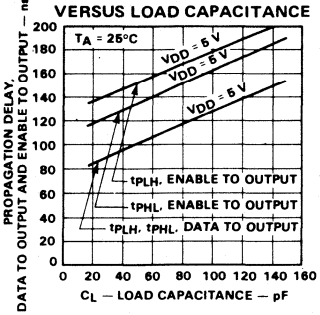
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



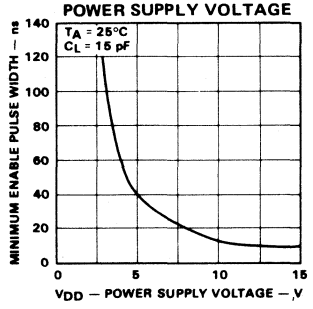
PROPAGATION DELAY VERSUS TEMPERATURE



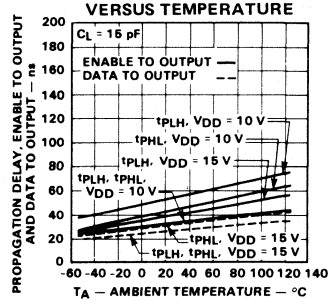
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



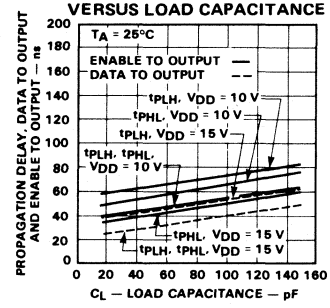
MINIMUM ENABLE PULSE WIDTH VERSUS POWER SUPPLY VOLTAGE



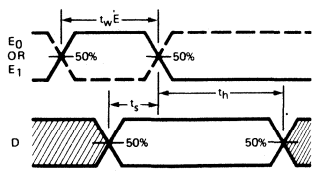
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE

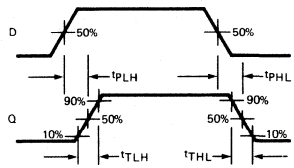


SWITCHING WAVEFORMS

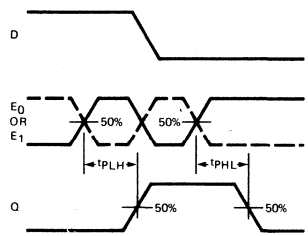


SET-UP AND HOLD TIMES, MINIMUM ENABLE PULSE WIDTH

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table. t_s and t_h are shown as positive values but may be specified as negative values.



PROPAGATION DELAY DATA TO OUTPUT AND TRANSITION TIMES, WITH LATCH ENABLED



PROPAGATION DELAY ENABLE TO OUTPUT

NOTE:
Either E_0 or E_1 is held HIGH or LOW while the other Enable Input is pulsed as per the Truth Table.

F4043/34043

QUAD R/S LATCH WITH 3-STATE OUTPUTS

DESCRIPTION – The F4043 is a Quad R/S Latch with 3-State Outputs with a common Output Enable (EO). Each latch has an active HIGH Set Input (S_n), an active HIGH Reset Input (R_n) and an active HIGH 3-State Output (Q_n).

When the Output Enable Input (EO) is HIGH, the state of the Latch Outputs (Q_n) can be determined from the Truth Table (see below). When the Output Enable Input (EO) is LOW, the Latch Outputs are in the high impedance OFF state. The Output Enable Input (EO) does not affect the state of the latch.

- **3-STATE BUFFERED OUTPUTS (ACTIVE HIGH)**
- **COMMON OUTPUT ENABLE**
- **SET INPUTS TO EACH LATCH (ACTIVE HIGH)**
- **RESET INPUTS TO EACH LATCH (ACTIVE HIGH)**

PIN NAMES

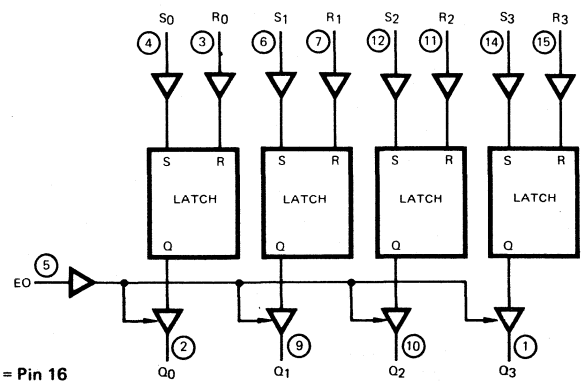
EO	Common Output Enable Input
S_0–S_3	Set Inputs
R_0–R_3	Reset Inputs
Q_0–Q_3	3-State Buffered Latch Outputs

TRUTH TABLE

INPUTS			OUTPUT
EO	S_n	R_n	Q_n
L	X	X	High Impedance
H	H	L	H
H	L	H	L
H	H	H	H
H	L	L	No Change

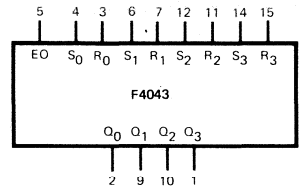
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC DIAGRAM



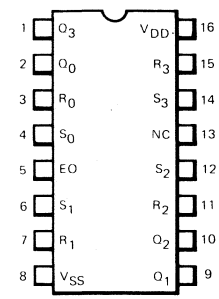
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 13
○ = Pin Number

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

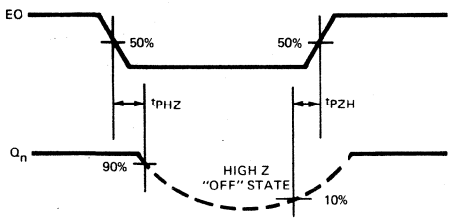
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC		0.05			0.1			0.2		μA	MIN, 25°C	Output Returned to V_{DD}, EO = V_{SS}
				3			6			12			MAX	
		XM		0.005			0.01			0.02			MIN, 25°C	
				0.3			0.6			1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC		−0.05			−0.1			−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, EO = V_{SS}
				−3			−6			−12			MAX	
		XM		−0.005			−0.01			−0.02			MIN, 25°C	
				−0.3			−0.6			−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

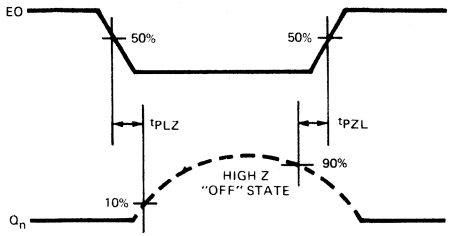
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, S_n to Q_n		90			45			35		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			90			45			35		ns	
t_{PLH}	Propagation Delay, R_n to Q_n		90			45			35		ns	
t_{PHL}			90			45			35		ns	
t_{PZH}	Output Enable Time		35			20			15		ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PZL}			35			20			15		ns	
t_{PHZ}	Output Disable Time		35			20			15		ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PLZ}			35			20			15		ns	
t_{TLH}	Output Transition Time		30			20			15		ns	
t_{THL}			30			20			15		ns	
t_{PLH}	Propagation Delay, S_n to Q_n		100			50			40		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			100			50			40		ns	
t_{PLH}	Propagation Delay, R_n to Q_n		100			50			40		ns	
t_{PHL}			100			50			40		ns	
t_{PZH}	Output Enable Time		40			20			15		ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PZL}			40			20			15		ns	
t_{PHZ}	Output Disable Time		40			20			15		ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PLZ}			40			20			15		ns	
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20		ns	
t_wS_n	Minimum S_n Pulse Width		40			20			15		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_wR_n	Minimum R_n Pulse Width		40			20			15		ns	
t_{rec}	S_n Recovery Time		10			5			3		ns	
t_{rec}	R_n Recovery Time		10			5			3		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

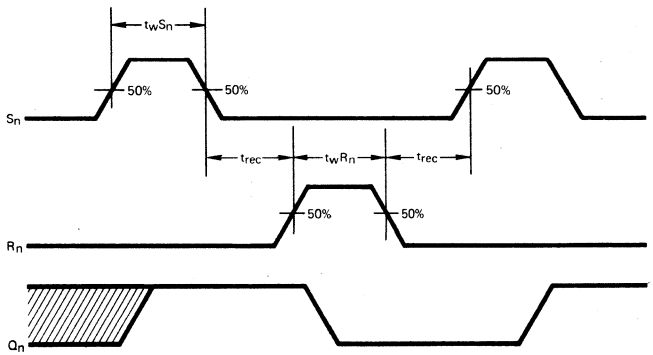
SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



MINIMUM R_N AND S_N PULSE WIDTHS AND RECOVERY TIMES FOR R_N AND S_N

F4044/34044

QUAD R/S LATCH WITH 3-STATE OUTPUTS

DESCRIPTION – The F4044 is a Quad R/S Latch with 3-state Outputs with a common Output Enable Input (EO). Each latch has an active LOW Set Input (S_n), an active LOW Reset Input (R_n) and an active HIGH 3-State Output (Q_n).

When the Output Enable Input (EO), is HIGH, the state of the Latch Outputs (Q_n) can be determined from the Truth Table (see below). When the Output Enable Input (EO) is LOW, the Latch Outputs are in the high impedance OFF state. The Output Enable Input (EO) does not affect the state of the latch.

- **3-STATE BUFFERED OUTPUTS (ACTIVE HIGH)**
- **COMMON OUTPUT ENABLE**
- **SET INPUTS TO EACH LATCH (ACTIVE LOW)**
- **RESET INPUTS TO EACH LATCH (ACTIVE LOW)**

PIN NAMES

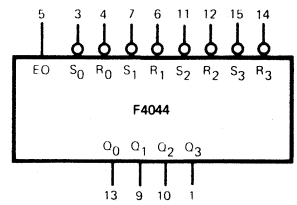
EO	Output Enable Input
$\overline{S_0}$–$\overline{S_3}$	Set Inputs (Active LOW)
$\overline{R_0}$–$\overline{R_3}$	Reset Inputs (Active LOW)
Q_0–Q_3	3-State Buffered Latch Outputs

TRUTH TABLE

INPUTS			OUTPUT
EO	$\overline{S}_n$	$\overline{R}_n$	Q_n
L	X	X	High Impedance
H	L	H	H
H	H	L	L
H	L	L	L
H	H	H	No Change

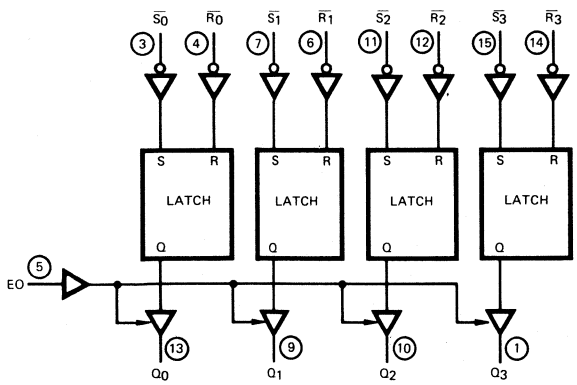
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC SYMBOL



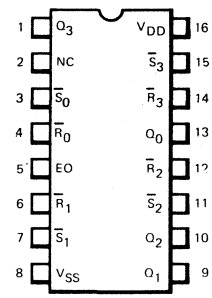
V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 2

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
NC = Pin 2
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpack version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

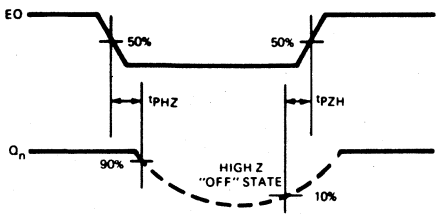
SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC		0.05			0.1			0.2		μA	MIN, 25°C	Output Returned to V_{DD}, EO = V_{SS}
				3			6			12			MAX	
		XM		0.005			0.01			0.02			MIN, 25°C	
				0.3			0.6			1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC		−0.05			−0.1			−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, EO = V_{SS}
				−3			−6			−12			MAX	
		XM		−0.005			−0.01			−0.02			MIN, 25°C	
				−0.3			−0.6			−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					140			280		56			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					60			120		24			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

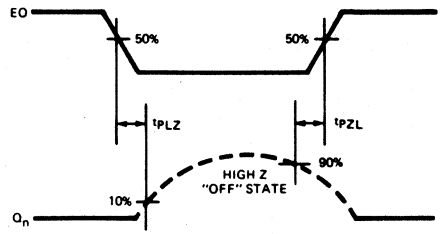
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, $\overline{S_n}$ to Q_n		90			45			35		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			90			45			35		ns	
t_{PLH}	Propagation Delay, $\overline{R_n}$ to Q_n		90			45			35		ns	
t_{PHL}			90			45			35		ns	
t_{PZH}	Output Enable Time		35			20			15		ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			35			20			15		ns	(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		35			20			15		ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			35			20			15		ns	(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		30			20			15		ns	
t_{THL}			30			20			15		ns	
t_{PLH}	Propagation Delay, $\overline{S_n}$ to Q_n		100			50			40		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			100			50			40		ns	
t_{PLH}	Propagation Delay, $\overline{R_n}$ to Q_n		100			50			40		ns	
t_{PHL}			100			50			40		ns	
t_{PZH}	Output Enable Time		40			20			15		ns	(R_L = 1 kΩ to V_{SS})
t_{PZL}			40			20			15		ns	(R_L = 1 kΩ to V_{DD})
t_{PHZ}	Output Disable Time		40			20			15		ns	(R_L = 1 kΩ to V_{SS})
t_{PLZ}			40			20			15		ns	(R_L = 1 kΩ to V_{DD})
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20		ns	
$t_{w\overline{S_n}}$	Minimum $\overline{S_n}$ Pulse Width		40			20			15		ns	
$t_{w\overline{R_n}}$	Minimum $\overline{R_n}$ Pulse Width		40			20			15		ns	
t_{rec}	$\overline{S_n}$ Recovery Time		10			5			3		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{rec}	$\overline{R_n}$ Recovery Time		10			5			3		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

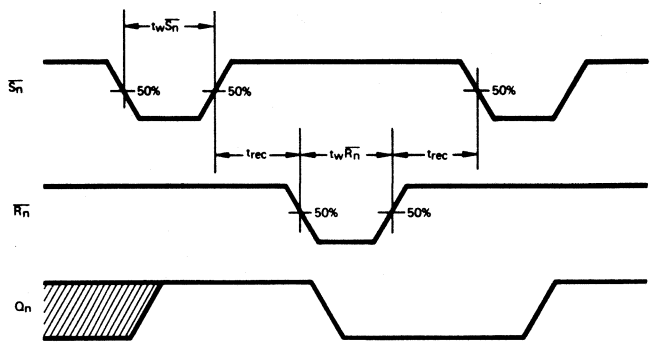
SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



MINIMUM $\overline{S_N}$ AND $\overline{R_N}$ PULSE WIDTHS AND RECOVERY TIMES FOR $\overline{S_N}$ AND $\overline{R_N}$

F4046/34046
MICROPOWER PHASE-LOCKED LOOP

DESCRIPTION – The F4046 is a Micropower Phase-Locked Loop consisting of a low power linear Voltage-Controlled Oscillator, a Source Follower Circuit, two different Phase Comparators, and a Zener diode. The Voltage-Controlled Oscillator has two External Capacitor connections (C_{exta}, C_{extb}), two External Resistor connections (R_{exta}, R_{extb}), a Voltage-Controlled Oscillator Input (I_{VCO}) and a Voltage-Controlled Oscillator Output (O_{VCO}). The Source Follower Circuit provides a Demodulated Output (O_D) from the Voltage-Controlled Oscillator. An active LOW Enable Input ($\overline{E}$) common to both the Voltage-Controlled Oscillator and the Source Follower Circuit is also provided. Phase Comparator I and Phase Comparator II have common Signal (I_S) and Comparator (I_C) Inputs and separate outputs; Phase Comparator I Output (O_{PCI}), Phase Comparator II Output (O_{PCII}), and Phase Pulse Output (O_{PII}). An input to the Zener diode (I_Z) is also provided.

The Voltage-Controlled Oscillator requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. A second external resistor (R_2) may be used to allow frequency offset. External resistor R_3 and external capacitor C_2 combined serve as a low pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). Output O_D is provided to avoid loading the low pass filter. External resistor R_4 is required if this output is utilized. O_D must be left open when not utilized. The output from the Voltage-Controlled Oscillator (O_{VCO}) may be connected directly or indirectly through CMOS frequency dividers (i.e., the F4018, F4020, F4022, F4024, F4029, F4040, F4518, F4520, F40160, F40161, F40162, F40163, F40192, or F40193) to the Comparator Input (I_C). With the Enable Input ($\overline{E}$) HIGH both the Voltage-Controlled Oscillator and the Source Follower Circuit are OFF to minimize power consumption. With $\overline{E}$ LOW, both are enabled.

For direct-coupling between O_{VCO} and I_C, the voltage swing at the Voltage-Controlled Oscillator Output (O_{VCO}) must be within standard CMOS logic levels ($V_{OH} \geq 0.7 \times V_{DD}$ and $V_{OL} \leq 0.3 \times V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the Signal Input (I_S).

Phase Comparator I is an Exclusive OR circuit ($I_C \oplus I_S$). I_C and I_S must have 50% duty cycles to maximize lock range. When the Output of Phase Comparator I (O_{PCI}) is connected back to the Voltage-Controlled Oscillator through the low pass filter network, an averaged voltage to I_{VCO} forces oscillation at a center frequency.

Phase Comparator II is an edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output. Phase Comparator II triggers on LOW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. The Output of Phase Comparator II (O_{PCII}) provides voltage levels and duty cycles corresponding to frequency and phase differentials between I_C and I_S. When O_{PCII} is connected to the Voltage-Controlled Oscillator Input (I_{VCO}) through the low pass filter network, a corresponding voltage across capacitor C_2 is adjusted until the Signal (I_S) and Comparator (I_C) Inputs are equal in both frequency and phase. At this point Phase Comparator II maintains a constant voltage across Capacitor C_2. When this stability has been established, the Phase Pulse Output (O_{PII}) is HIGH indicating a locked condition. Power dissipation in the low pass filter is reduced when Phase Comparator II is used.

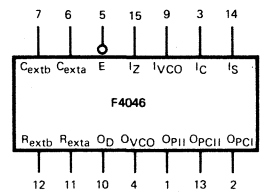
A 5.2 V, on chip zener diode is provided for regulating the power supply voltage, if necessary.

- **CHOICE OF 2-PHASE COMPARATORS**
- **ENABLE INPUT (ACTIVE LOW) FOR LOW POWER DISSIPATION IN STANDBY MODE**
- **ON-CHIP ZENER DIODE FOR SUPPLY REGULATION**

PIN NAMES

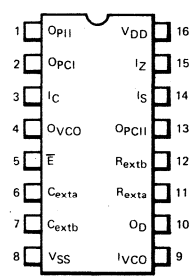
I_Z	Zener Diode Input
I_S	Signal Input
I_C	Comparator Input
I_{VCO}	Voltage-Controlled Oscillator Input
$\overline{E}$	Enable Input (Active LOW)
C_{exta}, C_{extb}	External Capacitor Connections
R_{exta}, R_{extb}	External Resistor Connections
O_{PCI}	Phase Comparator I Output
O_{PCII}	Phase Comparator II Output
O_{PII}	Phase Pulse Output
O_D	Demodulator Output
O_{VCO}	Voltage-Controlled Oscillator Output

LOGIC SYMBOL



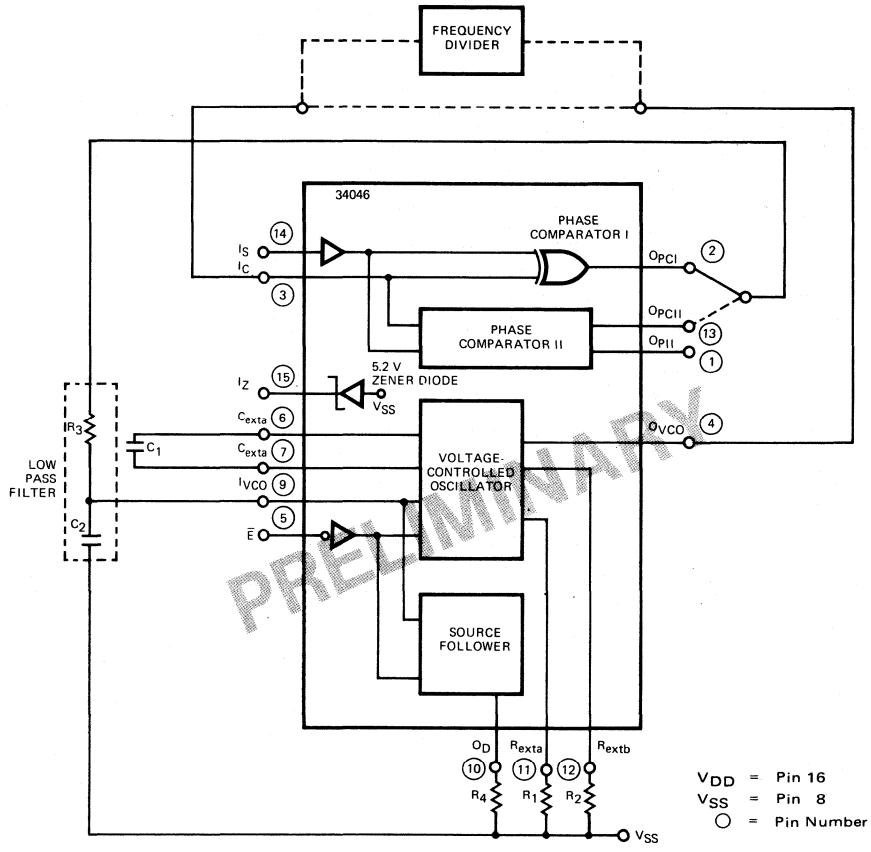
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



F4047/34047

MONOSTABLE/ASTABLE MULTIVIBRATOR

DESCRIPTION — The F4047 is a Monostable/Astable Multivibrator capable of operating in either the monostable or astable mode. Operation in either mode requires an external capacitor (C_x) between pins 1 and 3 (C_{ext},R_{ext}/C_{ext}) and an external resistor (R_x) between pins 2 and 3 (R_{ext},R_{ext}/C_{ext}). These external timing components (R_x,C_x) determine the output pulse width in the monostable mode and the output frequency in the astable mode. The F4047 also has active HIGH and active LOW astable mode Enable Inputs (E_{A0},$\overline{E}_{A1}$), active HIGH and active LOW Trigger Inputs (T_0,$\overline{T}_1$) for operation in the monostable mode, a Retrigger Input (I_{RT}), an Oscillator Output (O), active HIGH and active LOW flip-flop Outputs (Q,$\overline{Q}$) and an overriding asynchronous Master Reset Input (MR).

ASTABLE OPERATION. Astable operation is obtained by either a HIGH on the E_{A0} input or a LOW on the $\overline{E}_{A1}$ input. The frequency of the 50% duty cycle output at the Q and $\overline{Q}$ outputs is determined by the external timing components (R_x,C_x). A frequency twice that of the Q and $\overline{Q}$ outputs is available at the Oscillator Output (O). However, a 50% duty cycle is not guaranteed. The F4047 can be used as a gated oscillator by controlling the E_{A0} and $\overline{E}_{A1}$ inputs.

MONOSTABLE OPERATION. Monostable operation is obtained by connecting the E_{A0} input LOW and the $\overline{E}_{A1}$ input HIGH. The device can be triggered by either a LOW-to-HIGH transition at the T_0 input while the $\overline{T}_1$ input is LOW or a HIGH-to-LOW transition at the $\overline{T}_1$ input while the T_0 is HIGH. The output pulse width at Q and $\overline{Q}$ is determined by the external timing components (R_x,C_x). The device can be retriggered by applying a simultaneous LOW-to-HIGH transition to both the Retrigger Input (I_{RT}) and the T_0 input while the $\overline{T}_1$ input is LOW.

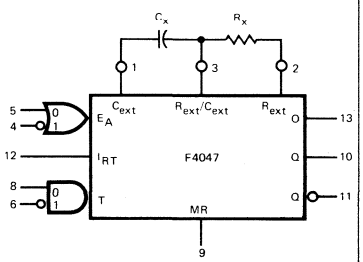
A HIGH on the Master Reset Input (MR) resets the output flip-flop (Q = LOW,$\overline{Q}$ =HIGH) independent of all other input conditions.

- **MONOSTABLE OR ASTABLE OPERATION**
- **TRUE AND COMPLEMENTARY BUFFERED OUTPUTS**
- **ENABLED WITH EITHER A LOW OR A HIGH LEVEL IN THE ASTABLE MODE**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION IN THE MONOSTABLE MODE**
- **ASYNCHRONOUS MASTER RESET**

PIN NAMES

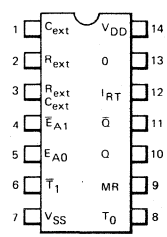
C_{ext}	External Capacitor Connection
R_{ext}	External Resistor Connection
R_{ext}/C_{ext}	Common External Capacitor and Resistor Connection
I_{RT}	Retrigger Input
T_0	Trigger Input (L → H Triggered)
$\overline{T}_1$	Trigger Input (H → L Triggered)
E_{A0}	Enable Input (Active HIGH)
$\overline{E}_{A1}$	Enable Input (Active LOW)
MR	Master Reset
O	Oscillator Output
Q,$\overline{Q}$	True and Complementary Buffered Outputs

LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)

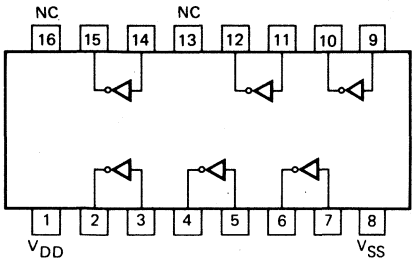


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4049 HEX INVERTING BUFFER • F4050 HEX NON-INVERTING BUFFER

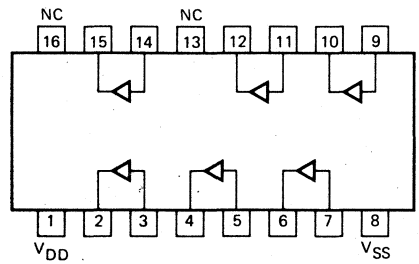
DESCRIPTION – These CMOS buffers provide high current output capability suitable for driving TTL or high capacitance loads. Since input voltages in excess of the buffers' supply voltage are permitted, these buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. The F4049 provides six inverting buffers, the F4050 six non-inverting buffers. Their guaranteed fan out into common bipolar logic elements is shown in Table 1.

F4049
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

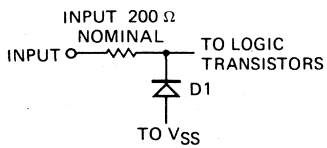


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4050
LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



INPUT PROTECTION



NOTE: Typical Breakdown Voltage of Diode D1 is 20 V.

TABLE 1
Guaranteed fan out of F4049, F4050 into common logic families

DRIVEN ELEMENT	GUARANTEED FAN OUT
Standard TTL, DTL	2
9LS, 93L, 74LS	9
74L	16

Conditions: $V_{DD} = V_{CC} = 5.0 \pm 0.25$ V
$V_{OL} \leq 0.5$ V, $T_A = 0$ to 75 °C

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V, F4049XM and F4050XM (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.85									mA	MIN	$V_{OUT} = 2.5$ V for $V_{DD} = 5$ V
		-1.25	-2.5								mA	25°C	Inputs at 0 or V_{DD}
		-0.9									mA	MAX	per Function
		-0.62			-1.85				-5.2		mA	MIN	$V_{OUT} = 4.5$ V for $V_{DD} = 5$ V $V_{OUT} = 9.5$ V for $V_{DD} = 10$ V
		-0.5	-1.0		-1.25	-2.5			-4.7		mA	25°C	$V_{OUT} = 14.5$ V for $V_{DD} = 15$ V
		-0.35			-0.9				-3.5		mA	MAX	Inputs at 0 or V_{DD} per Function
I_{OL}	Output LOW Current	3.75			10.0				24.5		mA	MIN	$V_{OUT} = 0.4$ V for $V_{DD} = 5$ V $V_{OUT} = 0.5$ V for $V_{DD} = 10$ V
		3.0	6.0		8.0	16.0			22.0		mA	25°C	$V_{OUT} = 0.5$ V for $V_{DD} = 15$ V
		2.1			5.6				16.8		mA	MAX	Inputs at 0 or V_{DD} per Function
		3.3									mA	MIN	$V_{OUT} = 0.4$ V for $V_{DD} = 4.5$ V
		2.6	5.2								mA	25°C	Inputs at 0 V or V_{DD}
		1.8									mA	MAX	per Function
I_{DD}	Quiescent Power Supply Current			0.3			0.5		0.1		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
				20.0			30.0		6.0			MAX	

Notes on the following page.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, F4049XC and F4050XC (Cont'd) (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OH}	Output HIGH Current	-1.5									mA	MIN	V_{OUT} = 2.5 V for V_{DD} = 5 V
		-1.25	-2.5								mA	25°C	Inputs at 0 or V_{DD}
		-1.0									mA	MAX	per Function
		-0.6			-1.5				-5.2		mA	MIN	V_{OUT} = 4.5 V for V_{DD} = 5 V V_{OUT} = 9.5 V for V_{DD} = 10 V V_{OUT} = 14.5 V for V_{DD} = 15 V
		-0.5	-1.0		-1.25	-2.5			-4.7		mA	25°C	
		-0.4			-1.0				-4.0		mA	MAX	Inputs at 0 or V_{DD} per Function
I_{OL}	Output LOW Current	3.6			9.6				24.5		mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 5 V V_{OUT} = 0.5 V for V_{DD} = 10 V V_{OUT} = 0.5 V for V_{DD} = 15 V
		3.0	6.0		8.0	16.0			22.0		mA	25°C	
		2.5			6.6				19.0		mA	MAX	Inputs at 0 or V_{DD} per Function
		3.1									mA	MIN	V_{OUT} = 0.4 V for V_{DD} = 4.5 V
		2.6	5.2								mA	25°C	Inputs at 0 V or V_{DD}
		2.1									mA	MAX	per Function
I_{DD}	Quiescent Power Supply Current			3.0			5.0		1.0		µA	MIN,25°C	All inputs common
				42.0			70.0		14.0			MAX	and at 0 V or V_{DD}

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, F4049 only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		45	90		20	55		15		ns	
t_{PHL}			40	75		20	40		15		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		30	60		17	35		12	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}			20	40		7	20		5	10	ns	
t_{PLH}	Propagation Delay		65	130		30	65		29		ns	
t_{PHL}			50	105		25	50		17		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		73	145		40	80		30	60	ns	Input Transition Times ⩽ 20 ns
t_{THL}			33	65		13	25		9	20	ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

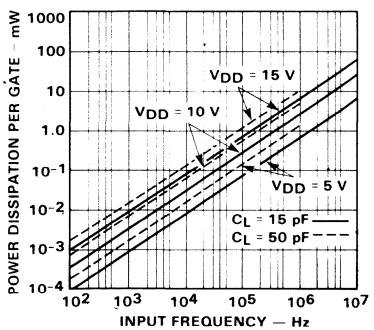
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C, F4050 only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		45	90		20	55		15		ns	
t_{PHL}			30	60		17	35		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		30	60		17	35		12	25	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		20	40		7	20		5	10	ns	
t_{PLH}	Propagation Delay		65	130		30	65		24		ns	
t_{PHL}			43	95		23	45		17		ns	C_L = 50 pF
t_{TLH}	Output Transition		73	145		90	80		30	60	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		33	65		13	25		9	20	ns	

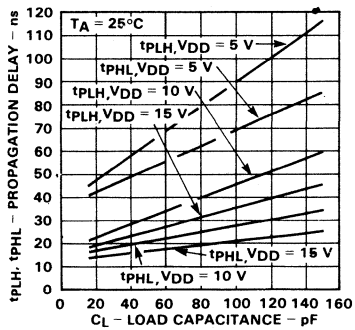
Notes on preceeding page.

TYPICAL ELECTRICAL CHARACTERISTICS

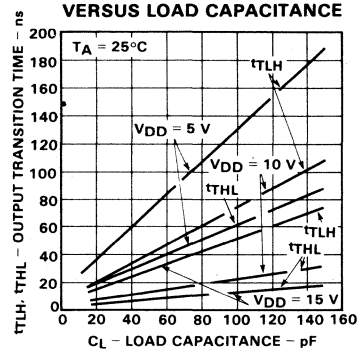
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



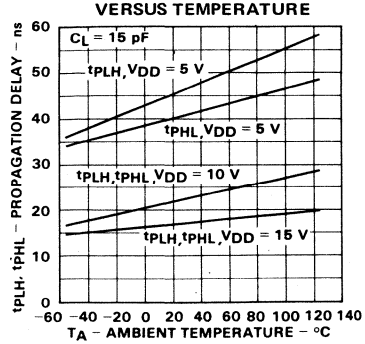
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



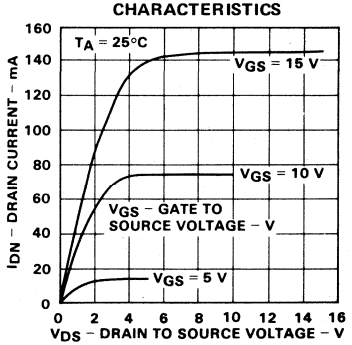
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



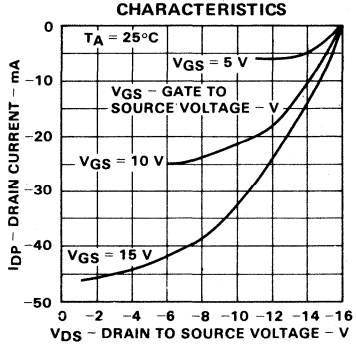
PROPAGATION DELAY VERSUS TEMPERATURE



N-CHANNEL DRAIN CHARACTERISTICS



P-CHANNEL DRAIN CHARACTERISTICS



F4051/34051

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The F4051 is an 8-Channel Analog Multiplexer/Demultiplexer with three Address Inputs (A_0-A_2), an active LOW Enable Input ($\overline{E}$), eight Independent Inputs/Outputs (Y_0-Y_7) and a Common Input/Output (Z).

The F4051 contains eight bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0-Y_7) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the eight switches is selected (low impedance, ON state) by the three Address Inputs (A_0-A_2). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0-A_2, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0-Y_7, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

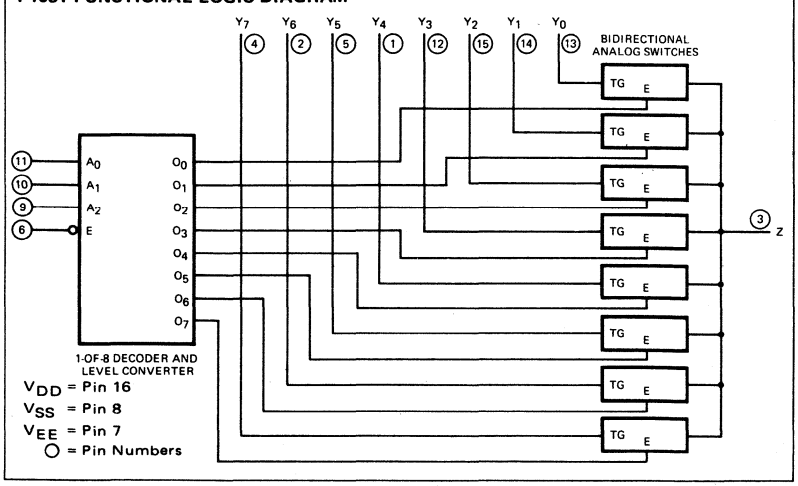
Y_0-Y_7	Independent Inputs/Outputs
A_0-A_2	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Common Input/Output

TRUTH TABLE

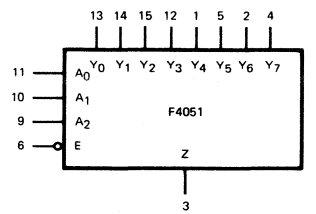
INPUTS				CHANNELS							
$\overline{E}$	A_2	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z	Y_4–Z	Y_5–Z	Y_6–Z	Y_7–Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

L = LOW Level
H = HIGH Level
X = Don't Care

F4051 FUNCTIONAL LOGIC DIAGRAM

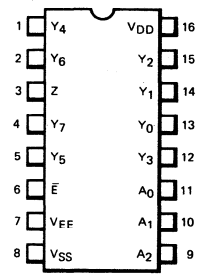


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95			55			35		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				95			55			35		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				1600			110			55		Ω	MIN	
				1000			125			60			25°C	Note 3
				850			200			95			MAX	
		XM		90			50			30		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				90			50			30		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				1750			100			50		Ω	MIN	
				1000			125			60			25°C	Note 3
				700			220			100			MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels						10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\bar{E} = V_{DD}$, $V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						80						
	Any Channel OFF	XC						100						$\bar{E} = V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40		8		μA	MIN,25°C	$V_{SS} = V_{EE}$ All inputs common and and at V_{DD} or V_{EE}
					700			1400		280			MAX	
		XM			2			4		0.8		μA	MIN,25°C	
					70			140		28			MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 4)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		20 8			7 4			4 3		ns ns	C_L = 15 pF, $\overline{E}$ = V_{SS} = V_{EE}, A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		160 200			90 120			75 90		ns ns	
t_{PZL} t_{PZH}	Output Enable Time		180 200			90 100			70 80		ns ns	C_L = 15 pF, $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1000 1000			900 900			860 850		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		25 10			10 6			6 4		ns ns	C_L = 50 pF $\overline{E}$ = V_{SS} = V_{EE},
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		170 210			95 125			80 95		ns ns	A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PZL} t_{PZH}	Output Enable Time		185 205			95 105			75 85		ns ns	C_L = 50 pF, $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1250 1240			1130 1120			1080 1070		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	C_L = 15 pF R_L = 10 kΩ, V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ, $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) at −40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = −40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (sine wave) 20 Log_{10} (V_{os}/V_{is}) = −40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) V_{SS} = $V_{DD}/2$ 20 Log_{10}(V_{os}/V_{is}) = −3 dB

NOTES:
1. Additional DC Characteristics for the Address and Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or $V_{DD/2}$.
3. V_{is} = 8.6 V for V_{DD} = 15 V.
   V_{is} = 5.1 V for V_{DD} = 10 V
   V_{is} = 1.9 V for V_{DD} = 5 V
4. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
5. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
6. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns, R_L = 10 kΩ.

F4052/34052

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The F4052 is a Dual 4-Channel Analog Multiplexer/Demultiplexer with common channel select logic. Each Multiplexer/Demultiplexer has four Independent Inputs/Outputs (Y_0-Y_3) and a Common Input/Output (Z). The common channel select logic includes two Address Inputs (A_0, A_1) and an active LOW Enable Input ($\bar{E}$).

Both multiplexer/demultiplexers contain four bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0-Y_3) and the other side connected to a Common Input/Output (Z). With the Enable Input LOW, one of the four switches is selected (low impedance, ON state) by the two Address Inputs. With the Enable Input HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0, A_1, $\bar{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0-Y_3, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **DIGITAL OR ANALOG MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

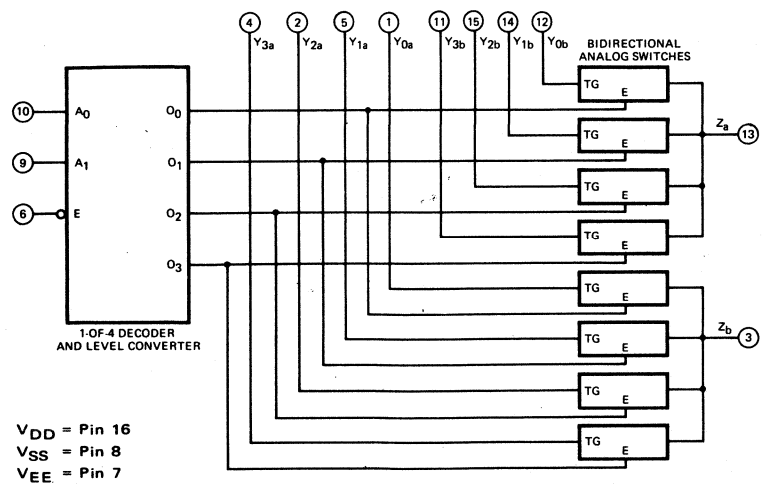
Y_{0a}-Y_{3a}	Independent Inputs/Outputs
Y_{0b}-Y_{3b}	Independent Inputs/Outputs
A_0, A_1	Address Inputs
$\bar{E}$	Enable Input (Active LOW)
Z_a, Z_b	Common Input/Output

TRUTH TABLE

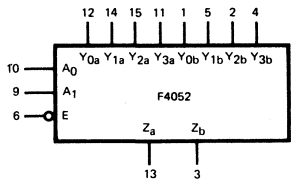
INPUTS			CHANNELS			
$\bar{E}$	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

L = LOW Level, H = HIGH Level, X = Don't care.

F4052 FUNCTIONAL LOGIC DIAGRAM

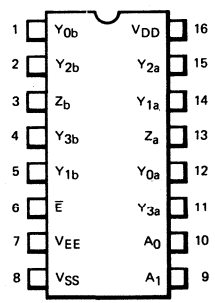


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
R_{ON}	ON Resistance	XC		95			55			35		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				95			55			35		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				125			100			65			MAX	
				1600			110			55		Ω	MIN	
				1000			125			60			25°C	Note 3
				850			200			95			MAX	
		XM		90			50			30		Ω	MIN	$V_{is} = V_{DD}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				90			50			30		Ω	MIN	$V_{is} = V_{EE}$
				100			65			40			25°C	Note 2
				150			110			70			MAX	
				1750			100			50		Ω	MIN	
				1000			125			60			25°C	Note 3
				700			220			100			MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels						10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\overline{E} = V_{DD}$, $V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						80						
	Any Channel OFF	XC						100						$\overline{E} = V_{SS} = V_{DD}/2$ $V_{is} = V_{DD}$ or V_{EE}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40		8		μA	MIN,25°C	$V_{SS} = V_{EE}$ All Inputs Common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			2			4		0.8		μA	MIN,25°C	
					70			140		28			MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 4)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		20 8			7 4			4 3		ns ns	C_L = 15 pF, $\overline{E}$ = V_{SS} = V_{EE}, A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		160 200			90 120			75 90		ns ns	
t_{PZL} t_{PZH}	Output Enable Time		180 200			90 100			70 80		ns ns	C_L = 15 pF $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1000 1000			900 900			860 850		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
t_{PLH} t_{PHL}	Propagation Delay, Input to Output		25 10			10 6			6 4		ns ns	C_L = 50 pF $\overline{E}$ = V_{SS} = V_{EE},
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		170 210			95 125			80 95		ns ns	A_n or V_{is} = V_{DD} or V_{EE} Note 6
t_{PZL} t_{PZH}	Output Enable Time		185 205			95 105			75 85		ns ns	C_L = 50 pF $\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ} t_{PHZ}	Output Disable Time		1250 1240			1130 1120			1080 1070		ns ns	V_{is} = V_{DD} or V_{EE} Note 6
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	C_L = 15 pF R_L = 10 kΩ , V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{EE}, V_{is} = $V_{DD}/2$ (sine wave) f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ , $\overline{E}$ = V_{EE} V_{is} = $V_{DD}/2$ (sine wave) at −40 dB V_{SS} = $V_{DD}/2$, 20 Log_{10} (V_{os}/V_{is}) = −40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ , V_{SS} = $V_{DD}/2$ $\overline{E}$ = V_{DD} V_{is} = $V_{DD}/2$ (sine wave) 20 Log_{10} (V_{os}/V_{is}) = −40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ , $\overline{E}$ = V_{SS} V_{is} = $V_{DD}/2$ (sine wave) V_{SS} = $V_{DD}/2$ 20 Log_{10} (V_{os}/V_{is}) = −3 dB

NOTES:
1. Additional DC Characteristics for the Address and Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or $V_{DD}/2$.
3. V_{is} = 8.6V for V_{DD} = 15V
   V_{is} = 5.1V for V_{DD} = 10V
   V_{is} = 1.9V for V_{DD} = 5V
4. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
5. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).
6. V_{IN} = V_{DD} (Square Wave), Input Transition Times ≤20 ns and R_L = 10 kΩ.

F4053/34053

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The F4053 is a Triple 2-Channel Analog Multiplexer/Demultiplexer with a common Enable Input ($\overline{E}$). Each Multiplexer/Demultiplexer has two Independent Inputs/Outputs (Y_0,Y_1), a Common Input/Output (Z), and a Select Input (S). Each multiplexer/demultiplexer contains two bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0,Y_1) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the two switches is selected (low impedance, ON state) by the Select Input (S). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Select Inputs (S_a-S_c).

V_{DD} and V_{SS} are the two supply voltage connections for the Digital Control Inputs (S_a,S_c,$\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog Inputs/Outputs (Y_0,Y_1,Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}-V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

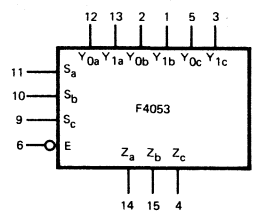
Y_{0a}-Y_{0c}, Y_{1a}-Y_{1c}	Independent Input/Outputs
S_a-S_c	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a-Z_c	Common Input/Outputs

TRUTH TABLE

INPUTS		CHANNELS	
$\overline{E}$	S	Y_0-Z	Y_1-Z
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF

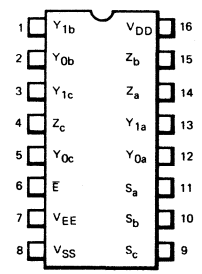
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4066/34066
QUAD BILATERAL SWITCHES

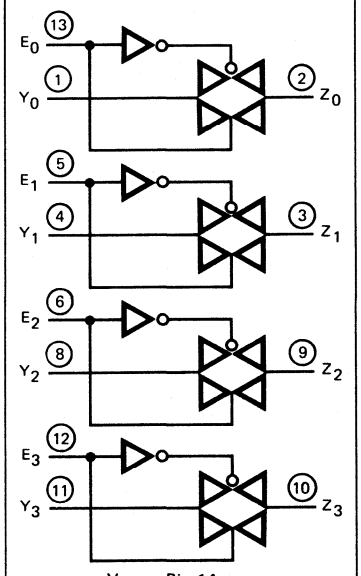
DESCRIPTION – The F4066 has four independent bilateral analog switches (transmission gates). Each switch has two Input/Output Terminals (Y_n, Z_n) and an active HIGH Enable Input (E_n). A HIGH on the Enable Input establishes a low impedance bidirectional path between Y_n and Z_n (ON condition). A LOW on the Enable Input disables the switch; high impedance between Y_n and Z_n (OFF condition).

- **DIGITAL OR ANALOG SIGNAL SWITCHING**
- **INDIVIDUAL ENABLE INPUTS (ACTIVE HIGH)**

PIN NAMES

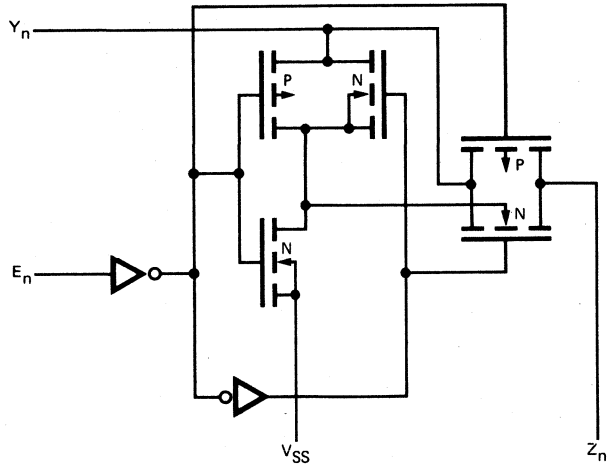
E_0 - E_3	Enable Inputs
Y_0 - Y_3	Input/Output Terminals
Z_0 - Z_3	Input/Output Terminals

LOGIC SYMBOL

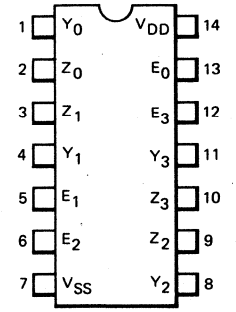


V_{DD} = Pin 14
V_{SS} = Pin 7
○ = Pin Numbers

LOGIC DIAGRAM (1/4 OF A F4066)



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		190	900		100	450		80	250	Ω	MIN	R_L = 10 kΩ
				270	1000		120	500		80	280		25°C	E_n = V_{DD},
				330	1090		170	520		130	300		MAX	V_{is} = V_{DD} to V_{SS}
		XM		160	850		85	400		60	220	Ω	MIN	R_L = 10 kΩ
				270	1000		120	500		80	280		25°C	E_n = V_{DD},
				360	1150		190	550		145	320		MAX	V_{is} = V_{DD} to V_{SS}
ΔR_{ON}	"Δ" ON Resistance Between Any Two Switches						10			5		Ω	25°C	V_{is} = V_{DD} to V_{SS}, E_n = V_{DD} R_L = 10 kΩ
I_Z	OFF State Leakage Current, Any Y to Z							100			100	nA	25°C	V_{is} = V_{DD} or V_{SS}, E_n = V_{SS}
I_{DD}	Quiescent Power Supply Current	XC			0.25			0.5		0.1		μA	MIN, 25°C	All inputs common and at V_{DD} or V_{SS}
					25			30		6			MAX	
		XM			0.25			0.5		0 1		μA	MIN, 25°C	
					25			30		6			MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C(See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		4 3			1.5 1.5			1 1		ns	C_L = 15 pF, R_L = 10 kΩ Input Transition Times ⩽ 20 ns $E_n = V_{DD}$ $V_{is} = V_{DD}$ (square wave)
t_{PZL} t_{PZH}	Output Enable Time		24 24			14 14			10 10		ns ns	C_L = 15 pF, R_L = 300Ω $E_n = V_{DD}$ (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		160 160			170 170			182 182		ns ns	Input Transition Times ⩽ 20 ns $V_{is} = V_{DD}$
t_{PLH} t_{PHL}	Propagation Delay, Y_n to Z_n or Z_n to Y_n		8 8			3 4			2 2.5		ns ns	C_L = 50 pF, R_L = 10 kΩ Input Transition Times ⩽ 20 ns $E_n = V_{DD}$ $V_{is} = V_{DD}$ (square wave)
t_{PZL} t_{PZH}	Output Enable Time		32 32			16 16			13 13		ns ns	C_L = 50 pF, R_L = 300Ω $E_n = V_{DD}$ (square wave)
t_{PLZ} t_{PHZ}	Output Disable Time		380 380			380 380			400 400		ns ns	Input Transition Times ⩽ 20 ns $V_{is} = V_{DD}$
	Distortion, Sine Wave Response		0.31			0.31			0.31		%	C_L = 15 pF, R_L = 10 kΩ Input Frequency = 1 kHz $E_n = V_{DD}$ $V_{is} = V_{DD}/2$ (sine wave)
	Crosstalk Between Any Two Switches					0.9					MHz	R_L = 1 kΩ $E_A = V_{DD}$, $E_B = V_{SS}$ $V_{is} = V_{DD}/2$ (sine wave) at -50 dB, 20 Log_{10} [V_{os} (B)/V_{is} (A)] = -50 dB
	Crosstalk, Enable Input to Output					50					mV	Input Transition Times ⩽ 20 ns $R_{L(OUT)}$ = 10 kΩ, $R_{L(IN)}$ = 1 kΩ $E_n = V_{DD}$ (square wave)
	OFF State Feedthrough					1.25					MHz	R_L = 1 kΩ $E_n = V_{SS}$, $V_{is} = V_{DD}/2$(sine wave) 20 Log_{10} (V_{os}/V_{is}) = -50 dB
	ON State Frequency Response					90					MHz	R_L = 1 kΩ $V_{is} = V_{DD}/2$ (sine wave) $E_n = V_{DD}$, 20 Log_{10} (V_{os}/V_{is}) = -3 dB
f_{MAX}	Enable Input Frequency (Note 3)					10					MHz	C_L = 15 pF, R_L = 1 kΩ Input Transition Times ⩽ 20 ns $E_n = V_{DD}$ (square wave) $V_{is} = V_{DD}$

NOTES:
1. Additional DC Characteristics for the Enable Inputs are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. V_{is}/V_{os} is the voltage signal at an Input/Output Terminal (Y_n/Z_n).

F4067/34067

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

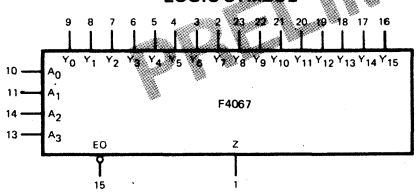
DESCRIPTION – The F4067 is a 16-Channel Analog Multiplexer/Demultiplexer with four Address Inputs (A_0-A_3), 16 Independent Inputs/Outputs (Y_0-Y_{15}), an active LOW Output Enable input ($\overline{EO}$), and a Common Input/Output (Z). The F4067 contains 16 bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0-Y_{15}) and the other side connected to a Common Input/Output (Z). One of the 16 switches is selected (low impedance, ON state) by the four Address Inputs (A_0-A_3) when the Output Enable input ($\overline{EO}$) is LOW. All unselected switches are in the high impedance OFF state. With the Output Enable input ($\overline{EO}$) HIGH, all 16 switches are in the high impedance OFF state. The Analog Input/Outputs (Y_0-Y_{15},Z) can swing between V_{DD} and V_{SS}. V_{DD}-V_{SS} may not exceed 15 V.

- **ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER**
- **24-PIN PACKAGE**
- **SINGLE POWER SUPPLY**

PIN NAMES

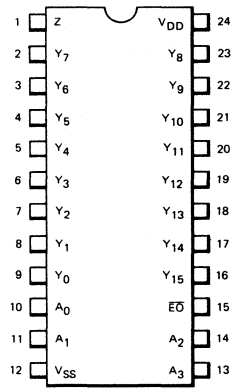
Y_0–Y_{15}	Independent Inputs/Outputs
A_0–A_3	Address Inputs
Z	Common Input/Output
$\overline{EO}$	Output Enable Input (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

INPUTS				CHANNEL														
A_3	A_2	A_1	A_0	Y_0-Z	Y_1-Z	Y_2-Z	Y_3-Z	Y_4-Z	Y_5-Z	Y_6-Z	Y_7-Z	Y_8-Z	Y_9-Z	Y_{10}-Z	Y_{11}-Z	Y_{12}-Z	Y_{13}-Z	Y_{14}-Z	Y_{15}-Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H	L	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
H	L	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
H	L	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
H	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
H	H	L	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
H	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

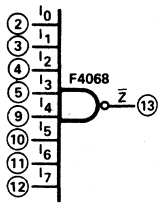
L = LOW Level H = HIGH Level $\overline{EO}$ = LOW Level

8-INPUT NAND GATE

DESCRIPTION – This CMOS logic element provides the positive 8-Input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

F4068 LOGIC SYMBOL

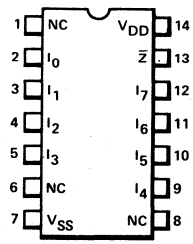
V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8



PIN NAMES

I_0–I_7	NAND Gate Inputs
$\overline{Z}$	Output (Active LOW)

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

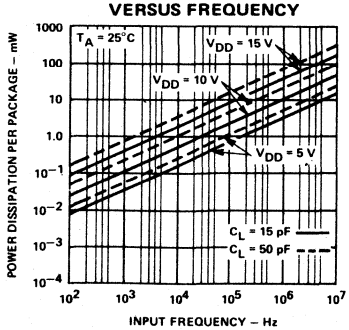
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay		65	160		30	65		22		ns	C_L = 15 pF, Input Transition Times ⩽ 20 ns
t_{PHL}			70	160		32	65		22			
t_{TLH}	Output Transition Time		25	75		13	40		10	25	ns	
t_{THL}			25	75		10	40		8	25		
t_{PLH}	Propagation Delay		82	200		40	85		29		ns	C_L = 50 pF, Input Transition Times ⩽ 20 ns
t_{PHL}			88	200		40	85		28			
t_{TLH}	Output Transition Time		64	135		32	70		24	45	ns	
t_{THL}			55	135		23	70		16	45		

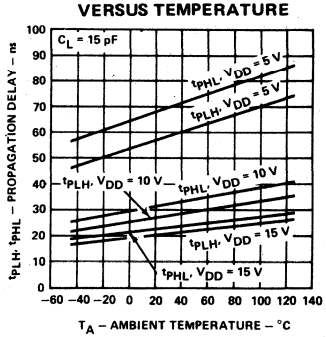
NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

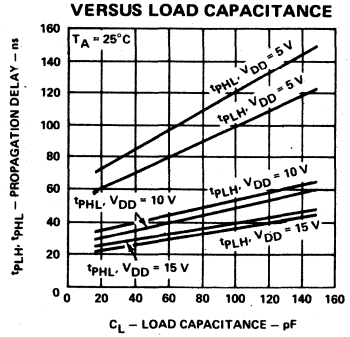
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



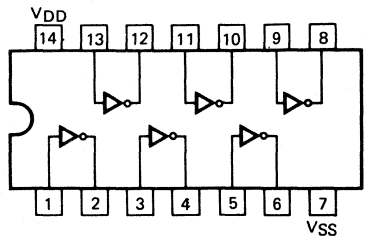
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



HEX INVERTER

DESCRIPTION — The F4069 is a general purpose Hex Inverter which has standard Fairchild input and output characteristics. A single-stage design has been used since the output impedance of a single-input gate is not pattern sensitive.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			3.0			5.0		1.0		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					42.0			70.0		14.0			MAX	
		XM			0.3			0.5		0.1		µA	MIN, 25°C	
					20.0			30.0		6.0			MAX	

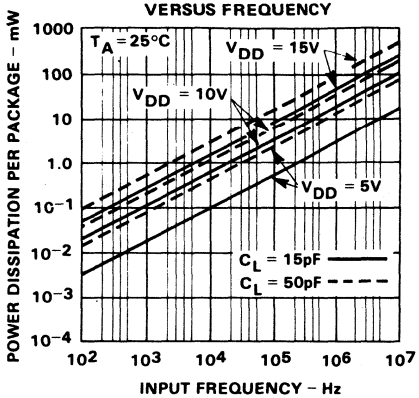
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		20	36		10	20		7		ns	
t_{PHL}			20	36		10	20		7		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		20	45		12	25		11	20	ns	Input Transition Times ≤ 20 ns
t_{THL}			20	45		12	25		11	20	ns	
t_{PLH}	Propagation Delay		32	64		16	32		13		ns	
t_{PHL}			32	64		16	32		13		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		45	135		23	70		18	45	ns	Input Transition Times ≤ 20 ns
t_{THL}			45	135		23	70		18	45	ns	

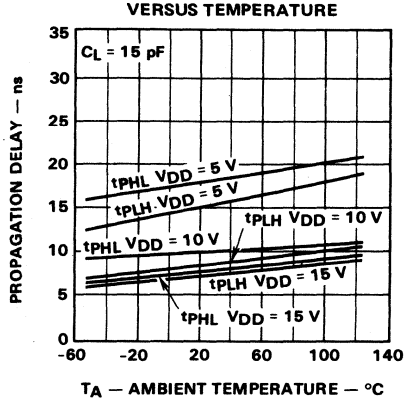
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

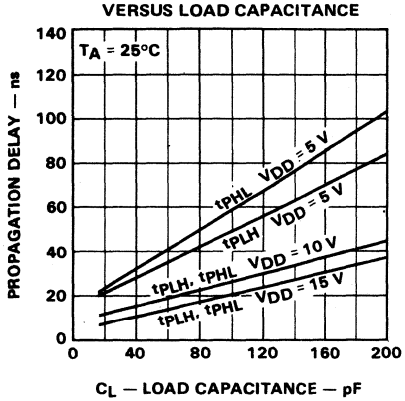
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



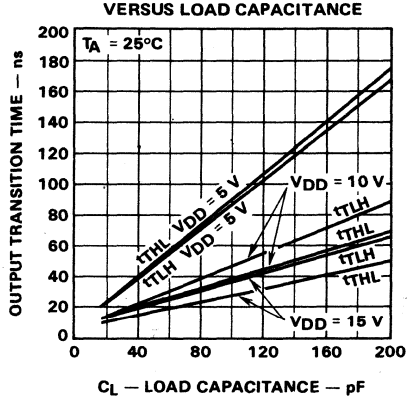
PROPAGATION DELAY VERSUS TEMPERATURE



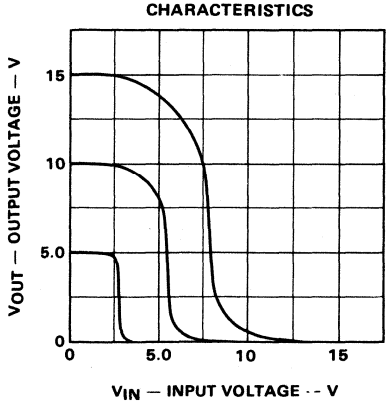
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



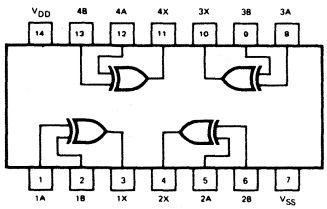
TYPICAL VOLTAGE TRANSFER CHARACTERISTICS



QUAD EXCLUSIVE-OR GATE

DESCRIPTION – The F4070 CMOS logic element provides the Exclusive-OR function. The outputs are fully buffered for best performance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



$X = \bar{A}B + A\bar{B}$

NOTE:
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			5.0			10.0		2.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					70.0			140.0		18.0			MAX	
		XM			0.5			1.0		0.2		μA	MIN, 25°C	
					30.0			60.0		12.0			MAX	

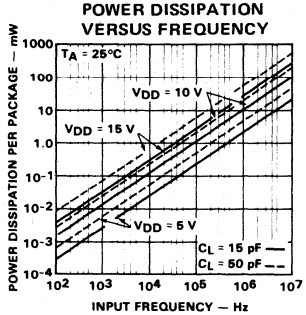
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		65	130		33	65		23		ns	
t_{PHL}	A or B to X		65	130		33	65		23		ns	C_L = 15 pF
t_{TLH}	Output Transition		23	45		10	25		8	20	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		23	45		10	25		8	20	ns	
t_{PLH}	Propagation Delay,		85	170		45	90		27		ns	
t_{PHL}	A or B to X		85	170		45	90		27		ns	C_L = 50 pF
t_{TLH}	Output Transition		50	100		23	50		17	35	ns	Input Transition Times ⩽ 20 ns
t_{THL}	Time		50	100		23	50		17	35	ns	

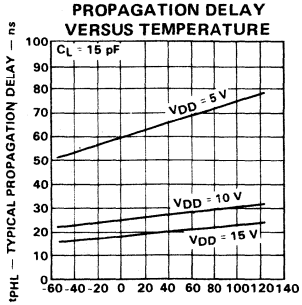
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

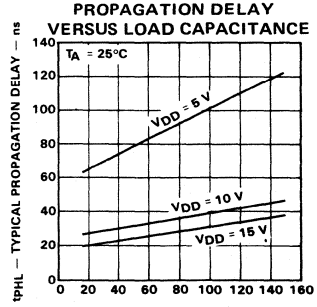
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



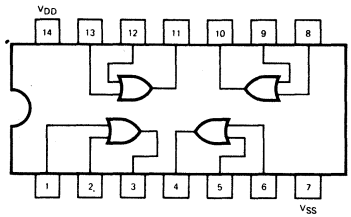
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



QUAD 2-INPUT OR GATE

DESCRIPTION — The F4071 is a positive logic Quad 2-Input OR Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		µA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

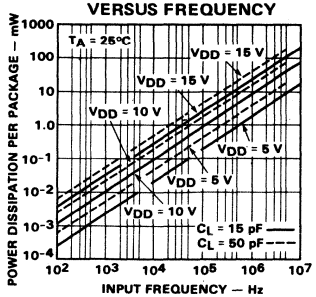
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		30	60		15	30		11		ns	
t_{PHL}			35	60		14	30		11		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		19	75		10	40		8	25	ns	Input Transition Times ≤ 20 ns
t_{THL}			24	75		10	40		7	25	ns	
t_{PLH}	Propagation Delay		43	85		22	40		17		ns	
t_{PHL}			52	100		23	40		15		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		45	135		24	70		18	45	ns	Input Transition Times ≤ 20 ns
t_{THL}			54	135		21	70		15	45	ns	

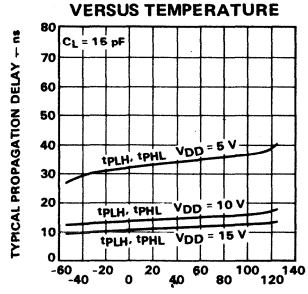
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

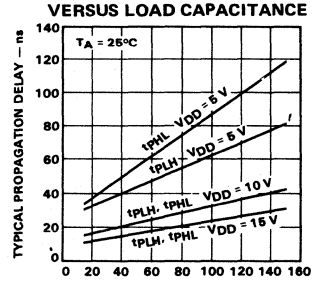
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



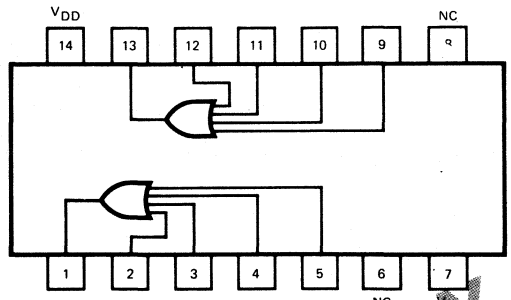
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



DUAL 4-INPUT OR GATE

DESCRIPTION – This CMOS logic element provides the positive Dual 4-Input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEMP	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5		1		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15			30		6			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3			6		1.2			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

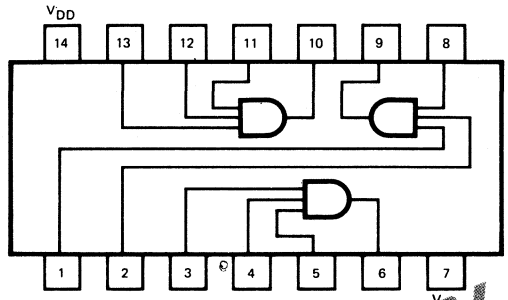
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		50			25			17		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			50			25			17		ns	
t_{TLH}	Output Transition Time		30			15			10		ns	
t_{THL}			30			15			10		ns	
t_{PLH}	Propagation Delay		65			30			20		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			65			30			20		ns	
t_{TLH}	Output Transition Time		70			35			30		ns	
t_{THL}			70			35			30		ns	

NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TRIPLE 3-INPUT AND GATE

DESCRIPTION — This CMOS logic element provides the positive Triple 3-Input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5		1		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15			30		6			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3			6		1.2			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

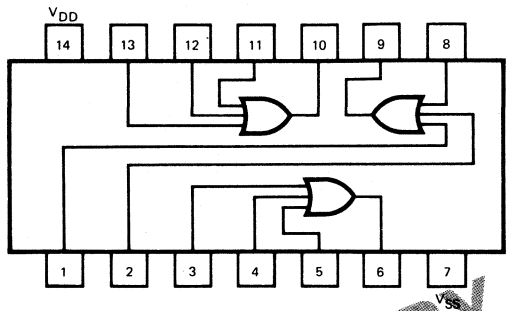
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		60			30			20		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			60			30			20		ns	
t_{TLH}	Output Transition Time		25			15			10		ns	
t_{THL}			25			15			10		ns	
t_{PLH}	Propagation Delay		80			35			25		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			80			35			25		ns	
t_{TLH}	Output Transition Time		70			35			25		ns	
t_{THL}			70			35			25		ns	

NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TRIPLE 3-INPUT OR GATE

DESCRIPTION — This CMOS logic element provides the positive Triple 3-Input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5		1		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15			30		6			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3			6		1.2			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		35			20			15		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			35			20			15		ns	
t_{TLH}	Output Transition Time		15			10			8		ns	
t_{THL}			15			10			8		ns	
t_{PLH}	Propagation Delay		45			25			20		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			45			25			20		ns	
t_{TLH}	Output Transition Time		38			20			15		ns	
t_{THL}			38			20			15		ns	

NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4076/34076

QUAD D FLIP-FLOP WITH 3-STATE OUTPUTS

DESCRIPTION — The F4076 is a Quad Edge-Triggered D Flip-Flop with four Data Inputs (D_0-D_3), two active LOW Data Enable Inputs ($\overline{ED_0}$-$\overline{ED_1}$), an edge-triggered Clock Input (CP), four 3-State Outputs (Q_0-Q_3), two active LOW Output Enable inputs ($\overline{EO_0}$, $\overline{EO_1}$), and an overriding asynchronous Master Reset Input (MR).

Information on the Data Inputs (D_0-D_3) is stored in the four Flip-Flops on the LOW-to-HIGH transition of the Clock Input (CP) if both Data Enable Inputs ($\overline{ED_0}$-$\overline{ED_1}$) are LOW. A HIGH on either Data Enable Input ($\overline{ED_0}$-$\overline{ED_1}$) prevents the Flip-Flops from changing on the LOW-to-HIGH transition of the Clock Input (CP), independent of the information on the Data Inputs (D_0-D_3).

When both Output Enable inputs ($\overline{EO_0}$-$\overline{EO_1}$) are LOW, the contents of the four Flip-Flops are available at the Outputs (Q_0-Q_3). A HIGH on either Output Enable input ($\overline{EO_0}$, $\overline{EO_1}$) forces the Outputs (Q_0-Q_3) into the high impedance OFF state.

A HIGH on the overriding asynchronous Master Reset Input (MR) resets all four Flip-Flops, indepedent of all other input conditions.

- **3-STATE OUTPUTS**
- **CLOCK IS L → H EDGE-TRIGGERED**
- **ACTIVE LOW DATA ENABLE INPUTS**
- **ACTIVE LOW OUTPUT ENABLE INPUTS**
- **ASYNCHRONOUS MASTER RESET**

PIN NAMES

D_0-D_3	Data Inputs
$\overline{ED_0}$-$\overline{ED_1}$	Data Enable Inputs (Active LOW)
$\overline{EO_0}$, $\overline{ED_1}$	Output Enable Inputs (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
MR	Master Reset Input
Q_0-Q_3	Data Outputs

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{ED_0}$	$\overline{ED_1}$	D_n	Q_{n+1}
H	X	X	Q_n
X	H	X	Q_n
L	L	L	L
L	L	H	H

CONDITIONS:

MR = $\overline{EO_0}$ = $\overline{EO_1}$ = LOW

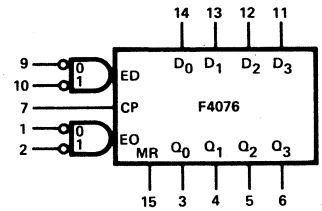
L = LOW Level

H = HIGH Level

X = Don't Care

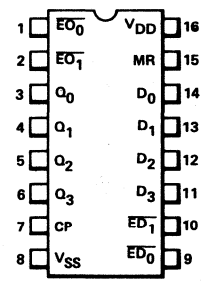
Q_{n+1} = State After Positive Clock Transition

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

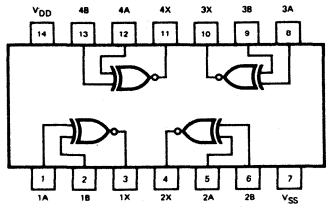


NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

QUAD EXCLUSIVE-NOR GATE

DESCRIPTION – The F4077 CMOS logic element provides the Exclusive-NOR function. The outputs are fully buffered for best performance. The F4077 may be used interchangeably for the 4811.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



$X = AB + \overline{A}\,\overline{B}$

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			5.0			10.0		2.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					70.0			140.0		28.0			MAX	
		XM			0.5			1.0		0.2		μA	MIN, 25°C	
					30.0			60.0		12.0			MAX	

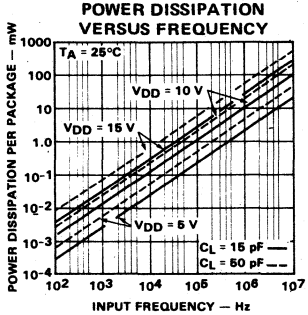
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		45	90		20	40		15		ns	
t_{PHL}	A or B to X		55	110		20	40		17		ns	C_L = 15 pF
t_{TLH}	Output Transition		23	45		10	25		7	20	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		23	45		10	25		7	20	ns	
t_{PLH}	Propagation Delay,		55	110		27	55		17		ns	
t_{PHL}	A or B to X		65	130		27	55		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		53	100		20	50		15	35	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		53	100		20	50		15	35	ns	

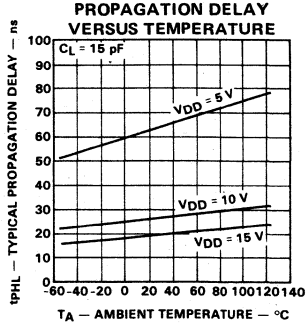
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

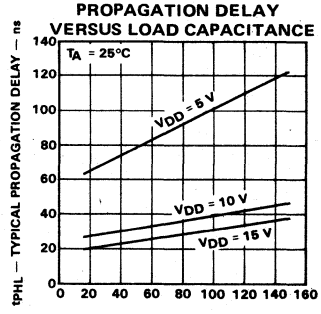
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



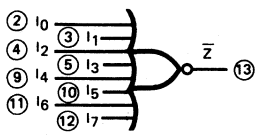
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



8-INPUT NOR GATE

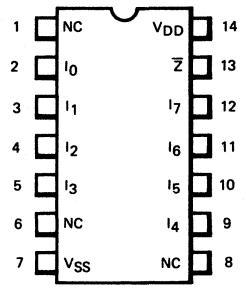
DESCRIPTION — This CMOS logic element provides the positive 8-Input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

F4078 LOGIC SYMBOL



V_{DD} = Pin 14
V_{SS} = Pin 7
NC = Pins 1, 6, 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

I_0-I_7	NOR Gate Inputs
$\overline{Z}$	Output (Active LOW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEMP	TEST CONDITIONS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		µA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

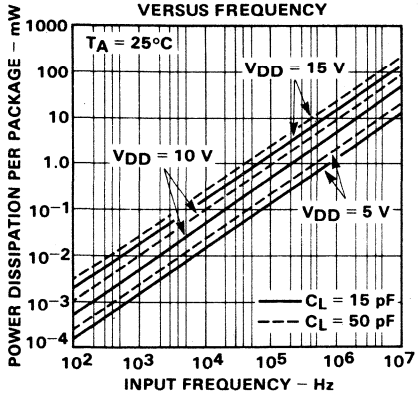
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V			LIMITS V_{DD} = 10 V			LIMITS V_{DD} = 15 V			UNITS	TEST CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		87	160		36	65		27		ns	
t_{PHL}			102	160		40	65		29		ns	C_L = 15 pF
t_{TLH}	Output Transition		35	75		20	40		16	25	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		37	75		17	40		15	25	ns	
t_{PLH}	Propagation Delay		108	200		46	85		34		ns	
t_{PHL}			129	200		50	85		35		ns	C_L = 50 pF
t_{TLH}	Output Transition		76	135		39	70		30	45	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		80	135		32	70		24	45	ns	

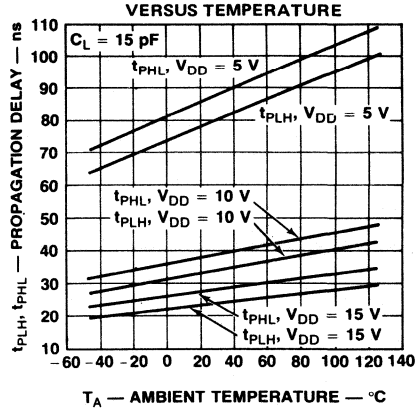
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

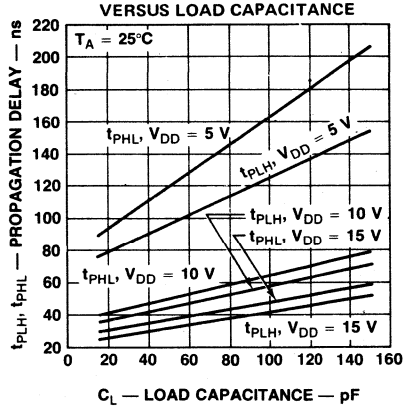
POWER DISSIPATION
VERSUS FREQUENCY



PROPAGATION DELAY
VERSUS TEMPERATURE



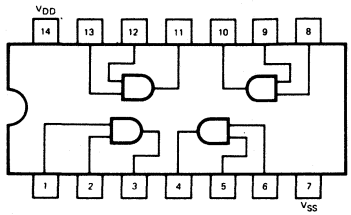
PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



QUAD 2-INPUT AND GATE

DESCRIPTION – The F4081 is a positive logic Quad 2-Input AND Gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		µA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

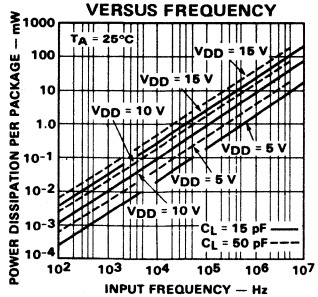
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		35	60		16	33		11		ns	
t_{PHL}			35	60		18	33		13		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		27	75		13	40		10	25	ns	Input Transition Times ≤ 20 ns
t_{THL}			25	75		10	40		7	25	ns	
t_{PLH}	Propagation Delay		55	95		23	50		17		ns	
t_{PHL}			60	95		25	50		19		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		70	135		30	70		23	45	ns	Input Transition Times ≤ 20 ns
t_{THL}			57	135		23	70		16	45	ns	

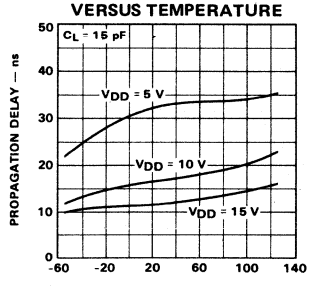
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

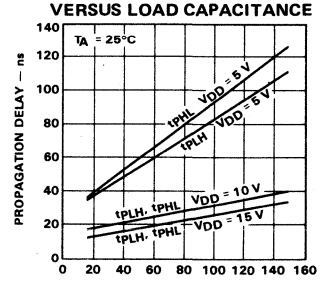
POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



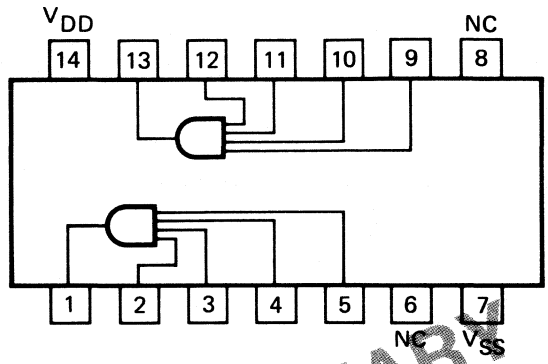
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



DUAL 4-INPUT AND GATE

DESCRIPTION – This CMOS logic element provides the positive Dual 4-Input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The 'Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			0.5			5		1		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15			30		6			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3			6		1.2			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		35			20			15		ns	
t_{PHL}			35			20			15		ns	C_L = 15 pF
t_{TLH}	Output Transition Time		20			10			8		ns	Input Transition Times ≤ 20 ns
t_{THL}			20			10			8		ns	
t_{PLH}	Propagation Delay		45			25			20		ns	
t_{PHL}			45			25			20		ns	C_L = 50 pF
t_{TLH}	Output Transition Time		45			20			15		ns	Input Transition Times ≤ 20 ns
t_{THL}			45			20			15		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and output transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.

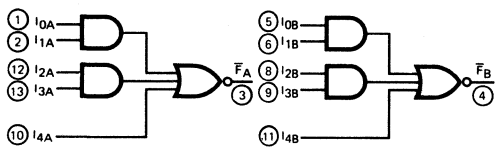
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION – The F4085 is a Dual 2-Wide 2-Input AND-OR-Invert (AOI) Gate, each with an additional input (I_{4A} or I_{4B}) which can be used as either an Expander Input or an Inhibit Input by connecting it to any standard CMOS output. A HIGH on this Input (I_4) forces the Output ($\overline{F}$) LOW independent of the other four inputs (I_0–I_3). The Outputs ($\overline{F_A}$ and $\overline{F_B}$) are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

I_{0A}–I_{4A}, I_{0B}–I_{4B}	Gate Inputs
$\overline{F}_A$, $\overline{F}_B$	Outputs (Active LOW)

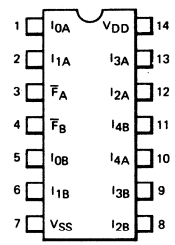
LOGIC DIAGRAM



$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		μA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

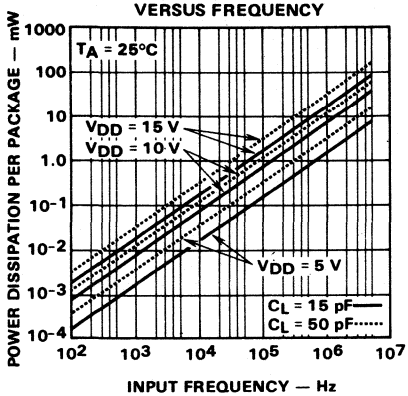
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		40	80		18	40		12		ns	
t_{PHL}	Any I to $\overline{F}$		54	100		28	50		15		ns	C_L = 15 pF
t_{TLH}	Output Transition		20	45		12	25		10	20	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		20	45		12	25		10	20	ns	
t_{PLH}	Propagation Delay,		56	115		25	55		17		ns	
t_{PHL}	Any I to $\overline{F}$		74	135		30	65		20		ns	C_L = 50 pF
t_{TLH}	Output Transition		45	100		22	50		15	35	ns	Input Transition Times ≤ 20 ns
t_{THL}	Time		45	100		22	50		15	35	ns	

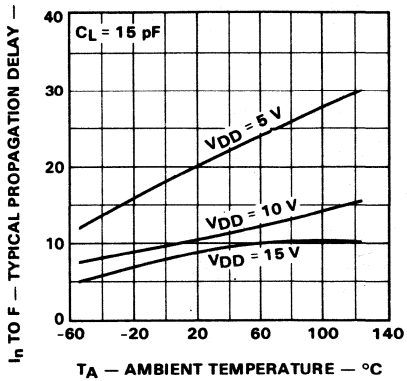
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

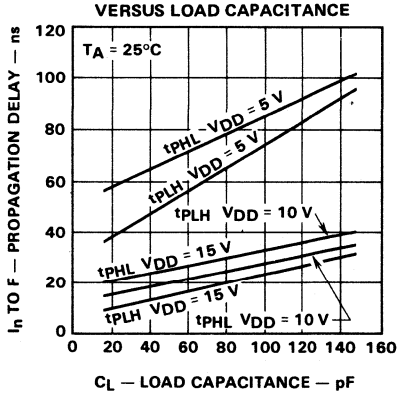
POWER DISSIPATION
VERSUS FREQUENCY



PROPAGATION DELAY
VERSUS TEMEPRATURE



PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



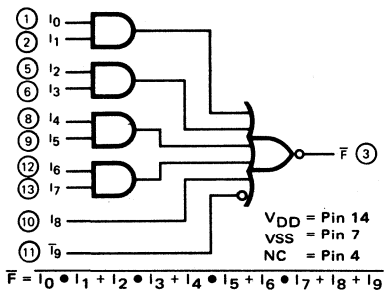
4-WIDE 2-INPUT AND-OR-INVERT GATE

DESCRIPTION – The F4086 is a 4-Wide 2-Input AND-OR-Invert (AOI) Gate with two additional inputs (I_8 and $\overline{I_9}$) which can be used as either expander inputs or inhibit inputs by connecting them to any standard CMOS output. A HIGH on I_8 or a LOW on $\overline{I_9}$ forces the Output ($\overline{F}$) LOW independent of the other eight inputs (I_0-I_7). The Output ($\overline{F}$) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.

PIN NAMES

I_0–I_8	Gate Inputs
$\overline{I_9}$	Gate Input (Active LOW)
$\overline{F}$	Output (Active LOW)

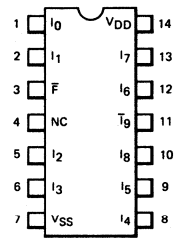
LOGIC DIAGRAM



$$\overline{F} = \overline{I_0 \bullet I_1 + I_2 \bullet I_3 + I_4 \bullet I_5 + I_6 \bullet I_7 + I_8 + I_9}$$

NOTE:
A HIGH on I_8 or a LOW on $\overline{I_9}$ forces the output ($\overline{F}$) LOW.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			0.5			5.0		1.0		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					15.0			30.0		6.0			MAX	
		XM			0.05			0.1		0.02		µA	MIN, 25°C	
					3.0			6.0		1.2			MAX	

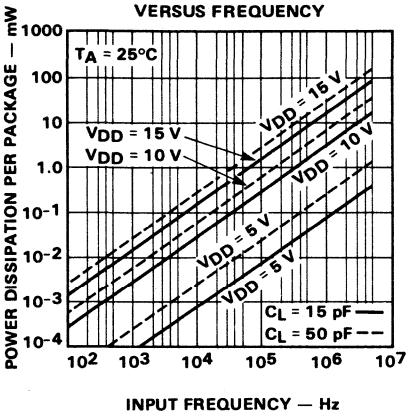
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, I_0 through I_8 to $\overline{F}$		80	150		35	70		20		ns	
t_{PHL}			80	150		35	70		20		ns	
t_{PLH}	Propagation Delay, $\overline{I_9}$ to $\overline{F}$		40	60		20	30		10		ns	C_L = 15 pF
t_{PHL}			40	60		20	30		10		ns	Input Transition Times ≤ 20 ns
t_{TLH}	Output Transition Time		25	45		12	25		8	20	ns	
t_{THL}			25	45		12	25		8	20	ns	
t_{PLH}	Propagation Delay, I_0 through I_8 to $\overline{F}$		100	180		40	80		25		ns	
t_{PHL}			100	180		40	80		25		ns	
t_{PLH}	Propagation Delay, $\overline{I_9}$ to $\overline{F}$		65	100		35	50		20		ns	C_L = 50 pF
t_{PHL}			65	100		35	50		20		ns	Input Transition Times ≤ 20 ns
t_{TLH}	Output Transition Time		55	100		25	50		18	35	ns	
t_{THL}			55	100		25	50		18	35	ns	

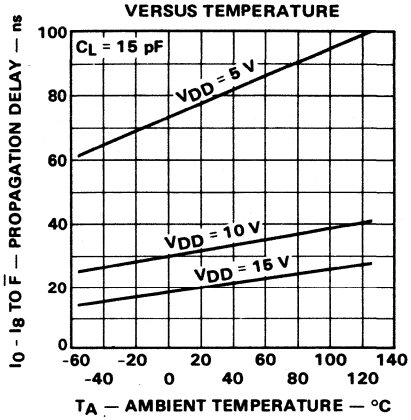
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

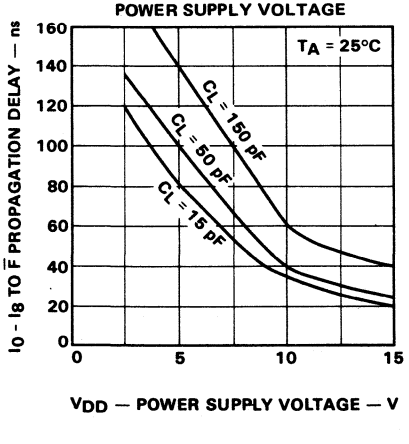
POWER DISSIPATION
VERSUS FREQUENCY



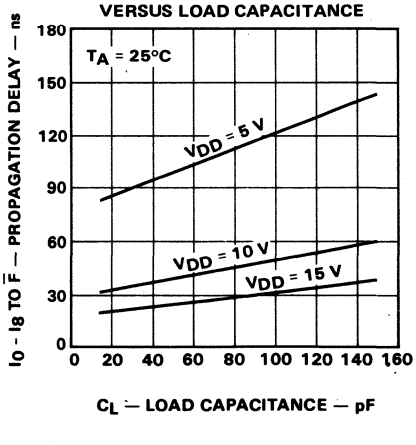
PROPAGATION DELAY
VERSUS TEMPERATURE



PROPAGATION DELAY
VERSUS
POWER SUPPLY VOLTAGE



PROPAGATION DELAY
VERSUS LOAD CAPACITANCE



F4104/34104

QUAD LOW VOLTAGE TO HIGH VOLTAGE TRANSLATER WITH 3-STATE OUTPUTS

DESCRIPTION – The F4104 Quad Low Voltage to High Voltage Translator with 3-State Outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage CMOS and TTL to high voltage CMOS. It has four Data Inputs (I_0-I_3), an active HIGH Output Enable input (EO), four Data Outputs (Z_0-Z_3) and their Complements ($\overline{Z}_0$-$\overline{Z}_3$). With the Output Enable input HIGH, the Outputs (Z_0-Z_3, $\overline{Z}_0$-$\overline{Z}_3$) are in the low impedance "ON" state, either HIGH or LOW as determined by the Data Inputs; with the Output Enable input LOW, the Outputs are in the high impedance "OFF" state.

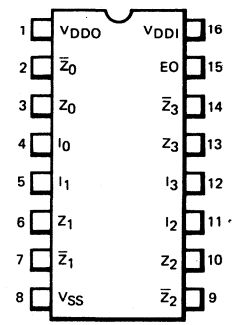
The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. For the allowable operating range of V_{DDI} and V_{DDO} see Figure 1. Each input protection circuit is terminated between V_{DDO} and V_{SS}. This allows the input signals to be driven from any potential between V_{DDO} and V_{SS}, without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10 mA.

When used in a bus organized system, all F4104 devices on the same bus line should be connected to the same V_{DDO} and V_{SS} supplies. Otherwise, parasitic diodes from the output to V_{DDO} and V_{SS} can become forward biased, even while the device is in the OFF state, causing catastrophic failure if the current is not limited to 10 mA.

- **3-STATE FULLY BUFFERED OUTPUTS**
- **OUTPUT ENABLE INPUT (ACTIVE HIGH)**
- **DUAL POWER SUPPLY**

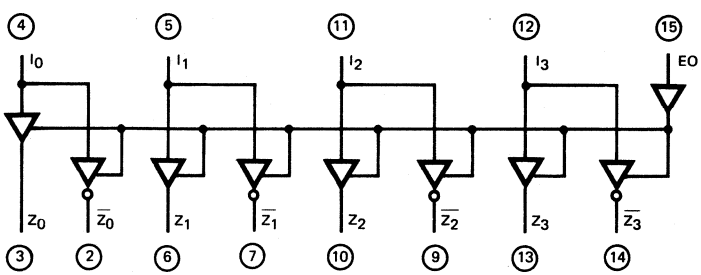
PIN NAMES	FUNCTION
I_0-I_3	Data Inputs
EO	Output Enable Input
Z_0-Z_3	Data Outputs
$\overline{Z}_0$-$\overline{Z}_3$	Complimentary Data Outputs

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC SYMBOL



V_{DDO} = Pin 1
V_{DDI} = Pin 16
V_{SS} = Pin 8
O = Pin Number

DC CHARACTERISTICS: $V_{DDO} = V_{DDI}$ as shown, $V_{SS} = 0$ V

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DDO/I}$ = 5 V			$V_{DDO/I}$ = 10 V			$V_{DDO/I}$ = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		3.5		Note 1	7.0		Note 1	10.5		Note 1	V	All	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage		Note 2		1.5	Note 2		3.0	Note 2		4.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		4.99 4.95			9.99 9.95			14.99 14.95			V	MIN, 25°C MAX	I_{OH} = 0 mA Note 3
			4.0			9.0			13.0				All	I_{OH} = 0 mA Note 4
V_{OL}	Output LOW Voltage				0.01 0.05			0.01 0.05			0.01 0.05	V	MIN, 25°C MAX	I_{OL} = mA Note 3
					0.5			1.0			2.0		All	I_{OL} = 0 mA Note 4
I_{IN}	Input Current	XC XM			0.1 0.01			0.1 0.01			1.0 1.0	µA	25°C	Lead Under Test at 0 V or V_{DDO}. All Other Inputs Simultaneously at 0 V or V_{DDO}
I_{OH}	Output HIGH Current		−1.5 −1.0									mA	MIN, 25°C MAX	V_{OUT} = 2.5 V for V_{DDO} = 5 V Note 3
			−0.7 −0.4			−1.4 −0.8			−2.2 −1.4				MIN, 25°C MAX	$V_{OUT} = V_{DDO}$ −0.5 V Note 3
I_{OL}	Output LOW Current		1.0 0.8 0.4			2.6 2.0 1.2			3.6 3.6 2.0			mA	MIN 25°C MAX	V_{OUT} = 0.4 V for V_{DDO} = 5 V V_{OUT} = 0.5 V for V_{DDO} = 10 V V_{OUT} = 0.5 V for V_{DDO} = 15 V Note 3
I_{OZH}	Output OFF Current HIGH	XC			0.5 30.0			1.0 60.0		0.2 12.0		µA	MIN, 25°C MAX	Output Returned to V_{DDO}, EO = V_{SS}
		XM			0.05 3.0			0.1 6.0		0.02 1.2			MIN, 25°C MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5 −30.0			−1.0 −60.0		−0.2 −12.0		µA	MIN, 25°C MAX	Output Returned V_{SS}, EO = V_{SS}
		XM			−0.05 −3.0			−0.1 −6.0		−0.02 −1.2			MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC			50 700			100 1400		20 280		µA	MIN, 25°C MAX	All Inputs Common and at 0 V or V_{DDI} = V_{DDO}
		XM			5 300			10 600		60 120		µA	MIN, 25°C MAX	

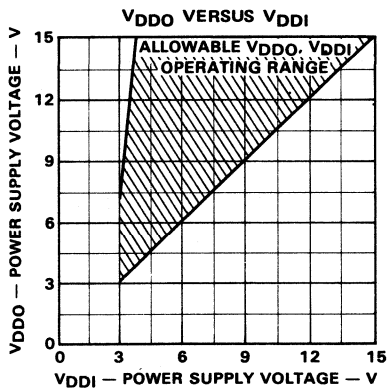
NOTES:
1. V_{IH} must be less than or equal to V_{DDO}. If V_{IH} is greater than V_{DDO}, current at each input must be limited to 10 mA.
2. V_{IL} must be greater than or equal to V_{SS}, if V_{IL} is less than V_{SS}, current at each input must be limited to 10 mA.
3. Inputs at 0 V or V_{DDO} per function.
4. Inputs at 0.3 V_{DDO} or 0.7 V_{DD} per function.
5. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DDI} = 5 V, V_{DDO} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 5)

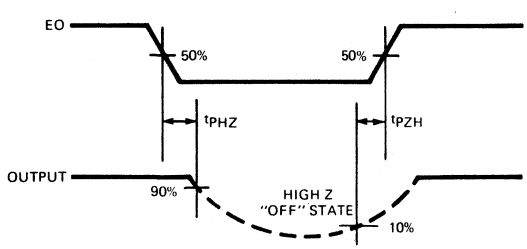
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DDO} = 5 V			V_{DDO} = 10 V			V_{DDO} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, I_n to Z_n or $\overline{Z_n}$		135 135			75 75			65 65		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PZH} t_{PZL}	Output Enable Time		190 185			95 90			75 75		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DDO}
t_{PHZ} t_{PLZ}	Output Disable Time		100 100			75 70			70 60		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DDO}
t_{TLH} t_{THL}	Output Transition Time		30 30			18 18			16 16		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, I_n to Z_n or $\overline{Z_n}$		160 160			85 85			75 75		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PZH} t_{PZL}	Output Enable Time		200 200			100 100			80 80		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DDO}
t_{PHZ} t_{PLZ}	Output Disable Time		115 110			80 80			75 70		ns ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DDO}
t_{TLH} t_{THL}	Output Transition Time		60 60			30 30			25 25		ns ns	

Notes on privious page.

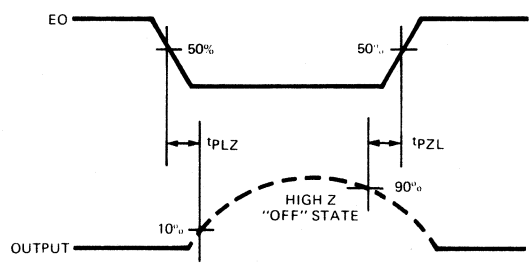
Fig. 1 TYPICAL ELECTRICAL CHARACTERISTICS



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

F4510/34510

UP/DOWN DECADE COUNTER

DESCRIPTION – The F4510 is an Edge-Triggered Synchronous Up/Down BCD Counter with a Clock Input ($\overline{CP}$), an active HIGH Up/Down Count Control Input (Up/$\overline{Dn}$), an active LOW Count Enable Input ($\overline{CE}$), an asynchronous active HIGH Parallel Load Input (PL), four Parallel Inputs (P_0-P_3), four Parallel Outputs (Q_0-Q_3), an active LOW Terminal Count Output ($\overline{TC}$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except the Master Reset Input (MR) which must be LOW. With the Parallel Load Input (PL) LOW, the counter changes on the LOW-to-HIGH transition of the Clock Input (CP) if the Count Enable Input ($\overline{CE}$) is LOW. The Up/Down Count Control Input (Up/$\overline{Dn}$) determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, the Terminal Count Output ($\overline{TC}$) is LOW when the Parallel Outputs Q_0-Q_3 are HIGH and the Count Enable ($\overline{CE}$) is LOW. When counting down, the Terminal Count Output ($\overline{TC}$) is LOW when all the Parallel Outputs (Q_0-Q_3) and the Count Enable Input ($\overline{CE}$) are LOW. A HIGH on the Master Reset Input resets the counter (Q_0-Q_3 = LOW) independent of all other input conditions.

- **UP/DOWN COUNT CONTROL**
- **SINGLE CLOCK INPUT (L→H EDGE-TRIGGERED)**
- **ASYNCHRONOUS PARALLEL LOAD INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **EASILY CASCADABLE**

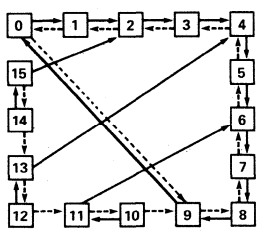
MODE SELECTION TABLE

PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	H	X	No Change
L	L	L	⎍	Count Down, Decade
L	H	L	⎍	Count Up, Decade

MR = LOW
H = HIGH Level
L = LOW Level

X = Don't Care
⎍ = Positive-Going Transition

F4510 STATE DIAGRAM

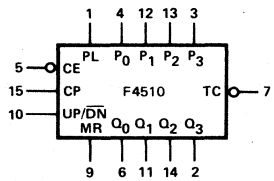


Count Up ——————
Count Down – – – – –

LOGIC EQUATION FOR TERMINAL COUNT

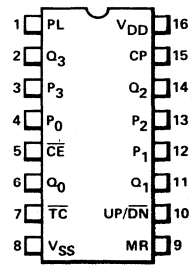
$TC = CE \bullet [(UP \bullet Q_0 \bullet Q_3) + (\overline{UP} \bullet \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3)]$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

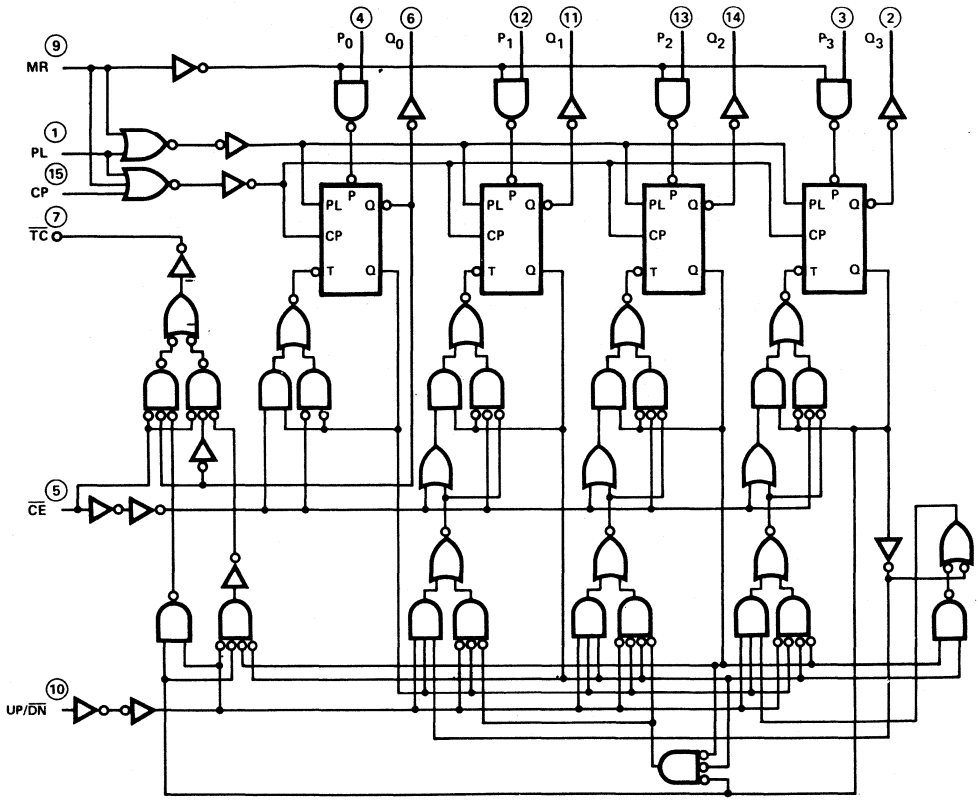


NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

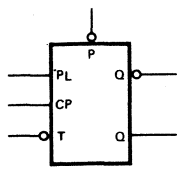
PIN NAMES

PL	Parallel Load Input (Active HIGH)
P_0-P_3	Parallel Inputs
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (L → H Edge-Triggered)
Up/$\overline{Dn}$	Up/Down Count Control Input
MR	Master Reset Input
$\overline{TC}$	Terminal Count Output (Active LOW)
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number



PL (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when PL is HIGH Overriding all Other Inputs
CP (Clock Pulse Input)
Q, Q̄ (True and Complimentary Outputs)
T (Toggle Input) — Forces the Q output to synchronously toggle when a HIGH is placed on this input.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

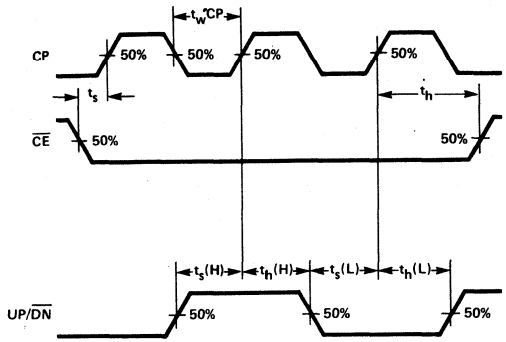
Notes on folowing page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

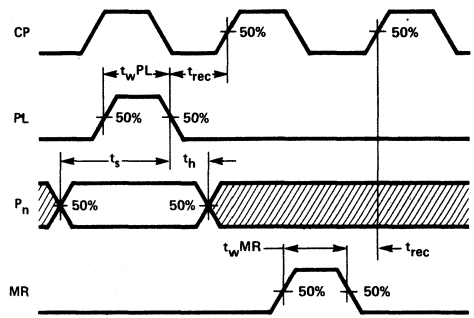
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		135			54			35		ns	C_L = 15 pF, Input Transition Times ≤ 20 ns
t_{PHL}			135			50			33			
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		150			62			42		ns	
t_{PHL}			228			90			60			
t_{PLH}	Propagation Delay, PL to Q_n		152			59			38		ns	
t_{PHL}			194			80			56			
t_{PLH}	Propagation Delay, MR to Q_n, $\overline{TC}$		350			150			100		ns	
t_{PHL}			250			110			75			
t_{TLH}	Output Transition Time		25			13			10		ns	
t_{THL}			25			13			10			
t_{PLH}	Propagation Delay, CP to Q_n		150			62			41		ns	C_L = 50 pF, Input Transition Times ≤ 20 ns
t_{PHL}			150			59			39			
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		167			71			48		ns	
t_{PHL}			252			100			66			
t_{PLH}	Propagation Delay, PL to Q_n		170			70			45		ns	
t_{PHL}			220			90			62			
t_{PLH}	Propagation Delay, MR to Q_n, $\overline{TC}$		370			170			105		ns	
t_{PHL}			270			120			80			
t_{TLH}	Output Transition Time		60			31			23		ns	
t_{THL}			65			25			18			
t_wCP	CP Minimum Pulse Width		50			21			14		ns	C_L = 15 pF, Input Transition Times ≤ 20 ns
t_wPL	PL Minimum Pulse Width		60			21			16		ns	
t_wMR	MR Minimum Pulse Width		60			30			20		ns	
t_{rec}	MR Recovery Time		75			30			20		ns	
t_{rec}	PL Recovery Time		62			24			17		ns	
t_s	Set-Up Time, UP/$\overline{DN}$ to CP		145			55			38		ns	
t_h	Hold Time, UP/$\overline{DN}$ to CP		101			38			25			
t_s	Set-Up Time, $\overline{CE}$ to CP		118			49			33		ns	
t_h	Hold Time, $\overline{CE}$ to CP		101			38			25			
t_s	Set-Up Time, P_n to PL		29			11			8		ns	
t_h	Hold Time, P_n to PL		26			7			4			
f_{MAX}	Input Clock Frequency (Note 4)		5			12					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input (CP) be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP AND UP/$\overline{DN}$ TO CP



MINIMUM PL AND MR PULSE WIDTH, RECOVERY TIME FOR PL AND MR, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4511/34511

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

DESCRIPTION – The F4511 is a BCD-to-7-Segment Latch/Decoder/Driver with four Address Inputs (A_0-A_3), an active LOW Latch Enable Input ($\overline{EL}$), an active Low Blanking Input ($\overline{I_B}$), an active LOW Lamp Test Input ($\overline{I_{LT}}$) and seven active HIGH NPN bipolar segment outputs (a-g).

When the Latch Enable Input ($\overline{EL}$) is LOW, the state of the Segment Outputs (a-g) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input ($\overline{EL}$) goes HIGH, the last data present at the Address Inputs (A_0-A_3) is stored in the latches and the Segment Outputs (a-g) remain stable.

When the Lamp Test Input ($\overline{I_{LT}}$) is LOW, all the Segment Outputs (a-g) are HIGH independent of all other input conditions. With the Lamp Test Input ($\overline{I_{LT}}$) HIGH, a LOW on the Blanking Input ($\overline{I_B}$) forces all Outputs (a-g) LOW. The Lamp Test Input ($\overline{I_{LT}}$) and the Blanking Input ($\overline{I_B}$) do not affect the latch circuit.

- **HIGH CURRENT SOURCING OUTPUTS (UP TO 25 mA)**
- **BLANKING INPUT (ACTIVE LOW)**
- **LAMP TEST INPUT (ACTIVE LOW)**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **MULTIPLEXING CAPABILITY**

PIN NAMES

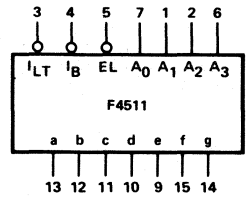
A_0–A_3	Address (Data) Inputs
$\overline{EL}$	Latch Enable Input (Active LOW)
$\overline{I_B}$	Blanking Input (Active LOW)
$\overline{I_{LT}}$	Lamp Test Input (Active LOW)
a–g	Segment Outputs

TRUTH TABLE

INPUTS							OUTPUTS							
$\overline{EL}$	$\overline{I_B}$	$\overline{I_{LT}}$	A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	L	H	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	L	H	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	L	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	H	H	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X				*				*

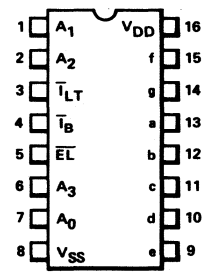
H = HIGH Level
L = LOW Level
X = Don't Care
* = Depends upon the BCD code applied during the LOW-to-HIGH transition of $\overline{EL}$.

LOGIC SYMBOL



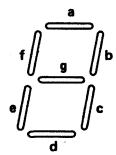
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

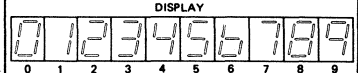


NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

NUMERICAL DESIGNATIONS



DISPLAY



F4512/34512
8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

DESCRIPTION – The F4512 is an 8-Input Multiplexer with Active LOW logic and output enables ($\overline{E}$, $\overline{EO}$). One of eight binary inputs is selected by Select Inputs S_0, S_1 and S_2 and is routed to the output F. A HIGH on the Output Enable ($\overline{EO}$) causes the F output to assume a high impedance or "OFF" state, regardless of other input conditions. This allows the output to interface directly with bus oriented systems (3-state). When the active LOW Enable ($\overline{E}$) is HIGH, it forces the output LOW provided the Output Enable ($\overline{EO}$) is LOW. By proper manipulation of the inputs, the F4512 can provide any logic functions of four variables. The F4512 cannot be used to multiplex analog signals.

- **SELECTS ONE-OF-EIGHT DATA SOURCES**
- **PERFORMS PARALLEL-TO-SERIAL CONVERSION**
- **3-STATE OUTPUTS WITH ACTIVE LOW OUTPUT ENABLE**
- **ACTIVE LOW LOGIC ENABLE**

PIN NAMES

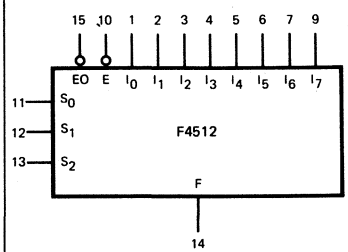
S_0, S_1, S_2	Select Inputs
$\overline{EO}$	Output Enable (Active LOW)
$\overline{E}$	Enable (Active LOW)
I_0 to I_7	Multiplexer Inputs
F	Multiplexer Output

TRUTH TABLE

INPUTS													OUTPUT
$\overline{EO}$	$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	F
L	H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	L	H	H	X	X	X	H	X	X	X	X	H
L	L	H	L	L	X	X	X	X	L	X	X	X	L
L	L	H	L	L	X	X	X	X	H	X	X	X	H
L	L	H	L	H	X	X	X	X	X	L	X	X	L
L	L	H	L	H	X	X	X	X	X	H	X	X	H
L	L	H	H	L	X	X	X	X	X	X	L	X	L
L	L	H	H	L	X	X	X	X	X	X	H	X	H
L	L	H	H	H	X	X	X	X	X	X	X	L	L
L	L	H	H	H	X	X	X	X	X	X	X	H	H
H	X	X	X	X	X	X	X	X	X	X	X	X	Z

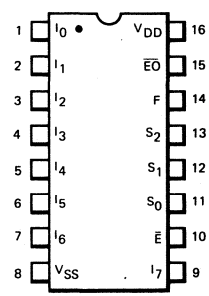
L = LOW Level
H = HIGH Level
X = Don't Care
Z = High Impedance State

LOGIC SYMBOL



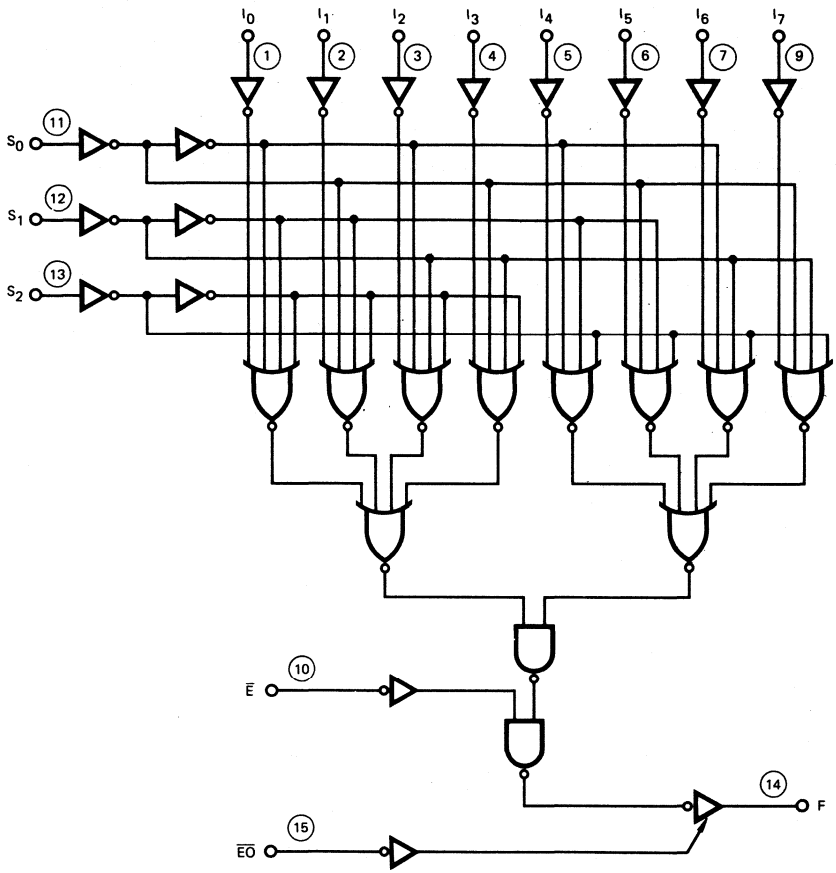
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDTIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5 30.0			1.0 60.0		0.2 12.0		μA	MIN, 25°C MAX	Output returned to V_{DD}, $\overline{EO}$ = V_{DD}
		XM			0.05 3.0			0.1 6.0		0.02 1.2			MIN, 25°C MAX	
I_{OZL}	Output OFF Current LOW	XC			− 0.5 −30.0			− 1.0 −60.0		− 0.2 −12.0		μA	MIN, 25°C MAX	Output returned to V_{SS}, $\overline{EO}$ = V_{DD}
		XM			− 0.05 − 3.0			− 0.1 − 6.0		− 0.02 − 1.2			MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC			30 600			60 1200		12 240		μA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM			5 100			10 200		2 40		μA	MIN, 25°C MAX	

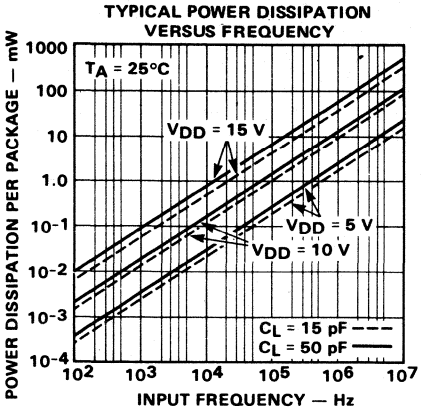
AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

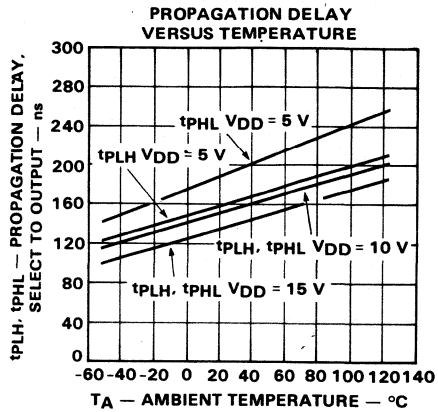
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		130 130	260 260		65 65	130 130		45 45		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		150 150	300 300		75 75	150 150		55 55		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, E to Output		70 70	140 140		35 35	70 70		25 25		ns ns	
t_{PZH} t_{PZL}	Output Enable Time		26 28	70 70		11 11	35 35		10 10		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		34 39	90 90		20 20	45 45		15 15		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		45 45	100 100		20 20	60 60		15 15	40 40	ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		150 150	300 300		75 75	150 150		52 52		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, Select to Output		175 175	350 350		85 85	170 170		60 65		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, E to Output		90 90	175 175		45 45	90 90		30 32		ns ns	
t_{PZH} t_{PZL}	Output Enable Time		33 30	85 85		20 22	45 45		18 20		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		39 40	100 100		20 20	50 50		15 15		ns ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time		90 100	200 200		40 40	100 100		33 30	65 65	ns ns	

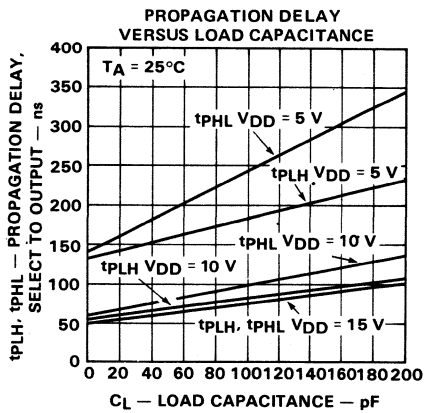
NOTES:

1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

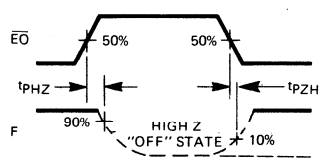
TYPICAL ELECTRICAL CHARACTERISTICS



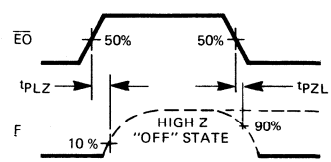




SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

APPLICATIONS

MULTIPLEXER AS A FUNCTION GENERATOR – In most digital systems there are areas, usually in the control section, where a number of inputs generate an output in a highly irregular way. In other words, an unusual function must be generated which is apparently not available as an MSI building block. In such cases, many designers tend to return to classical methods of logic design with NAND and NOR gates using Boolean Algebra, Karnaugh maps and Veitch diagrams for logic minimization. Surprisingly enough, multiplexers can simplify these designs.

The F4512 8-Input multiplexer can generate any one of the 65,536 different functions of four variables. An example will illustrate the technique. Assume four binary inputs are A, B, C and D and F is the desired function (See Fig. 1). If C is connected to S_0, B to S_1 and A to S_2, any combination of A, B and C will select an input (assuming the output is enabled). For each combination of A, B and C, the required output, as a function of the fourth variable D, is either H or L the same as D or the opposite of D. Therefore, the truth table may be examined and each input of the F4512 is connected to V_{DD}, V_{SS}, D or $\overline{D}$ as required and in such fashion the function is generated.

In the example shown, (Fig. 1) the first two outputs are the opposite of D, so I_0 is connected to D. The second two are HIGH, so I_1 is connected to V_{DD}, etc.

32-INPUT MULTIPLEXER – The 3-State Output Enable can be used to expand the F4512. A 32-Input Multiplexer utilizing four F4512s and a F4011 is shown in Fig. 2.

INPUT VARIABLES				REQUIRED FUNCTION
A	B	C	D	F
L	L	L	L	H
L	L	L	H	L
L	L	H	L	H
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
·	·	·	·	·
·	·	·	·	·
		·	·	·

H = HIGH Level
L = LOW Level

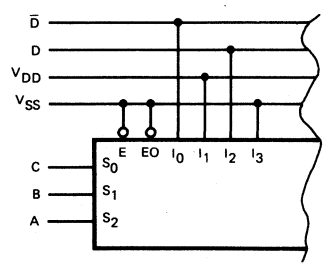


Fig. 1

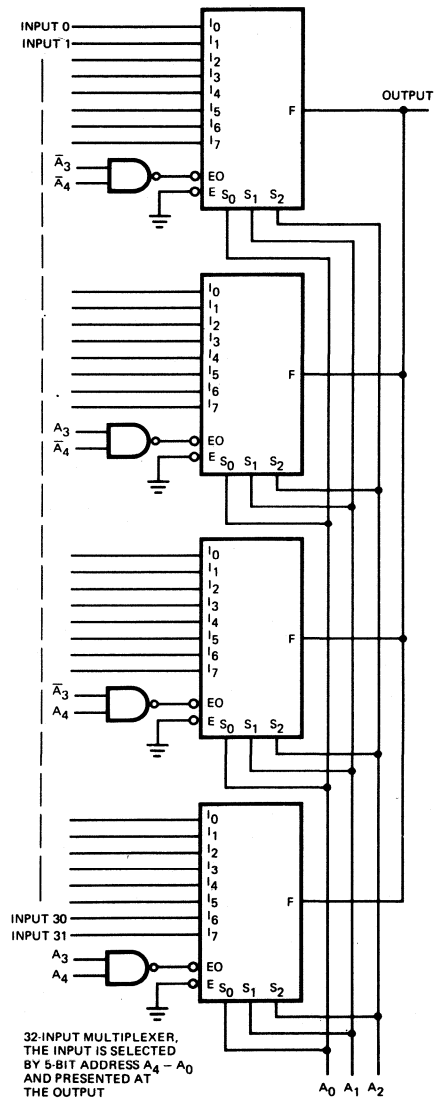


Fig. 2

F4514/34514

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCH

DESCRIPTION — The F4514 is a 1-of-16 Decoder/Demultiplexer with four binary weighted Address Inputs (A_0-A_3), a Latch Enable Input (EL), an active LOW Enable Input ($\overline{E}$) and sixteen mutually exclusive active HIGH Outputs (O_0-O_{15}).

When the Latch Enable Input (EL) is HIGH, the selected Output (O_0-O_{15}) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input (EL) goes LOW, the last data present at the Address inputs (A_0-A_3) is stored in the latches and the Outputs (O_0-O_{15}) remain stable. When the Enable Input ($\overline{E}$) is LOW, the selected Output (O_0-O_{15}), determined by the contents of the latch, is HIGH. When the Enable Input ($\overline{E}$) is HIGH, all Outputs (O_0-O_{15}) are LOW. The Enable Input ($\overline{E}$) does not affect the state of the latch.

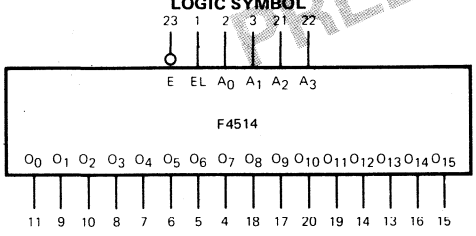
With the Latch Enable Input (EL) HIGH, 16-channel demultiplexing results when data is applied to the Enable Input ($\overline{E}$) and the desired output is selected by A_0-A_3. The selected output (O_0-O_{15}) will follow as the inverse of the data. All unselected outputs (O_0-O_{15}) are LOW.

- **LATCH ENABLE INPUT (ACTIVE HIGH)**
- **ENABLE INPUT (ACTIVE LOW)**
- **SELECTED BUFFERED OUTPUTS (ACTIVE HIGH) COMPLEMENT OF THE INPUT**

PIN NAMES

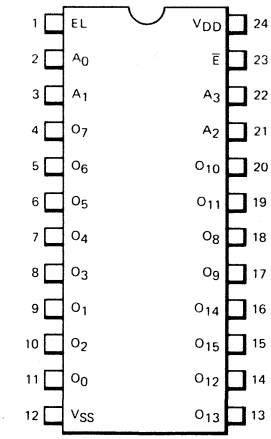
A_0-A_3	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
EL	Latch Enable Input
O_0-O_{15}	Outputs

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



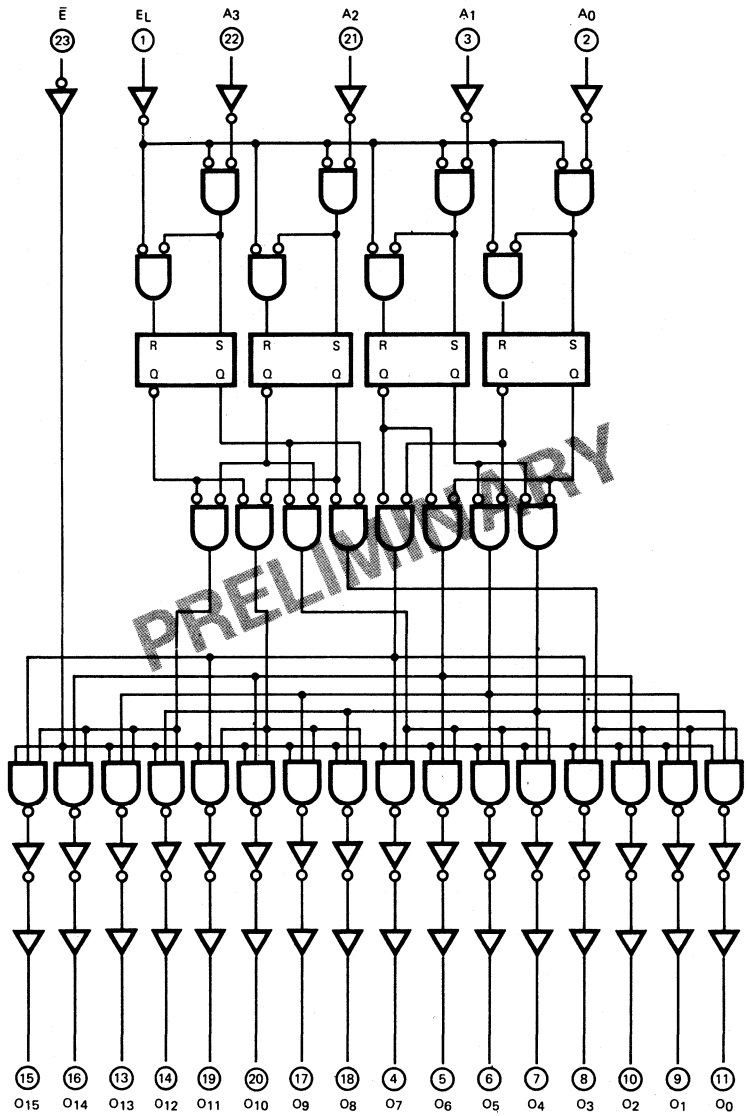
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

INPUTS					OUTPUTS														
$\overline{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

H = HIGH Level
L = LOW Level
EL = HIGH

LOGIC DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

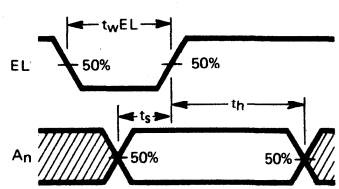
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A_n to O_n		400			150			110		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			400			150			110		ns	
t_{PLH}	Propagation Delay, EL to O_n		400			150			110		ns	
t_{PHL}			400			150			110		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to O_n		175			75			60		ns	
t_{PHL}			175			75			60		ns	
t_{TLH}	Output Transition Time		35			20			10		ns	
t_{THL}			35			20			10		ns	
t_{PLH}	Propagation Delay, A_n to O_n		450			165			120		ns	
t_{PHL}			450			165			120		ns	
t_{PLH}	Propagation Delay, EL to O_n		450			165			120		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			450			165			120		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to O_n		190			80			65		ns	
t_{PHL}			190			80			65		ns	
t_{TLH}	Output Transition Time		65			35			15		ns	
t_{THL}			65			35			15		ns	
t_s	Set-Up Time, A_n to EL		75			30			25		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_h	Hold Time, A_n to EL		35			20			15		ns	
t_wEL	Minimum EL Pulse Width		100			30			25		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

SWITCHING WAVEFORMS



MINIMUM EL PULSE WIDTH AND SET-UP AND HOLD TIMES, A_n TO EL

NOTE:
Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

F4515/34515

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCH

DESCRIPTION – The F4515 is a 1-of-16 Decoder/Demultiplexer with four binary weighted Address Inputs (A_0-A_3), a Latch Enable Input (EL), an active LOW Enable Input ($\overline{E}$) and sixteen mutually exclusive active LOW Outputs ($\overline{O_0}$-$\overline{O_{15}}$).

When the Latch Enable Input (EL) is HIGH, the selected Output ($\overline{O_0}$-$\overline{O_{15}}$) is determined by the data on the Address Inputs (A_0-A_3). When the Latch Enable Input (EL) goes LOW, the last data present at the Address Inputs (A_0-A_3) is stored in the latches and the Outputs ($\overline{O_0}$-$\overline{O_{15}}$) remain stable. When the Enable Input ($\overline{E}$) is LOW, the selected Output ($\overline{O_0}$-$\overline{O_{15}}$), determined by the contents of the latch, is LOW. When the Enable Input ($\overline{E}$) is HIGH, all Outputs ($\overline{O_0}$-$\overline{O_{15}}$) are HIGH. The Enable Input ($\overline{E}$) does not affect the state of the latch.

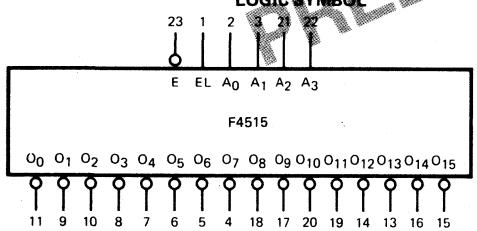
With the Latch Enable Input (EL) HIGH, 16-channel demultiplexing results when data is applied to the Enable Input ($\overline{E}$) and the desired output is selected by A_0-A_3. The selected Output ($\overline{O_0}$-$\overline{O_{15}}$) will follow the data at the Enable Input ($\overline{E}$). All unselected outputs ($\overline{O_0}$-$\overline{O_{15}}$) are HIGH.

- **LATCH ENABLE INPUT (ACTIVE HIGH)**
- **ENABLE INPUT (ACTIVE LOW)**
- **BUFFERED OUTPUTS (ACTIVE LOW)**

PIN NAMES

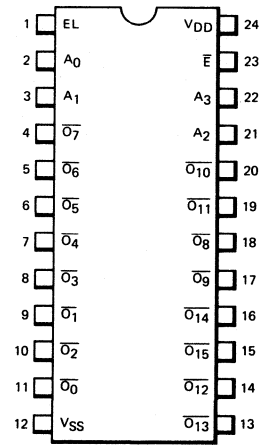
A_0-A_3	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
EL	Latch Enable Input
$\overline{O_0}$-$\overline{O_{15}}$	Outputs (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



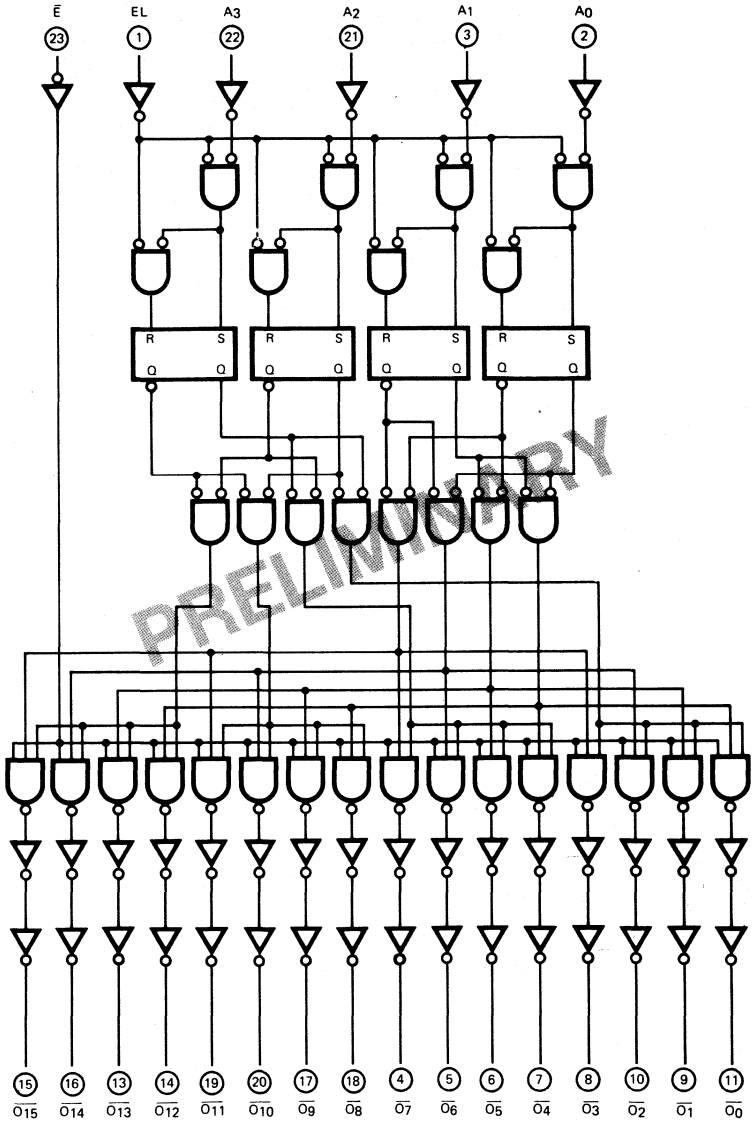
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

INPUTS					OUTPUTS													
$\overline{E}$	A_0	A_1	A_2	A_3	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$	$\overline{O_5}$	$\overline{O_6}$	$\overline{O_7}$	$\overline{O_8}$	$\overline{O_9}$	$\overline{O_{10}}$	$\overline{O_{11}}$	$\overline{O_{12}}$	$\overline{O_{13}}$	$\overline{O_{14}}$	$\overline{O_{15}}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
EL = HIGH

LOGIC DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

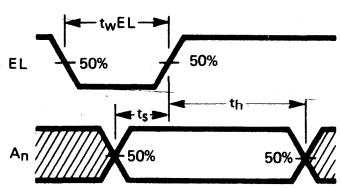
SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			50 700			100 1400		20 280		μA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM			5 300			10 600		2 120		μA	MIN, 25°C MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, A_n to $\overline{O_n}$		400 400			150 150			110 110		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, EL to $\overline{O_n}$		400 400			150 150			110 110		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to $\overline{O_n}$		175 175			75 75			60 60		ns ns	
t_{TLH} t_{THL}	Output Transition Time		35 35			20 20			10 10		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, A_n to $\overline{O_n}$		450 450			165 165			120 120		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, EL to $\overline{O_n}$		450 450			165 165			120 120		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to $\overline{O_n}$		190 190			80 80			65 65		ns ns	
t_{TLH} t_{THL}	Output Transition Time		65 65			35 35			15 15		ns ns	
t_s t_h	Set-Up Time, A_n to EL Hold Time, A_n to EL		75 35			30 20			25 15		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_wEL	Minimum EL Pulse Width		100			30			25		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
3. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

SWITCHING WAVEFORMS



MINIMUM EL PULSE WIDTH AND SET-UP AND HOLD TIMES, A_n TO EL

NOTE:
Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

F4516/34516

UP/DOWN COUNTER

DESCRIPTION — The F4516 is an edge-triggered synchronous Up/Down 4-Bit Binary Counter with a Clock Input (CP), an active HIGH Count Up/Down Control Input (Up/$\overline{Dn}$), an active LOW count Enable Input ($\overline{CE}$), an asynchronous active HIGH Parallel Load Input (PL), four Parallel Inputs (P_0-P_3), four parallel Outputs (Q_0-Q_3), an active LOW Terminal Count Output ($\overline{TC}$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except the Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the Count Enable Input ($\overline{CE}$) are LOW, the counter changes on the LOW-to-HIGH transition of the Clock Input (CP). The Count Up/Down Control Input (Up/$\overline{Dn}$) determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, the Terminal Count Output ($\overline{TC}$) is LOW when $Q_0 = Q_1 = Q_2 = Q_3$ = HIGH and $\overline{CE}$ = LOW. When counting down the Terminal Count Output ($\overline{TC}$) is LOW when $Q_0 = Q_1 = Q_2 = Q_3$ = LOW and the $\overline{CE}$ = LOW. A HIGH on the Master Reset Input (MR) resets the counter ($Q_0 = Q_1 = Q_2 = Q_3$ = LOW) independent of all other input conditions.

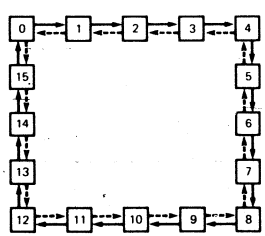
- **UP/DOWN COUNT CONTROL**
- **SINGLE CLOCK INPUT (L→H EDGE-TRIGGERED)**
- **ASYNCHRONOUS PARALLEL LOAD INPUT**
- **ASYNCHRONOUS MASTER RESET**

MODE SELECTION TABLE

PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	H	X	No Change
L	L	L	↓	Count Down, Binary
L	H	L	↑	Count Up, Binary

MR = LOW
H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Positive-Going Transition

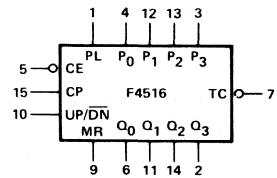
STATE DIAGRAM



LOGIC EQUATION FOR TERMINAL COUNT

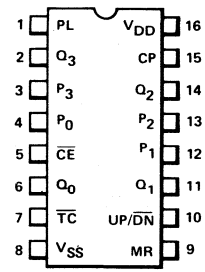
$$\overline{TC} = \overline{CE} \bullet [(UP/\overline{DN}) \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3] + [(UP/\overline{DN}) \bullet \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3]$$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

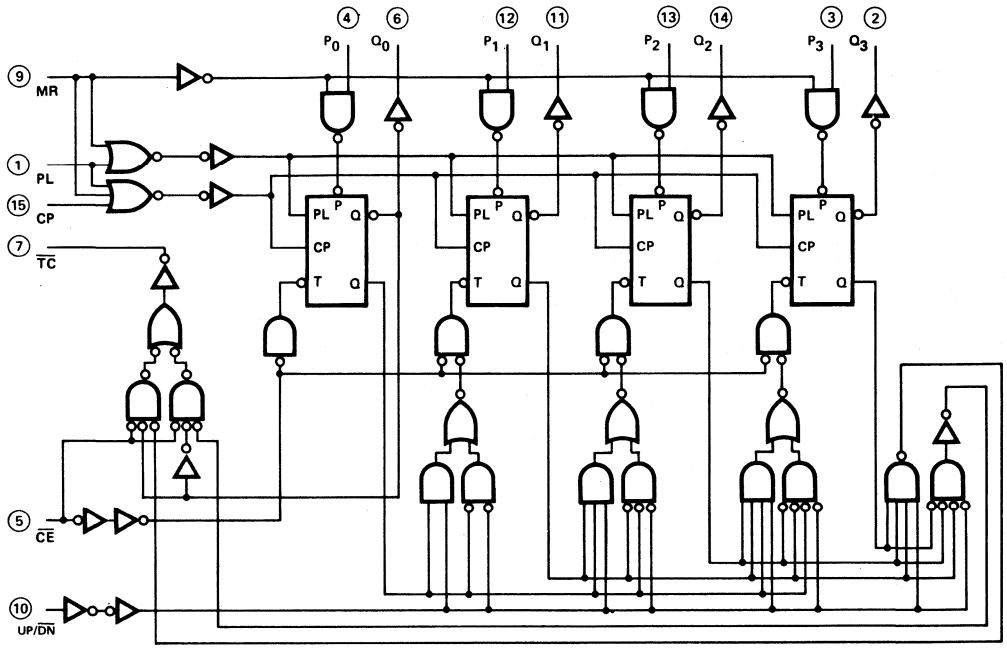


NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package,

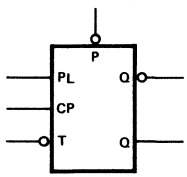
PIN NAMES

PL	Parallel Load Input (Active HIGH)
P_0-P_3	Parallel Inputs
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (L→H Edge-Triggered)
Up/$\overline{Dn}$	Up/Down Count Control Input
MR	Master Reset Input
$\overline{TC}$	Terminal Count Output (Active LOW)
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number



PL (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
$\overline{P}$ (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when PL is HIGH Overriding all Other Inputs
$\overline{T}$ (Toggle Input) — Forces the Q Output to Synchronously Toggle when a HIGH is placed on this Input
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complementary Outputs)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

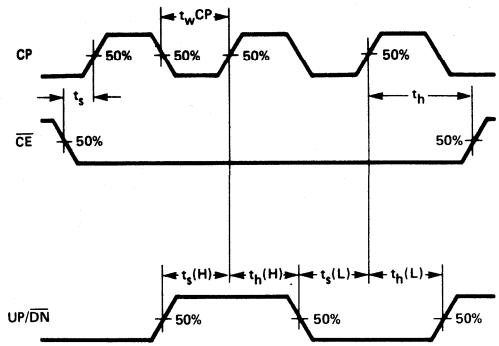
Notes on following page

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

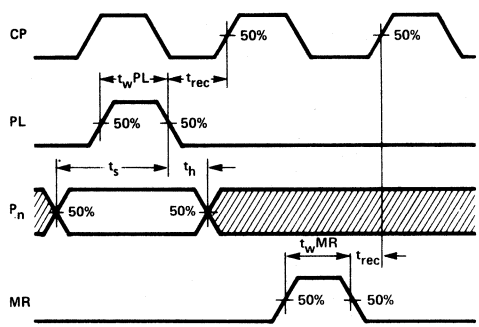
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		135			54			35		ns	C_L = 15 pF, Input Transition Times ≤ 20 ns
t_{PHL}			135			50			33			
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		150			62			42		ns	
t_{PHL}			228			90			60			
t_{PLH}	Propagation Delay, PL to Q_n		152			59			38		ns	
t_{PHL}			194			80			56			
t_{PLH}	Propagation Delay, MR to Q_n, $\overline{TC}$		350			150			100		ns	
t_{PHL}			250			110			75			
t_{TLH}	Output Transition Time		25			13			10		ns	
t_{THL}			25			13			10			
t_{PLH}	Propagation Delay, CP to Q_n		150			62			41		ns	C_L = 50 pF, Input Transition Times ≤ 20 ns
t_{PHL}			150			59			39			
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		167			71			48		ns	
t_{PHL}			252			100			66			
t_{PLH}	Propagation Delay, PL to Q_n		170			70			45		ns	
t_{PHL}			220			90			62			
t_{PLH}	Propagation Delay, MR to Q_n, $\overline{TC}$		370			170			105		ns	
t_{PHL}			270			120			80			
t_{TLH}	Output Transition Time		60			31			23		ns	
t_{THL}			65			25			18			
t_wCP	CP Minimum Pulse Width		50			21			14		ns	C_L = 15 pF, Input Transition Times ≤ 20 ns
t_wPL	PL Minimum Pulse Width		60			21			16		ns	
t_wMR	MR Minimum Pulse Width		60			30			20		ns	
t_{rec}	MR Recovery Time		75			30			20		ns	
t_{rec}	PL Recovery Time		62			24			17		ns	
t_s	Set-Up Time, UP/$\overline{DN}$ to CP		145			55			38		ns	
t_h	Hold Time, UP/$\overline{DN}$ to CP		101			38			25			
t_s	Set-Up Time, $\overline{CE}$ to CP		118			49			33		ns	
t_h	Hold Time, $\overline{CE}$ to CP		101			38			25			
t_s	Set-Up Time, P_n to PL		29			11			8		ns	
t_h	Hold Time, P_n to PL		26			7			4			
f_{MAX}	Input Clock Frequency (Note 4)		5			12					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input (CP) be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP AND UP/$\overline{DN}$ TO CP



MINIMUM PL AND MR PULSE WIDTH, RECOVERY TIME FOR PL AND MR, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4518/34518

DUAL 4-BIT DECADE COUNTER

DESCRIPTION – The F4518 is a Dual 4-Bit Internally Synchronous BCD Counter. Each counter has both an active HIGH Clock Input (CP_0) and an active LOW Clock Input ($\overline{CP}_1$), buffered Outputs from all four bit positions (Q_0-Q_3) and an active HIGH overriding asynchronous Master Reset Input (MR).

The counter advances on either the LOW-to-HIGH transition of the CP_0 Input if $\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of the $\overline{CP}_1$ Input if CP_0 is LOW (see the Truth Table). Either Clock Input (CP_0, $\overline{CP}_1$) may be used as the Clock Input to the counter and the other Clock Input may be used as a Clock Inhibit Input.

A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP}_1$).

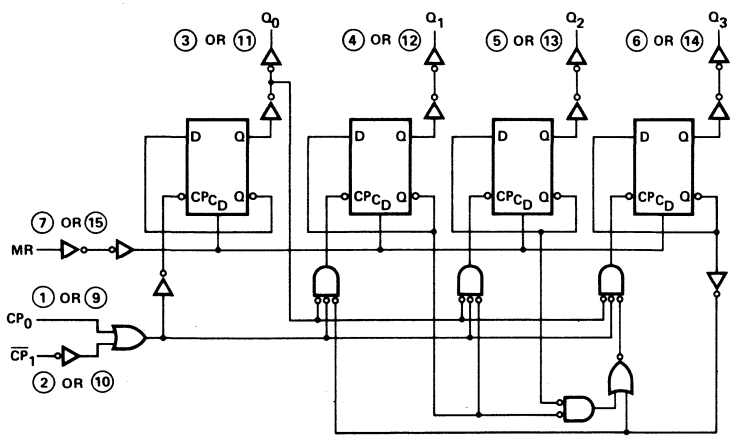
- **TYPICAL COUNT FREQUENCY OF 10 MHz AT V_{DD} = 10 V**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **BUFFERED OUTPUTS FROM ALL FOUR BIT POSITIONS**
- **FULLY SYNCHRONOUS COUNTING**

TRUTH TABLE

CP_0	$\overline{CP}_1$	MR	MODE
⌐	H	L	Counter Advances
L	⌐	L	Counter Advances
¬	X	L	No Change
X	⌐	L	No Change
⌐	L	L	No Change
H	¬	L	No Change
X	X	H	Reset (Asynchronous)

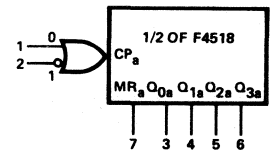
X = Don't Care
L = LOW Level
H = HIGH Level
⌐ = Positive-Going Transition
¬ = Negative-Going Transition

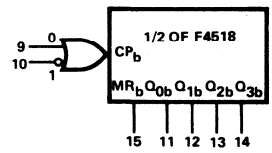
1/2 OF A F4518 LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

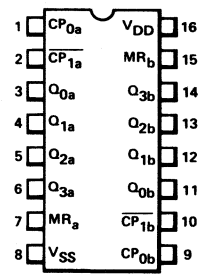
LOGIC SYMBOLS





V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP_{0a}, CP_{0b}	Clock Input (L → H Triggered)
$\overline{CP}_{1a}$, $\overline{CP}_{1b}$	Clock Input (H → L Triggered)
MR_a, MR_b	Master Reset Inputs
Q_{0a}–Q_{3a}	Outputs
Q_{0b}–Q_{3b}	Outputs

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

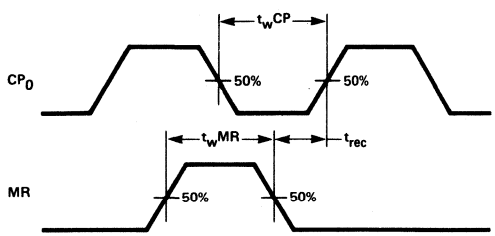
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		300			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

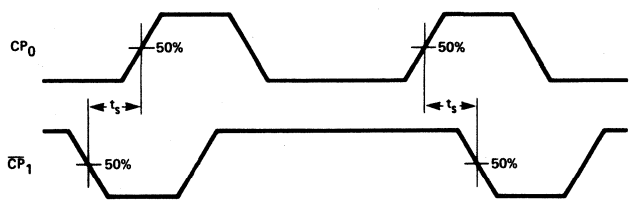
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$		200			85			55		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}	to Q_n		200			85			55			
t_{PHL}	Propagation Delay, MR to Q_n		200			80			55		ns	
t_{TLH}	Output Transition Time		35			18			12		ns	
t_{THL}			35			18			12			
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$		220			95			60		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}	to Q_n		220			95			60			
t_{PHL}	Propagation Delay, MR to Q_n		220			90			60		ns	
t_{TLH}	Output Transition Time		65			35			25		ns	
t_{THL}			65			35			25			
t_wMR	MR Minimum Pulse Width		70			30			20		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wCP	CP_0 or $\overline{CP_1}$ Minimum Pulse Width		120			50			35		ns	
t_{rec}	MR Recovery Time		15			5			0		ns	
t_s	Set-Up Time, CP_0 to $\overline{CP_1}$		130			57			40		ns	
t_s	Set-Up Time, $\overline{CP_1}$ to CP_0		130			57			40		ns	
f_{MAX}	Input Count Frequency (Note 4)		4			10					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR CP_0, $\overline{CP_1}$ AND MR AND MR RECOVERY TIME



SET-UP AND HOLD TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0

CONDITIONS: $\overline{CP_1}$ = HIGH and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = LOW and the device triggers on a HIGH-to-LOW transition at $\overline{CP_1}$

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4519/34519

QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The F4519 provides four multiplexing circuits with common selection inputs; each circuit contains two inputs and one output. It may be used to select four bits of information from one of two sources. The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, the output (Z_a) is the logical Exclusive-NOR of the A_n and B_n input ($Z_n = A_n \odot B_n$). When S_A and S_B are LOW, the output (Z_n) is LOW, independent of the multiplexer inputs (A_n and B_n). The F4519 cannot be used to multiplex analog signals. The outputs utilize standard buffers for best performance.

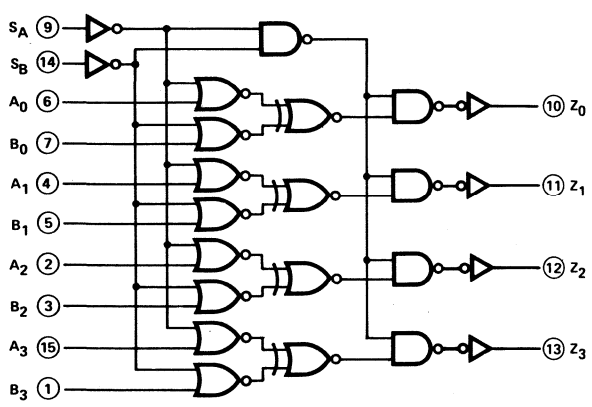
- **COMMON SELECT INPUTS**
- **FULLY BUFFERED OUTPUTS**

TRUTH TABLE

SELECT		INPUTS		OUTPUT
S_A	S_B	A_n	B_n	Z_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	L	L	H
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

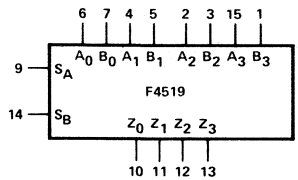
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC DIAGRAM



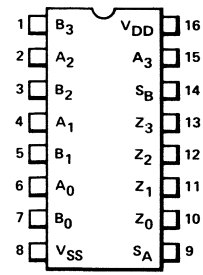
○ = Pin Number

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

S_A, S_B	Select Inputs (Active HIGH)
A_0-A_3, B_0-B_3	Multiplexer Inputs
Z_0-Z_3	Multiplexer Outputs

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			5			10		2		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					150			300		60			MAX	
		XM			0.5			1		0.2		μA	MIN, 25°C	
					30			60		12			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, S_n to Z_n		100			45			35		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			100			45			35			
t_{PLH}	Propagation Delay, A_n, B_n to Z_n		100			45			35		ns	
t_{PHL}			100			45			35			
t_{TLH}	Output Transition Time		35			20			10		ns	
t_{THL}			35			20			10			
t_{PLH}	Propagation Delay, S_n to Z_n		110			50			40		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			110			50			40			
t_{PLH}	Propagation Delay, A_n, B_n to Z_n		110			50			40		ns	
t_{PHL}			110			50			40			
t_{TLH}	Output Transition Time		65			35			15		ns	
t_{THL}			65			35			15			

NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4520/34520

DUAL 4-BIT BINARY COUNTER

DESCRIPTION — The F4520 is a Dual 4-Bit Internally Synchronous Binary Counter. Each counter has both an active HIGH Clock Input (CP_0) and an active LOW Clock Input ($\overline{CP}_1$), buffered Outputs from all four bit positions (Q_0-Q_3) and an active HIGH overriding asynchronous Master Reset Input (MR).

The counter advances on either the LOW-to-HIGH transition of the CP_0 Input if $\overline{CP}_1$ is HIGH or the HIGH-to-LOW transition of the $\overline{CP}_1$ Input if CP_0 is LOW (see the Truth Table). Either Clock Input (CP_0, $\overline{CP}_1$) may be used as the Clock Input to the counter and the other Clock Input may be used as a Clock Inhibit Input.

A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of the Clock Inputs (CP_0, $\overline{CP}_1$).

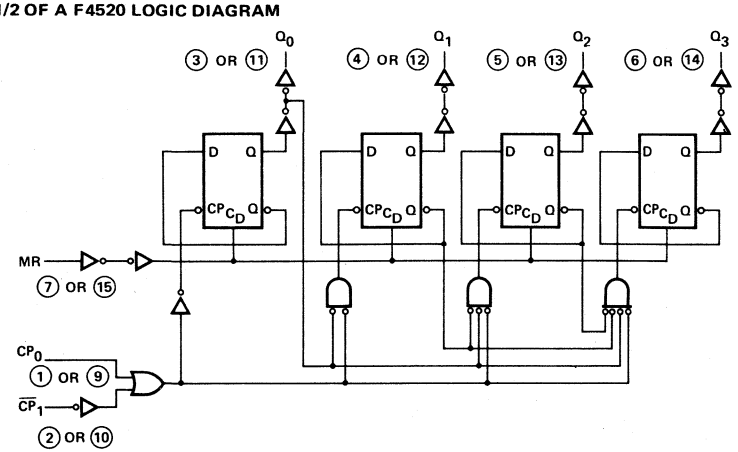
- **TYPICAL COUNT FREQUENCY OF 10 MHz AT V_{DD} = 10 V**
- **TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION**
- **ASYNCHRONOUS ACTIVE HIGH MASTER RESET**
- **BUFFERED OUTPUTS FROM ALL FOUR BIT POSITIONS**
- **FULLY SYNCHRONOUS COUNTING**

TRUTH TABLE

CP_0	$\overline{CP}_1$	MR	MODE
⎍	H	L	Counter Advances
L	⎎	L	Counter Advances
⎎	X	L	No Change
X	⎍	L	No Change
⎍	L	L	No Change
H	⎎	L	No Change
X	X	H	Reset (Asynchronous)

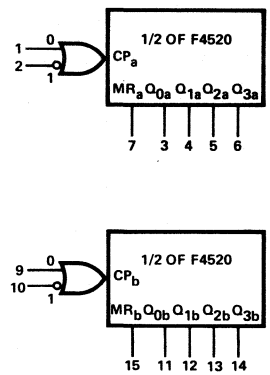
X = Don't Care
L = LOW Level
H = HIGH Level
⎍ = Positive-Going Transition
⎎ = Negative-Going Transition

1/2 OF A F4520 LOGIC DIAGRAM



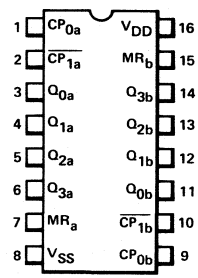
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

LOGIC SYMBOLS



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP_{0a}, CP_{0b}	Clock Input (L → H Triggered)
$\overline{CP}_{1a}$, CP_{1b}	Clock Input (H → L Triggered)
MR_a, MR_b	Master Reset Inputs
Q_{0a}–Q_{3a}	Outputs
Q_{0b}–Q_{3b}	Outputs

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

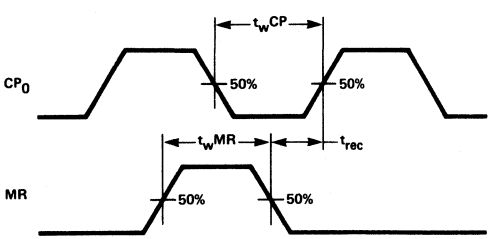
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		μA	MIN, 25°C	
					900			1500		300			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

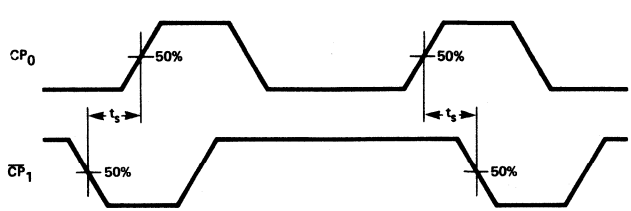
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$		200			85			55		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}	to Q_n		200			85			55			
t_{PHL}	Propagation Delay, MR to Q_n		200			80			55		ns	
t_{TLH}	Output Transition Time		35			18			12		ns	
t_{THL}			35			18			12			
t_{PLH}	Propagation Delay, CP_0 or $\overline{CP_1}$		220			95			60		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}	to Q_n		220			95			60			
t_{PHL}	Propagation Delay, MR to Q_n		220			90			60		ns	
t_{TLH}	Output Transition Time		65			35			25		ns	
t_{THL}			65			35			25			
t_wMR	MR Minimum Pulse Width		70			30			20		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_wCP	CP_0 or $\overline{CP_1}$ Minimum Pulse Width		120			50			35		ns	
t_{rec}	MR Recovery Time		15			5			0		ns	
t_s	Set-Up Time, CP_0 to $\overline{CP_1}$		130			57			40		ns	
t_s	Set-Up Time, $\overline{CP_1}$ to CP_0		130			57			40		ns	
f_{MAX}	Input Count Frequency (Note 4)		4			10					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR CP_0, $\overline{CP_1}$ AND MR AND MR RECOVERY TIME



SET-UP AND HOLD TIMES, CP_0 TO $\overline{CP_1}$ AND $\overline{CP_1}$ TO CP_0

CONDITIONS: $\overline{CP_1}$ = HIGH and the device triggers on a LOW-to-HIGH transition at CP_0. The timing also applies when CP_0 = LOW and the device triggers on a HIGH-to-LOW transition at $\overline{CP_1}$.

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4522/34522

PROGRAMMABLE 4-BIT BCD DOWN COUNTER

DESCRIPTION – The F4522 is a synchronous Programmable 4-Bit BCD Down Counter with an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP}_1$), an asynchronous Parallel Load Input (PL), four Parallel Inputs (P_0–P_3), a Carry Forward Input (CF), four buffered Parallel Outputs (Q_0–Q_3), a Terminal Count Output (TC) and an overriding asynchronous Master Reset Input (MR).

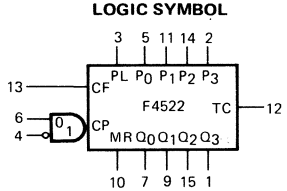
Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the active LOW Clock Input ($\overline{CP}_1$) are LOW, the counter advances on a LOW-to-HIGH transition of the active HIGH Clock Input (CP_0). When the Parallel Load Input (PL) is LOW and the active HIGH Clock Input (CP_0) is HIGH, the counter advances on a HIGH-to-LOW transition of the $\overline{CP}_1$ Input. The Terminal Count Output (TC) is HIGH when the counter is in the zero state (Q_0 = Q_1 = Q_2 = Q_3 = LOW) and the Carry Forward Input (CF) is HIGH. A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of other input conditions.

- **FULLY SYNCHRONOUS PROGRAMMABLE BCD DOWN COUNTER**
- **CLOCK INPUT EITHER HIGH-TO-LOW OR LOW-TO-HIGH EDGE-TRIGGERED**
- **ASYNCHRONOUS MASTER RESET**
- **CASCADABLE**
- **ASYNCHRONOUS PARALLEL LOAD**

PIN NAMES

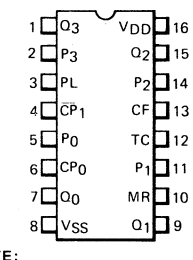
PL	Parallel Load Input
P_0–P_3	Parallel Inputs
CF	Carry Forward Input
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP}_1$	Clock Input (H→L Edge-Triggered)
MR	Asynchronous Master Reset Input
TC	TC Terminal Count Output
Q_0–Q_3	Buffered Outputs

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4526/34526

PROGRAMMABLE 4-BIT BINARY DOWN COUNTER

DESCRIPTION – The F4526 is a synchronous Programmable 4-Bit Binary Down Counter with an active HIGH and an active LOW Clock Input (CP_0, $\overline{CP}_1$), an asynchronous Parallel Load Input (PL), four Parallel Inputs (P_0–P_3), a Carry Forward Input (CF), four buffered Parallel Outputs (Q_0–Q_3), a Terminal Count Output (TC) and an overriding asynchronous Master Reset Input (MR).

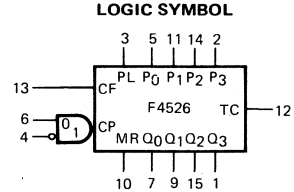
Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except Master Reset Input (MR) which must be LOW. When the Parallel Load Input (PL) and the active LOW Clock Input ($\overline{CP}_1$) are LOW, the counter advances on a LOW-to-HIGH transition of the active HIGH Clock Input (CP_0). When the Parallel Load Input (PL) is LOW and the active HIGH Clock Input (CP_0) is HIGH, the counter advances on a HIGH-to-LOW transition of the $\overline{CP}_1$ Input. The Terminal Count Output (TC) is HIGH when the counter is in the zero state (Q_0 = Q_1 = Q_2 = Q_3 = LOW) and the Carry Forward Input (CF) is HIGH. A HIGH on the Master Reset Input (MR) resets the counter (Q_0-Q_3 = LOW) independent of other input conditions.

- **FULLY SYNCHRONOUS PROGRAMMABLE BCD DOWN COUNTER**
- **CLOCK INPUT EITHER HIGH-TO-LOW OR LOW-TO-HIGH EDGE-TRIGGERED**
- **ASYNCHRONOUS MASTER RESET**
- **CASCADABLE**
- **ASYNCHRONOUS PARALLEL LOAD**

PIN NAMES

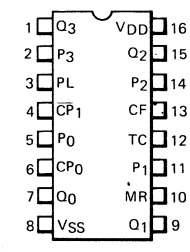
PL	Parallel Load Input
P_0–P_3	Parallel Inputs
CF	Carry Forward Input
CP_0	Clock Input (L→H Edge-Triggered)
$\overline{CP}_1$	Clock Input (H→L Edge-Triggered)
MR	Asynchronous Master Reset Input
TC	Terminal Count Output
Q_0–Q_3	Buffered Outputs

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4528/34528

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The F4528 is a Dual Retriggerable Resettable Monostable Multivibrator. Each Multivibrator has an active LOW Input ($\overline{I_0}$), an active HIGH Input (I_1), an active LOW Clear Direct Input ($\overline{C_D}$), an Output (Q), its Complement ($\overline{Q}$) and two pins for connecting the external timing components (C_{ext}, C_{ext}/R_{ext}). An external timing capacitor must be connected between C_{ext} and C_{ext}/R_{ext} and an external resistor must be connected between C_{ext}/R_{ext} and V_{DD}.

A HIGH-to-LOW transition on the $\overline{I_0}$ Input when the I_1 Input is LOW or a LOW-to-HIGH transition on the I_1 Input when the $\overline{I_0}$ Input is HIGH produces a positive pulse (L→H→L) on the Q Output and a negative pulse (H→L→H) on the $\overline{Q}$ Output if the Clear Direct Input ($\overline{C_D}$) is HIGH. A LOW on the Clear Direct Input ($\overline{C_D}$) forces the Q Output LOW, $\overline{Q}$ Output HIGH and inhibits any further pulses until the Clear Direct Input ($\overline{C_D}$) is HIGH.

- **RESETTABLE**
- **TRIGGER ON EITHER A HIGH-TO-LOW TRANSITION ON $\overline{I_0}$ OR A LOW-TO-HIGH TRANSITION ON I_1**
- **COMPLEMENTARY OUTPUTS AVAILABLE**

PIN NAMES

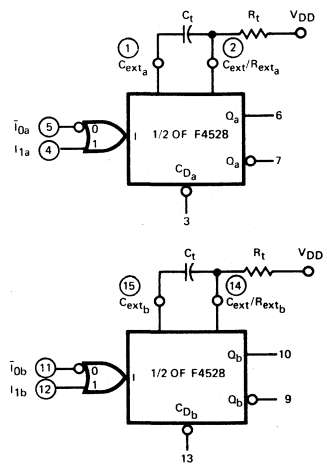
$\overline{I_{0a}}$, $\overline{I_{0b}}$	Input (H→L Triggered)
I_{1a}, I_{1b}	Input (L→H Triggered)
$\overline{CD_a}$, $\overline{CD_b}$	Clear Direct Input (Active LOW)
Q_a, Q_b	Output
$\overline{Q_a}$, $\overline{Q_b}$	Complimentary Output (Active LOW)
C_{exta}, C_{extb}	External Capacitor Connections
C_{ext}/R_{exta}, C_{ext}/R_{extb}	External Capacitor/Resistor Connections

TRUTH TABLE

$\overline{I_0}$	I_1	$\overline{C_D}$	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

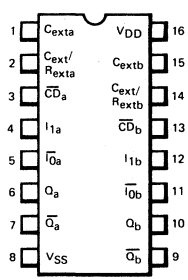
H = HIGH Level
L = LOW Level
H→L = HIGH-to-LOW Transition
L→H = LOW-to-HIGH Transition
X = Don't Care

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4531/34531
13-INPUT PARITY CHECKER GENERATOR

DESCRIPTION — The F4531 is a 13-Input Parity Checker/Generator with 13 Parity Inputs (I_0–I_{12}) and a Parity Output (Z). When the number of Parity Inputs that are HIGH is even, the Output (Z) is LOW. When the number of Parity Inputs that are HIGH is odd, the Output (Z) is HIGH. For words of 12 bits or less, the Output (Z) can be used to generate either odd or even parity by appropriate termination of the unused Parity Input (s). For words of 14 or more bits, the devices can be cascaded by connecting the output (Z) of one device to any Parity Input (I_0–I_{12}) of another device. When cascading devices, it is recommended that the Output (Z) of one device be connected to the I_{12} input of the other device since there is less delay to the Output (Z) from the I_{12} input than from any other Input (I_0-I_{11}).

- **VARIABLE WORD LENGTH**
- **FULLY BUFFERED OUTPUT (ACTIVE HIGH)**
- **PARITY INPUTS (ACTIVE HIGH)**

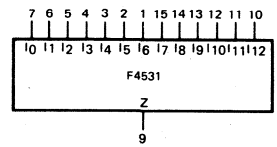
PIN NAMES	FUNCTION
I_0–I_{12}	Parity Inputs
Z	Buffered Output

TRUTH TABLE

INPUTS		OUTPUT
I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7 I_8 I_9 I_{10} I_{11} I_{12}		Z
All Thirteen	Inputs LOW	L
Any One	Input HIGH	H
Any Two	Inputs HIGH	L
Any Three	Inputs HIGH	H
Any Four	Inputs HIGH	L
Any Five	Inputs HIGH	H
Any Six	Inputs HIGH	L
Any Seven	Inputs HIGH	H
Any Eight	Inputs HIGH	L
Any Nine	Inputs HIGH	H
Any Ten	Inputs HIGH	L
Any Eleven	Inputs HIGH	H
Any Twelve	Inputs HIGH	L
All Thirteen	Inputs HIGH	H

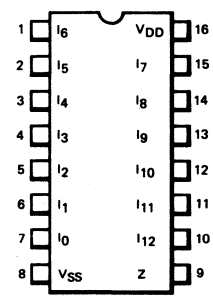
L = LOW Level
H = HIGH Level

LOGIC SYMBOL



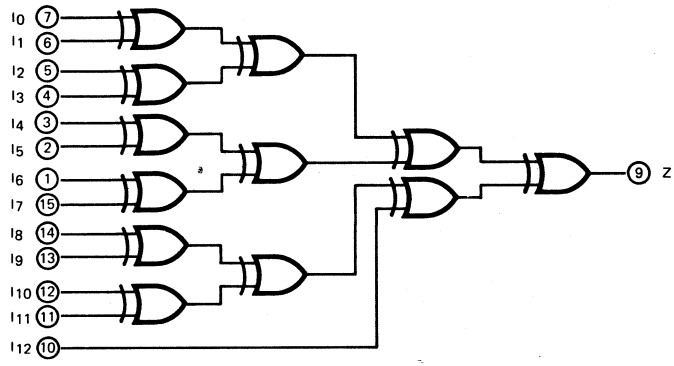
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
O = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					300			600		120			MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25 °C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_0-I_{11} to Z		175			70			50		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			175			70			50		ns	
t_{PLH}	Propagation Delay, I_{12} to Z		105			45			30		ns	
t_{PHL}			105			45			30		ns	
t_{TLH}	Output Transition Time		35			20			10		ns	
t_{THL}			35			20			10		ns	
t_{PLH}	Propagation Delay, I_0-I_{11} to Z		195			80			55		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			195			80			55		ns	
t_{PLH}	Propagation Delay, I_{12} to Z		115			50			35		ns	
t_{PHL}			115			50			35		ns	
t_{TLH}	Output Transition Time		65			35			15		ns	
t_{THL}			65			35			15		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4532/34532
8-INPUT PRIORITY ENCODER

DESCRIPTION – The F4532 is an 8-Input Priority Encoder with eight active HIGH Priority Inputs (I_0-I_7), three active HIGH Address Outputs (A_0-A_2), an active HIGH Enable Input (E_{In}), an active HIGH Enable Output (E_{Out}) and an active HIGH Group Select Output (GS).

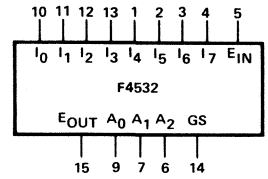
Data is accepted on the eight Priority Inputs (I_0-I_7). The binary code corresponding to the highest Priority Input (I_0-I_7) which is HIGH is generated on the Address Outputs (A_0-A_2) if the Enable Input (E_{In}) is HIGH. Priority Input I_7 is assigned the highest priority. The Group Select output (GS) is HIGH when one or more Priority Inputs (I_0-I_7) and the Enable Input (E_{In}) are HIGH. The Enable Output (E_{Out}) is HIGH when all the Priority Inputs (I_0-I_7) are LOW and the Enable Input (E_{In}) is HIGH. The Enable Input (E_{In}) when LOW, forces all Outputs (A_0-A_2, GS, E_{Out}) LOW.

- **ACTIVE HIGH PRIORITY INPUTS**
- **CASCADABLE**

PIN NAMES

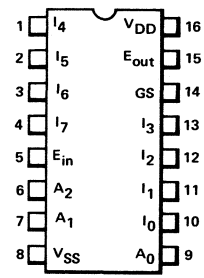
I_0-I_7	Priority Inputs
E_{In}	Enable Input
E_{Out}	Enable Output
GS	Group Select Output
A_0-A_2	Address Outputs

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



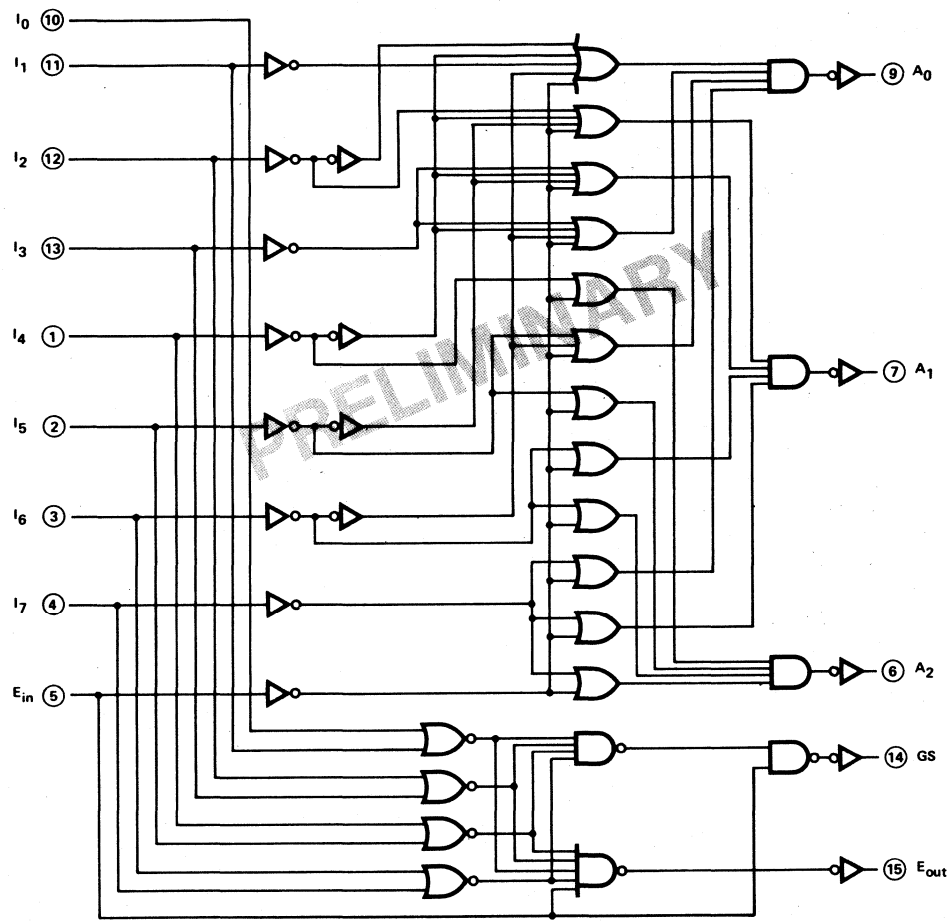
NOTE:
The Flatpak version, has the same pin-outs (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

INPUTS									OUTPUTS				
E_{In}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	A_2	A_1	A_0	E_{Out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

X = Don't Care
L = LOW Level
H = HIGH Level

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			5			10		2		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					70			140		28			MAX	
		XM			0.5			1		0.2		μA	MIN, 25°C	
					30			60		12			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, E_{IN} to E_{OUT}		75			40			30		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			75			40			30			
t_{PLH}	Propagation Delay, E_{IN} to GS		60			30			20		ns	
t_{PHL}			60			30			20			
t_{PLH}	Propagation Delay, E_{IN} to A_n		120			60			40		ns	
t_{PHL}			120			60			40			
t_{PLH}	Propagation Delay, I_n to A_n		125			60			45		ns	
t_{PHL}			125			60			45			
t_{PLH}	Propagation Delay, I_n to GS		120			55			40		ns	
t_{PHL}			120			55			40			
t_{TLH}	Output Transition Time		35			20			10		ns	
t_{THL}			35			20			10			
t_{PLH}	Propagation Delay, E_{IN} to E_{OUT}		85			45			35		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			85			45			35			
t_{PLH}	Propagation Delay, E_{IN} to GS		65			35			25		ns	
t_{PHL}			65			35			25			
t_{PLH}	Propagation Delay, E_{IN} to A_n		135			70			45		ns	
t_{PHL}			135			70			45			
t_{PLH}	Propagation Delay, I_n to A_n		135			70			50		ns	
t_{PHL}			135			70			50			
t_{PLH}	Propagation Delay, I_n to GS		135			60			45		ns	
t_{PHL}			135			60			45			
t_{TLH}	Output Transition Time		65			35			15		ns	
t_{THL}			65			35			15			

NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4539/34539
DUAL 4-INPUT MULTIPLEXER

DESCRIPTION – The F4539 is a Dual 4-Input Digital Multiplexer with common select logic. Each multiplexer has four Multiplexer Inputs (I_0-I_3), an active LOW Enable Input ($\overline{E}$) and a Multiplexer Output (Z). When HIGH, the Enable Input ($\overline{E}$) forces the Multiplexer Output (Z) of the respective multiplexer LOW, independent of the Select (S_0, S_1) and Multiplexer (I_0-I_3) Inputs. With the Enable Input ($\overline{E}$) LOW, the common Select Inputs (S_0, S_1) determine which Multiplexer Input (I_0-I_3) on each of the multiplexers is routed to the respective Multiplexer Output (Z).

- **COMMON SELECT LOGIC**
- **ACTIVE LOW ENABLES**

PIN NAMES

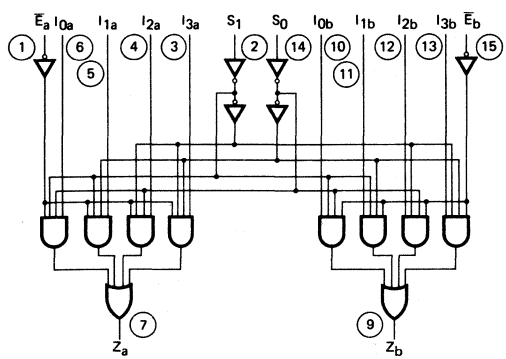
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs
I_{0b}, I_{1b}, I_{2b}, I_{3b}	
S_0, S_1	Select Inputs
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)
Z_a, Z_b	Multiplexer Outputs

TRUTH TABLE

INPUTS			OUTPUT
S_0	S_1	$\overline{E}$	Z
X	X	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

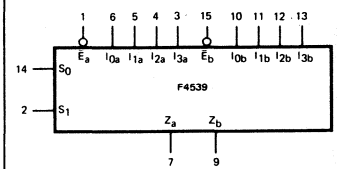
H = HIGH Level
L = LOW Level
X = Don't Care

LOGIC DIAGRAM



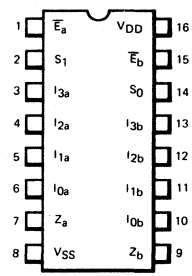
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			30			60		12		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					600			1200		240			MAX	
		XM			5			10		2		µA	MIN, 25°C	
					100			200		40			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, I_X to Z		145			61			43		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			120			50			33		ns	
t_{PLH}	Propagation Delay, Select to Z		190			78			55		ns	
t_{PHL}			192			78			55		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Z		100			42			29		ns	
t_{PHL}			96			42			32		ns	
t_{TLH}	Output Transition Time		38			19			12		ns	
t_{THL}			31			15			12		ns	
t_{PLH}	Propagation Delay, I_X to Z		166			71			51		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			140			58			40		ns	
t_{PLH}	Propagation Delay, Select to Z		210			88			62		ns	
t_{PHL}			210			88			62		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Z		120			53			37		ns	
t_{PHL}			118			51			38		ns	
t_{TLH}	Output Transition Time		76			39			29		ns	
t_{THL}			66			30			22		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4555/34555 • F4556/34556
DUAL 1-OF-4 DECODERS/DEMULTIPLEXERS

DESCRIPTION – The F4555 and F4556 are Dual 1-of-4 Decoders/Demultiplexers. Each decoder/demultiplexer has two Address Inputs (A_0, A_1), an active LOW Enable Input ($\overline{E}$) and four mutually exclusive Outputs which are active HIGH for the F4555 (O_0-O_3) and active LOW for the F4556 ($\overline{O}_0$-$\overline{O}_3$).

When the F4555 is used as a decoder, the Enable Input ($\overline{E}$) when HIGH, forces all Outputs (O_0-O_3) LOW. When used as a demultiplexer, the appropriate Output is selected by the data on the Address Inputs (A_0, A_1) and follows as the inverse of the Enable Input ($\overline{E}$). All unselected Outputs are LOW.

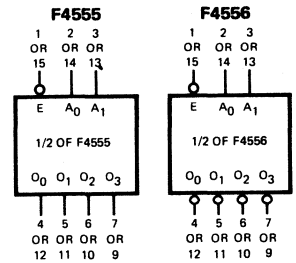
When the F4556 is used as a decoder, the Enable Input ($\overline{E}$) when HIGH forces all Outputs ($\overline{O}_0$-$\overline{O}_3$) HIGH. When used as a demultiplexer, the appropriate Output is selected by the data on the Address Inputs (A_0, A_1) and follows the state of the Enable Input ($\overline{E}$). All unselected Outputs are HIGH.

- **ACTIVE HIGH OUTPUTS FOR THE F34555 AND ACTIVE LOW OUTPUTS FOR THE F34556**
- **OVERRIDING ACTIVE LOW ENABLE**

PIN NAMES

$\overline{E}$	Enable Input (Active LOW)
A_0, A_1	Address Inputs
O_0-O_3	Outputs (Active HIGH – F4555 Only)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW – F4556 Only)

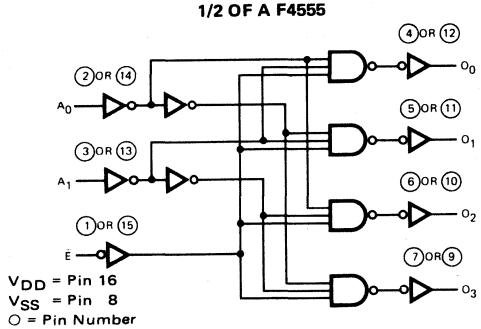
LOGIC SYMBOLS



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

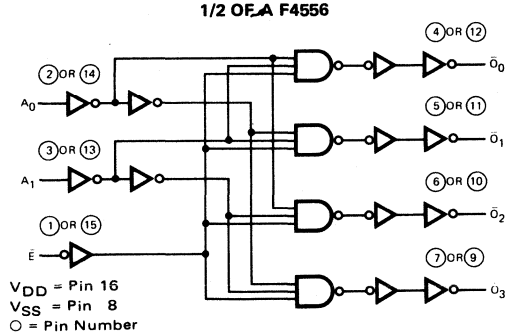
LOGIC DIAGRAMS

1/2 OF A F4555



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

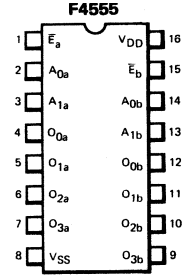
1/2 OF A F4556



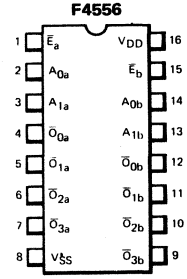
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAMS
DIP (TOP VIEW)

F4555



F4556



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F4555 TRUTH TABLE

$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

F4556 TRUTH TABLE

$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			20			40		8		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					200			400		80			MAX	
		XM			2			4		0.8		μA	MIN, 25°C	
					100			200		40			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0V, T_A = 25°C, F4555 only (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Address to Output		130			54			33		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			105			45			40		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		130			51			32		ns	
t_{PHL}			105			45			32		ns	
t_{TLH}	Output Transition Time		35			15			12		ns	
t_{THL}			33			13			10		ns	
t_{PLH}	Propagation Delay, Address to Output		148			60			40		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			127			54			45		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		148			60			40		ns	
t_{PHL}			127			53			40		ns	
t_{TLH}	Output Transition Time		65			20			25		ns	
t_{THL}			66			25			20		ns	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0V, T_A = 25°C, F4556 only (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Address to Output		120			48			33		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}			160			58			40		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		114			45			32			
t_{PHL}			125			50			32		ns	
t_{TLH}	Output Transition Time		37			18			12		ns	
t_{THL}			35			15			10		ns	
t_{PLH}	Propagation Delay, Address to Output		140			57			40		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}			185			68			45		ns	
t_{PLH}	Propagation Delay, $\overline{E}$ to Output		134			55			40		ns	
t_{PHL}			145			58			40		ns	
t_{TLH}	Output Transition Time		75			37			25		ns	
t_{THL}			77			29			20		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

F4582/34582
CARRY LOOKAHEAD GENERATOR

DESCRIPTION – The F4582 is a Lookahead Carry Generator which provides high speed lookahead over word lengths of more than four bits. The device has a Carry Input (C_n), four active LOW Carry Generate Inputs (G_0-G_3), four active LOW Carry Propagate Inputs (P_0-P_3), three Carry Outputs (C_{n+x},C_{n+y},C_{n+z}), an active LOW Carry Propagate Output (P) and an active LOW Carry Generate Output (G). The logic equations for all outputs are shown below.

- **EXPANDABLE TO ANY NUMBER OF BITS**
- **HIGH SPEED LOOKAHEAD OVER WORD LENGTHS OF MORE THAN FOUR BITS**

PIN NAMES

C_n	Carry Input
$\overline{G}_0$-$\overline{G}_3$	Carry Generate Inputs (Active LOW)
$\overline{P}_0$-$\overline{P}_3$	Carry Propagate Inputs (Active LOW)
C_{n+x},C_{n+y},C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)

LOGIC EQUATIONS

$$C_{n+x} = G_0 + P_0 \cdot C_n$$

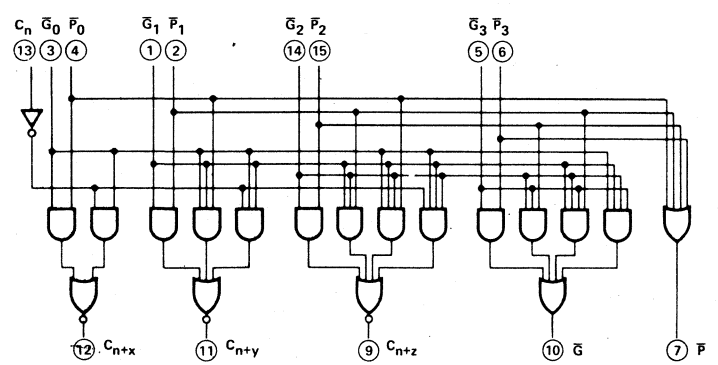
$$C_{n+y} = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_n$$

$$C_{n+z} = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_n$$

$$\overline{G} = \overline{G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0}$$

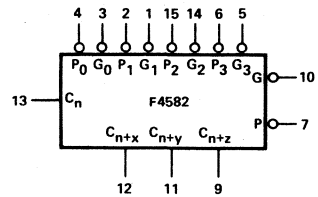
$$\overline{P} = \overline{P_3 \cdot P_2 \cdot P_1 \cdot P_0}$$

LOGIC DIAGRAM



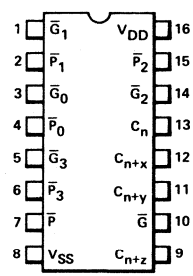
V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			5			10		2		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					150			300		60			MAX	
		XM			0.5			1.0		0.2		μA	MIN, 25°C	
					30			60		12			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, C_n to C_{n+x},		140			65			45		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}	C_{n+y} or C_{n+z}		140			65			45			
t_{PLH}	Propagation Delay, $\overline{P_n}$ to C_{n+x},		140			65			45		ns	
t_{PHL}	C_{n+y} or C_{n+z}		140			65			45			
t_{PLH}	Propagation Delay, $\overline{G_n}$ to C_{n+x},		140			65			45		ns	
t_{PHL}	C_{n+y} or C_{n+z}		140			65			45			
t_{PLH}	Propagation Delay, $\overline{P_1}$, $\overline{P_2}$, $\overline{P_3}$		140			65			45		ns	
t_{PHL}	to $\overline{G}$		140			65			45			
t_{PLH}	Propagation Delay, $\overline{G_n}$ to $\overline{G}$		140			65			45		ns	
t_{PHL}			140			65			45			
t_{PLH}	Propagation Delay, $\overline{P_n}$ to $\overline{P}$		140			65			45		ns	
t_{PHL}			140			65			45			
t_{TLH}	Output Transition Time		30			17			13		ns	
t_{THL}			30			17			13			
t_{PLH}	Propagation Delay, C_n to C_{n+x},		160			75			55		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}	C_{n+y} or C_{n+z}		160			75			55			
t_{PLH}	Propagation Delay, $\overline{P_n}$ to C_{n+x},		160			75			55		ns	
t_{PHL}	C_{n+y} or C_{n+z}		160			75			55			
t_{PLH}	Propagation Delay, $\overline{G_n}$ to C_{n+x},		160			75			55		ns	
t_{PHL}	C_{n+y} or C_{n+z}		160			75			55			
t_{PLH}	Propagation Delay, $\overline{P_1}$, $\overline{P_2}$, $\overline{P_3}$		160			75			55		ns	
t_{PHL}	to $\overline{G}$		160			75			55			
t_{PLH}	Propagation Delay, $\overline{G_n}$ to $\overline{G}$		160			75			55		ns	
t_{PHL}			160			75			55			
t_{PLH}	Propagation Delay, $\overline{P_n}$ to $\overline{P}$		160			75			55		ns	
t_{PHL}			160			75			55			
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20			

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G_0}$	$\overline{P_0}$	$\overline{G_1}$	$\overline{P_1}$	$\overline{G_2}$	$\overline{P_2}$	$\overline{G_3}$	$\overline{P_3}$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

F4702/34702

PROGRAMMABLE BIT RATE GENERATOR

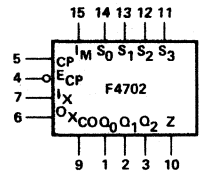
FAIRCHILD MACROLOGIC™ CMOS

DESCRIPTION – The F4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as Universal Asynchronous Receiver and Transmitter circuits (UARTs). It generates any of the 14 commonly used bit rates using an on-chip crystal oscillator, but it's design also provides for easy and economical multichannel operation, where any of the possible frequencies must be made available on any output channel.

One F4702 can control up to eight output channels. When more than one bit rate generator is required, they can still be operated from one crystal.

- PROVIDES 14 COMMONLY USED BIT RATES
- ONE F4702 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- USES 2.4576 MHz INPUT FOR STANDARD FREQUENCY OUTPUTS (16 TIMES BIT RATE)
- CONFORMS TO EIA RS-404
- ON-CHIP INPUT PULL UP CIRCUITS
- TTL COMPATIBLE–OUTPUTS WILL SINK 1.6 mA
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- LOW POWER DISSIPATION–1.35 mA POWER DISSIPATION AT 5 V AND 2.4576 MHz
- 16-PIN DUAL IN-LINE PACKAGE

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	$\overline{E_{CP}}$	CP	OPERATION
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍⎍	Reset During First CP = HIGH Time

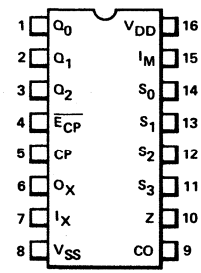
H = HIGH Level
L = LOW Level
X = Don't Care
⎍⎍ = 1st HIGH Level Clock Pulse After $\overline{E_{CP}}$ Goes LOW
⎍⎍⎍ Clock Pulses

Note : Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576 MHz.

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

CONNECTION DIAGRAM
DIP (TOP VIEW)

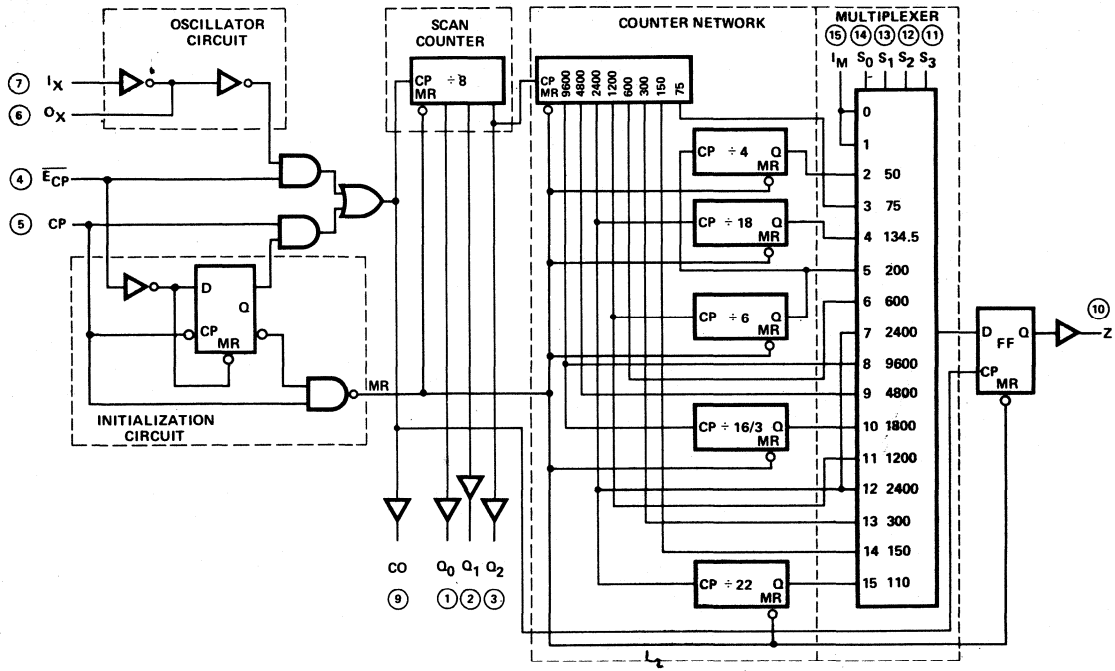


NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

CP	External Clocl Input
$\overline{E_{CP}}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

FUNCTIONAL DESCRIPTION – Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud interfacing with electromechanical devices, to 9600 baud for high speed modems. Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the receiver requires a clock rate that is a multiple of the incoming bit rate. Popular MOS-LSI UART circuits use a clock that is 16 times the transmitted bit rate. The F4702 can generate 14 standardized clock rates from one common high frequency input.

The F4702 contains the following five functional subsystems which are discussed in detail below:

1. An Oscillator Circuit with associated gating.
2. A Prescaler used as scan counter for multichannel operation (described in the applications section).
3. A network of Counter Chains to generate the required standardized frequencies.
4. An Output Multiplexer (frequency selector) with resynchronizing output flip-flop.
5. An Initializing (reset) Circuit.

OSCILLATOR

For conventional operation generating 16 output clock pulses ber bit period, the input clock frequency must be 2.4576 MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will obviously result in a proportionally lower output frequency.

The F4702 can be driven from two alternate clock sources: (1) When the $\overline{E_{CP}}$ (active LOW External Clock Enable) input is LOW, the CP input is the clock source. (2) When the $\overline{E_{CP}}$ input is HIGH, a crystal connected between I_X and O_X, or a signal applied to the I_X input is the clock source.

PRESCALER (SCAN COUNTER)

The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered Outputs Q_0, Q_1, and Q_2. This prescaler is of no particular advantage in single frequency applications, but it is essential for the simple economical multichannel scheme described in the Application section of this data sheet.

COUNTER NETWORK

The prescaler Output Q_2 is a square wave of 1/8 the input frequency and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the Block Diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576 MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is 16 x 9.6 kHz = 153.6 kHz. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200,
bit rate 200 is divided by 4 to generate bit rate 50,
bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of −0.87%,
bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of −0.83%, and
bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the ÷ 16 feature of the UART, the resulting distortion is less than 0.78%, irrespective of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

OUTPUT MULTIPLEXER

The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select Inputs (S_0-S_3). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered Output (Z) that is synchronous with the prescaler Outputs (Q_0-Q_2). Table 2 lists the correspondence between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, non-standardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

INITIALIZATION (RESET)

The initialization circuit generates a common master reset signal for all flip-flops in the F4702. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the $\overline{E_{CP}}$ input goes LOW. When E_{CP} is HIGH, selecting the Crystal Input, CP must be LOW. A HIGH level on CP would apply a continuous reset.

All inputs to the F4702, except I_X have on-chip pull up circuits which improve TTL compatibility and eliminate the need to tie a permanently HIGH input to V_{DD}.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage	
V_{OH}	Output HIGH Voltage		4.99 4.95			V	MIN, 25°C MAX	I_{OH} = 0 mA, Inputs at 0 or 5 V per the Logic Function or Truth Table	
			4.0			V	All	I_{OH} = 0 mA, Inputs at 1.5 or 3.5 V	
V_{OL}	Output LOW Voltage				0.01 0.05	V	MIN, 25°C MAX	I_{OL} = 0 mA, Inputs at 0 or 5 V per the Logic Function or Truth Table	
					0.5	V	All	I_{OL} = 0 mA, Inputs at 1.5 or 3.5 V	
I_{IL} (See Note 5)	Input LOW Current for Input I_X	XC			−0.1	µA	25°C	Pin Under Test at 0 V All Other Inputs Simultaneously at 5 V	
		XM			−0.01				
	Input LOW Current for all Other Inputs	XC		−30					
		XM		−30					
I_{IH}	Input HIGH Current for Input I_X	XC			0.1	µA	25°C	Pin Under Test at 5 V All Other Inputs Simultaneously at 0 V	
		XM			0.01				
	Input HIGH Current for all Other Inputs	XC			0.1				
		XM			0.01				
I_{OH}	Output HIGH Current for all Output O_X		−0.5 −0.3 −0.1			mA	MIN, 25°C MAX	V_{OUT} = 4.5 V	Inputs at 0 or 5 V per Logic Function or Truth Table
	Output HIGH Current for all Other Outputs		−1.5 −1.0			mA	MIN, 25°C MAX	V_{OUT} = 2.5 V	
			−0.5 −0.3			mA	MIN, 25°C MAX	V_{OUT} = 4.5 V	
I_{OL}	Output LOW Current for all Output O_X		0.2 0.2 0.1			mA	MIN, 25°C MAX	V_{OUT} = 0.4 V	
	Output LOW Current for all Other Outputs		3.2 3.2 1.6			mA	MIN, 25°C MAX		
I_{DD}	Quiescent Power Supply Current	XC			100 1000	µA	MIN, 25°C MAX	$\overline{E_{CP}}$ = V_{DD}, CP = 0 V, All Other Inputs Common and at 0 V or V_{DD}	
		XM			10 150	µA	MIN, 25°C MAX		

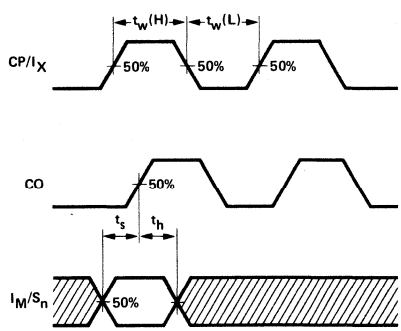
See Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		105			55			35		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PHL}	I_X to CO		105			55			35			
t_{PLH}	Propagation Delay,		80			40			30		ns	
t_{PHL}	CP to CO		80			40			30			
t_{PLH}	Propagation Delay,		40			20			15		ns	
t_{PHL}	CO to Q_n		40			20			15			
t_{PLH}	Propagation Delay,		50			25			20		ns	
t_{PHL}	CO to Z		50			25			20			
t_{TLH}	Output Transition		50			25			15		ns	
t_{THL}	Time		35			20			10			
t_{PLH}	Propagation Delay,		150			75			55		ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PHL}	I_X to CO		150			75			55			
t_{PLH}	Propagation Delay,		100			50			35		ns	
t_{PHL}	CP to CO		100			50			35			
t_{PLH}	Propagation Delay,		60			30			25		ns	
t_{PHL}	CO to Q_n		60			30			25			
t_{PLH}	Propagation Delay,		70			35			25		ns	
t_{PHL}	CO to Z		70			35			25			
t_{TLH}	Output Transition		70			35			25		ns	
t_{THL}	Time		40			25			15			
t_s	Set-Up Time, Select to CO		150			100			75		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_h	Hold Time, Select to CO		−10			−7			−5			
t_s	Set-Up Time, I_M to CO		150			70			50		ns	
t_h	Hold Time, I_M to CO		−10			−7			−5			
$t_wCP(L)$	Minimum Clock Pulse Width,		150			75			50		ns	
$t_wCP(H)$	LOW and HIGH		150			75			50			
$t_wI_X(L)$	Minimum I_X Pulse Width,		150			75			50		ns	
$t_wI_X(H)$	LOW and HIGH		150			75			50			

NOTES:
1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull up circuits on all inputs except I_X. This is done for TTL compatibility.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. The first HIGH Level Clock Pulse after $\overline{E}_{CP}$ goes LOW must be at least 350 ns long to guarantee reset of all Counters.
5. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CP AND I_X PULSE WIDTHS AND SET-UP AND HOLD TIMES, SELECT INPUT (S_n) TO CLOCK OUTPUT (CO) AND I_M INPUT TO CLOCK OUTPUT (CO)

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

APPLICATIONS

SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the F4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals these five bit rates are adequate.

SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

Fixed Programmed Multichannel Operation

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one F4702 and one 93L34 8-Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the F4702 to interrogate sequentially the state of eight different frequency signals. The 93L34 8-Bit Addressable Latch, addressed by the same Scan Counter Outputs, reconverts the multiplexed single Output (Z) of the F4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0:	110 Baud,	Q_1:	9600 Baud,	Q_2:	4800 Baud,	Q_3:	1800 Baud,
Q_4:	1200 Baud,	Q_5:	2400 Baud,	Q_6:	300 Baud,	Q_7:	150 Baud.

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

Fully Programmable Multichannel Operation

Figure 3 shows a fully programmable 8-channel bit rate generator system that, under computer control, generates arbitrarily assigned bit rates on all eight outputs simultaneously. The basic operation is similar to the previously described fixed programmed system, but two 9LS170 4 x 4 Register File MSI packages are connected as programmable look-up tables between the Scan Counter Outputs (Q_0 to Q_2) and the multiplexer Select Inputs (S_0 to S_3). The content of this 8-word by 4-bit memory determines which frequency appears at what output.

19200 Baud Operation

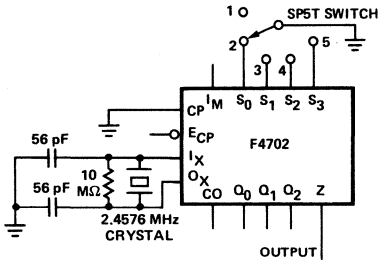
Though a 19200 Baud signal is not internally routed to the multiplexer, the F4702 can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code 0 or 1. An additional 2-input NAND gate can be used to retain the "Zero Baud" feature on select code 0. Any multichannel operation that involves 19200 Baud must be limited to four outputs as shown in Figure 4. Only the two least significant Scan Counter Outputs are used, so that the scan is completed within one half period of the 19200 output frequency.

CLOCK EXPANSION

One F4702 can control up to eight output channels. For more than eight channels, additional Bit Rate Generators are required. These Bit Rate Generators can all be run from the same crystal or clock input. Figure 5 shows one possible expansion scheme. One F4702 is provided with a crystal. All other devices derive their clock from this master. Figure 6 shows a different scheme where the master clock output feeds into the I_X input of all slaves and all $\overline{E_{CP}}$ inputs are normally held HIGH. This scheme retains the reset feature and the selection between two different clock sources of the basic F4702 circuit.

During normal operation, the common $\overline{E_{CP}}$ line is HIGH and the common clock line (CP) is LOW. For diagnostic purposes the common $\overline{E_{CP}}$ is forced LOW. This deselects the crystal frequency and initiates the diagnostic mode. When CP goes HIGH for the first time, all F4702s are reset through their individual on-chip initialization circuitry. Subsequent LOW-to-HIGH clock transitions on the common CP line advance the scan counter, causing all F4702s to operate synchronously.

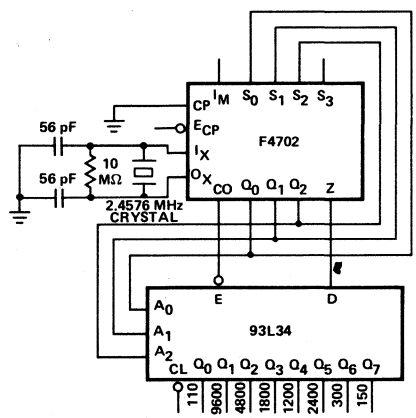
TYPICAL APPLICATIONS



SWITCH POSITION	BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

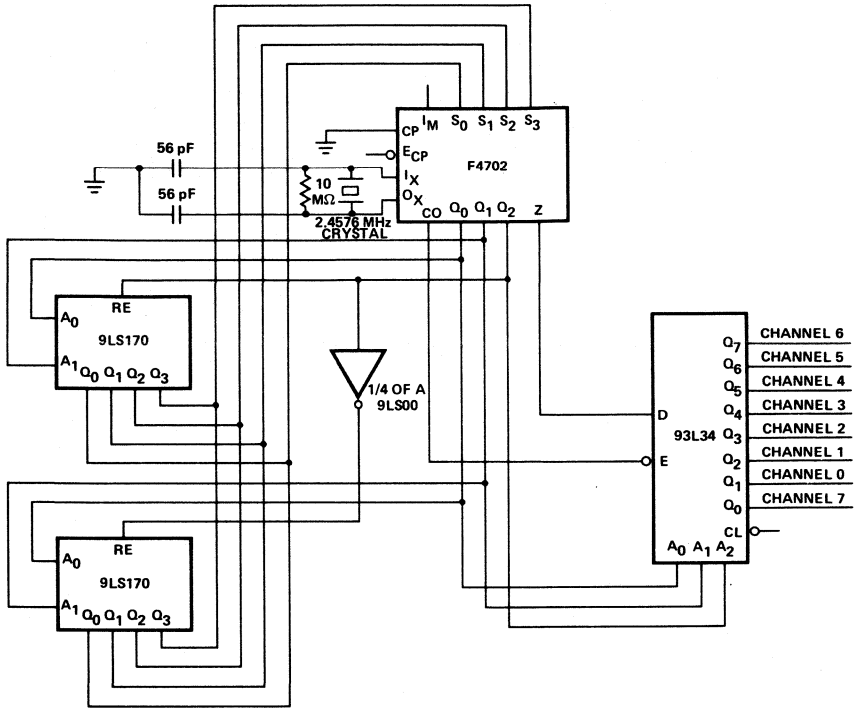
Fig. 1



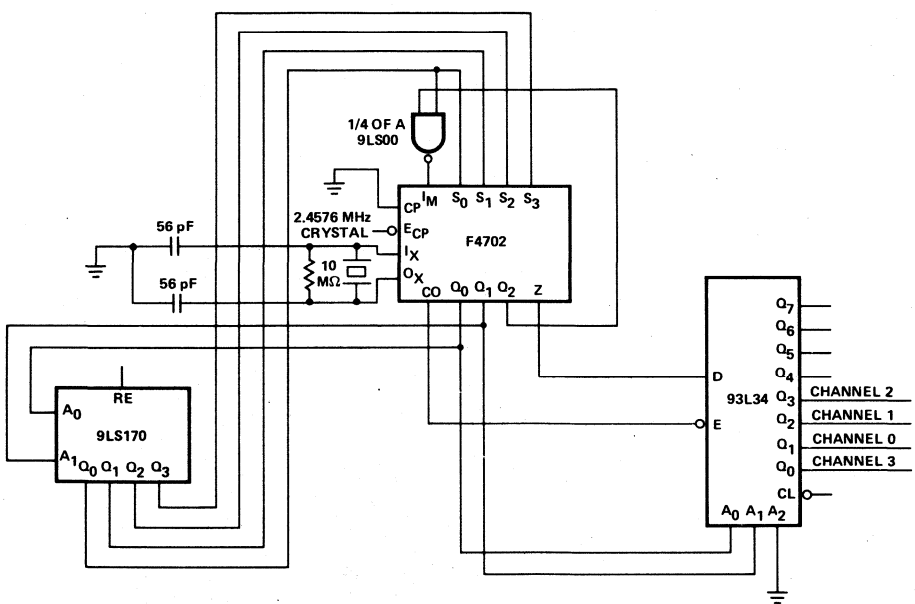
BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

Fig. 2

TYPICAL APPLICATIONS (Cont'd)



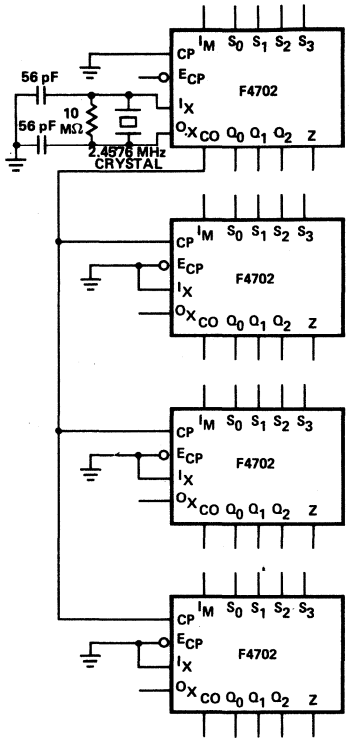
FULLY PROGRAMMABLE 8-CHANNEL BIT RATE GENERATOR SYSTEM
Fig. 3



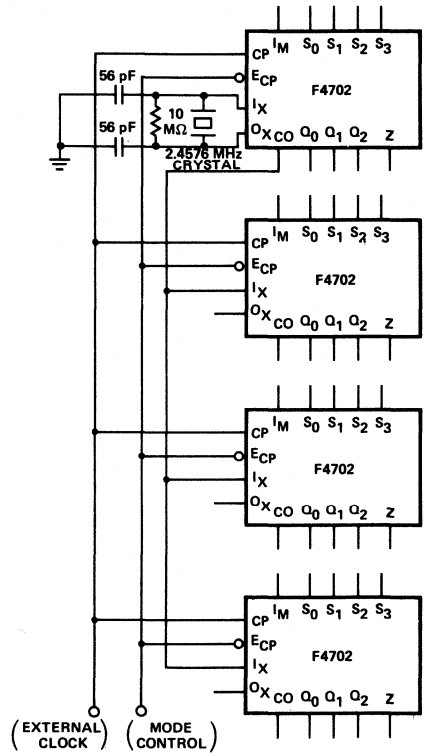
FULLY PROGRAMMABLE 4-CHANNEL BIT RATE GENERATOR SYSTEM WITH THE 19.2k BAUD FEATURE
Fig. 4

4

TYPICAL APPLICATIONS (Cont'd)



CASCADE CLOCK EXPANSION SCHEME
Fig. 5



TANDEM CLOCK EXPANSION SCHEME
Fig. 6

CRYSTAL SPECIFICATION RECOMMENDATIONS – Table 3 is a convenient listing of recommended crystal specifications. Crystal manufacturers are also listed below.

TABLE 3 CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250 Ω
Unwanted Modes	–6.0 dB (Min)
Type of Operation	Parallel
Load Capacitance	32 pF ±0.5

CRYSTAL MANUFACTURERS

CTS Knights, Inc.
Sandwich, Ill. 60548
(815) 786-8411
Crystal #F1004

X - Tron Electronics
1869 National Ave.
Hayward, Calif.
(415) 783-2145

Erie Frequency Control
499 Lincoln St.
Carlisle, Pa. 17013
(717) 249-2232

International Crystal Mfg. Company
10 No. Lee
Oklahoma City, Okla. 73102
(405) 236-3741

Sentry Manufacturing Co.
Crystal Park
Chickasha, Oklahoma 73018
(405) 224-6780

F4703/34703

16 × 4 PARALLEL/SERIAL FIFO

FAIRCHILD MACROLOGIC™ CMOS

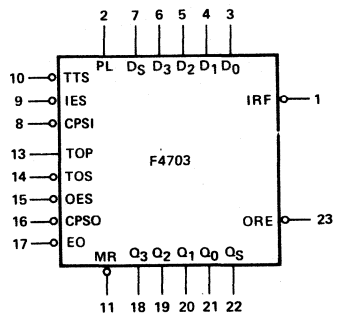
DESCRIPTION – The F4703 is an expandable high speed First-In First Out (FIFO) buffer memory with totally asynchronous and independent data inputs and outputs, in either serial or 4-bit parallel form. It can be extended to any number of words and to any number of parallel bits without additional circuitry and without compromising any features. It has 3-state output buffers which provide added versatility and make the F4703 compatible with the other circuits of the bus-oriented Macrologic CMOS family.

- **2 MHz DATA RATE**
- **SERIAL OR PARALLEL INPUT**
- **SERIAL OR PARALLEL OUTPUT**
- **EXPANDABLE WITHOUT EXTERNAL LOGIC**
- **3-STATE FULLY BUFFERED OUTPUTS**
- **24-PIN PACKAGE**
- **NEW SLIM 24-PIN DIP**

PIN NAMES

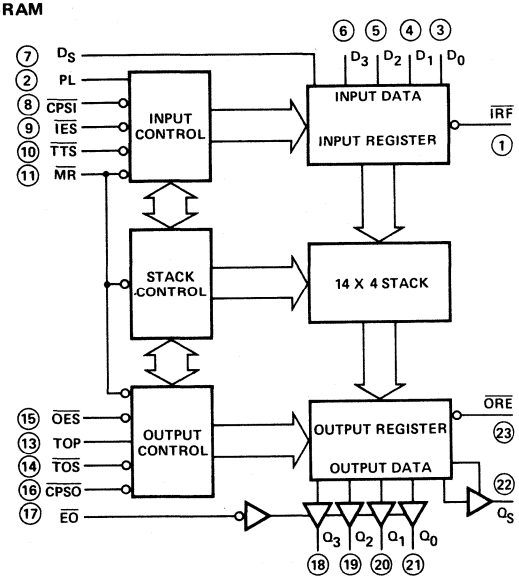
D_0-D_3	Parallel Data Inputs
D_S	Serial Data Input
PL	Parallel Load Input
$\overline{CPSI}$	Serial Input Clock Input (HIGH-to-LOW Triggered)
$\overline{CPSO}$	Serial Output Clock Input (HIGH-to-LOW Triggered)
$\overline{IES}$	Serial Input Enable (Active LOW)
$\overline{TTS}$	Transfer to Stack Input (Active LOW)
$\overline{TOS}$	Transfer Out Serial Input (Active LOW)
TOP	Transfer Out Parallel Input
$\overline{OES}$	Serial Output Enable Input (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{IRF}$	Input Register Full Output (Active LOW)
$\overline{ORE}$	Output Register Empty Output (Active LOW)
Q_0-Q_3	Parallel Data Outputs
Q_S	Serial Data Output

LOGIC SYMBOL

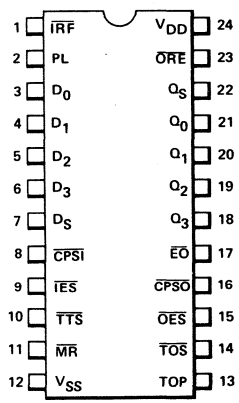


V_{DD} = Pin 24
V_{SS} = Pin 12

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

FUNCTIONAL DESCRIPTION – As shown in the block diagram, the F4703 consists of three parts: 1) an input register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion. 2) a 4-bit wide, 14-word deep fall-through stack with self-contained control logic. 3) an output register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion. Since these three sections operate asynchronously and almost independently, they will be described separately below:

INPUT REGISTER (DATA ENTRY):
The input register can receive data in either bit-serial or in 4-bit parallel form, store it until it is sent to the fall-through stack, and generate and accept the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The $\overline{Q}$ output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

PARALLEL ENTRY:
A HIGH level on the PL input loads the D_0-D_3 data inputs into the F_0-F_3 flip-flops and sets the FC flip-flop, which forces $\overline{IRF}$ LOW, indicating "input register full". The D inputs must be stable while PL is HIGH. During parallel entry the $\overline{IES}$ input should be LOW; the $\overline{CPSI}$ input may be either HIGH or LOW.

SERIAL ENTRY:
Data on the DS input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the $\overline{CPSI}$ clock input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition the four serial data bits are aligned in the four data flip-flops and the FC flip-flop is set, forcing $\overline{IRF}$ LOW (input register full) and internally inhibiting further $\overline{CPSI}$ clock pulses.

Figure 3 illustrates the final positions in a F4703 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit.

TRANSFER TO THE FALL-THROUGH STACK:
The outputs of the flip-flops F_0-F_3 feed the stack. A LOW level on the $\overline{TTS}$ input attempts to initiate a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

Data falls through the stack automatically, pausing only when it is necessary for an empty next location. In the F4703, like in most modern FIFO designs, the $\overline{MR}$ input initializes the stack control section only and does not clear the data.

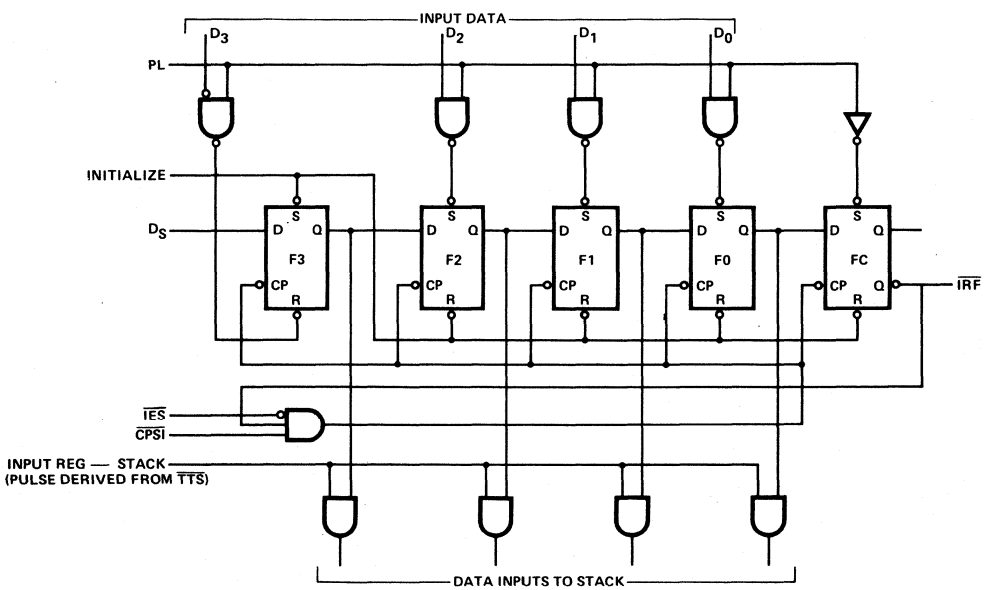


Fig. 1 CONCEPTUAL INPUT SECTION

OUTPUT REGISTER (DATA EXTRACTION):

The output register receives a 4-bit data word from the bottom stack location, stores it and puts it on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. Figure 2 is a conceptual logic diagram of the output section.

PARALLEL DATA EXTRACTION:

When the FIFO is empty (after a LOW pulse is applied to $\overline{MR}$), the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, provided the "Transfer Out Parallel" (TOP) input is HIGH, and the $\overline{OES}$ input is LOW. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled).

TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next LOW-to-HIGH transition of TOP transfers the next word (if available) into the output register as explained above. During parallel data extraction $\overline{TOS}$, $\overline{CPSO}$ and $\overline{OES}$ should be LOW.

SERIAL DATA EXTRACTION:

When the FIFO is empty (after a LOW pulse is applied to $\overline{MR}$), the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output shift register provided the "Transfer Out Serial" ($\overline{TOS}$) input is LOW. TOP must be HIGH, and $\overline{OES}$ and $\overline{CPSO}$ must be LOW.

As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the shift register. The 3-state serial data output Q_S is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW and disables the serial output Q_S. For serial operation the $\overline{ORE}$ output is tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

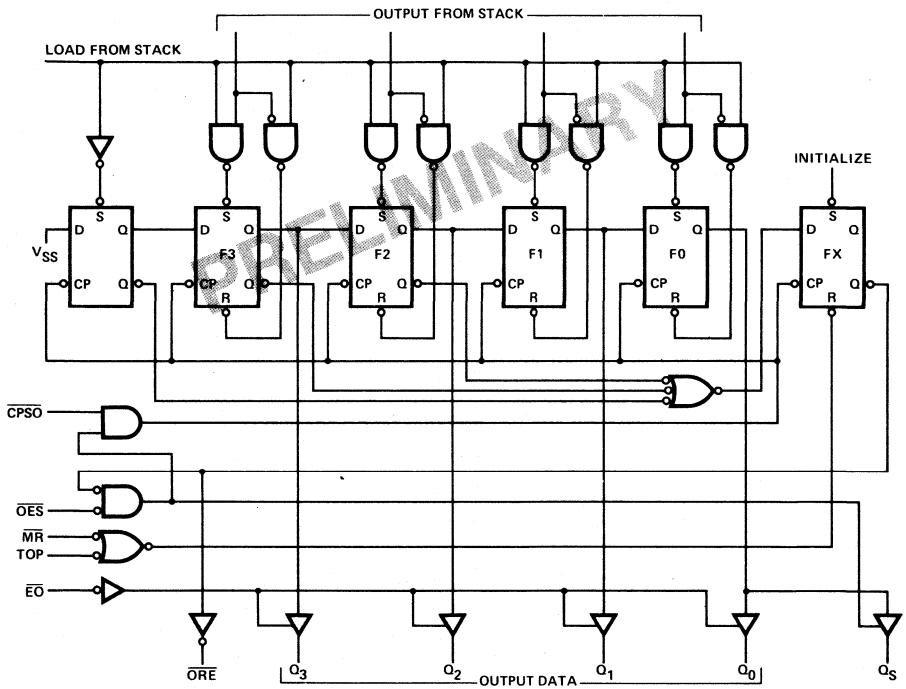


Fig. 2 CONCEPTUAL OUTPUT SECTION

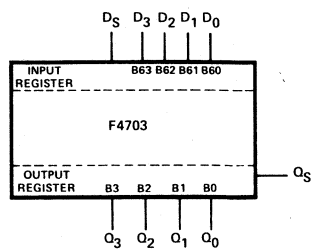


Fig. 3 FINAL POSITIONS IN A F4703 RESULTING FROM A 64-BIT SERIAL TRAIN

EXPANSION

VERTICAL EXPANSION — The F4703 can be vertically expanded to store more words without any external parts. The interconnections necessary to form a 46-word by 4-bit FIFO are shown in Figure 4. Using the same technique, any FIFO of 15n + 1 words by four bits can be constructed. Note that expansion does not sacrifice any of the FIFO's flexibility for Serial/Parallel input and output.

HORIZONTAL EXPANSION — The F4703 can also be horizontally expanded to store long words (in multiples of four bits) without any external logic. The inter-connections necessary to form a 16-word by 12-bit FIFO are shown in Figure 5. Using the same technique, any FIFO of 16 words by 4 x n bits can be constructed. When expanding in the horizontal direction, it is necessary to connect the $\overline{IRF}$ and $\overline{ORE}$ outputs of the right most device (most significant device) to the $\overline{TTS}$ and $\overline{TOS}$ inputs respectively of all devices to the left (less significant devices).

As in the vertical expansion scheme, horizontal expansion does not require sacrificing any of the FIFO's flexibility for Serial/Parallel input and output.

HORIZONTAL AND VERTICAL EXPANSION — The F4703 can be expanded in both the horizontal and vertical direction without any external parts and without sacrificing any of the FIFO's flexibility for Serial/Parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in Figure 6.

Figures 7 and 8 show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in Figure 6. The final position of data after serial insertion of 496 bits into the FIFO array of Figure 6 is shown in Figure 9.

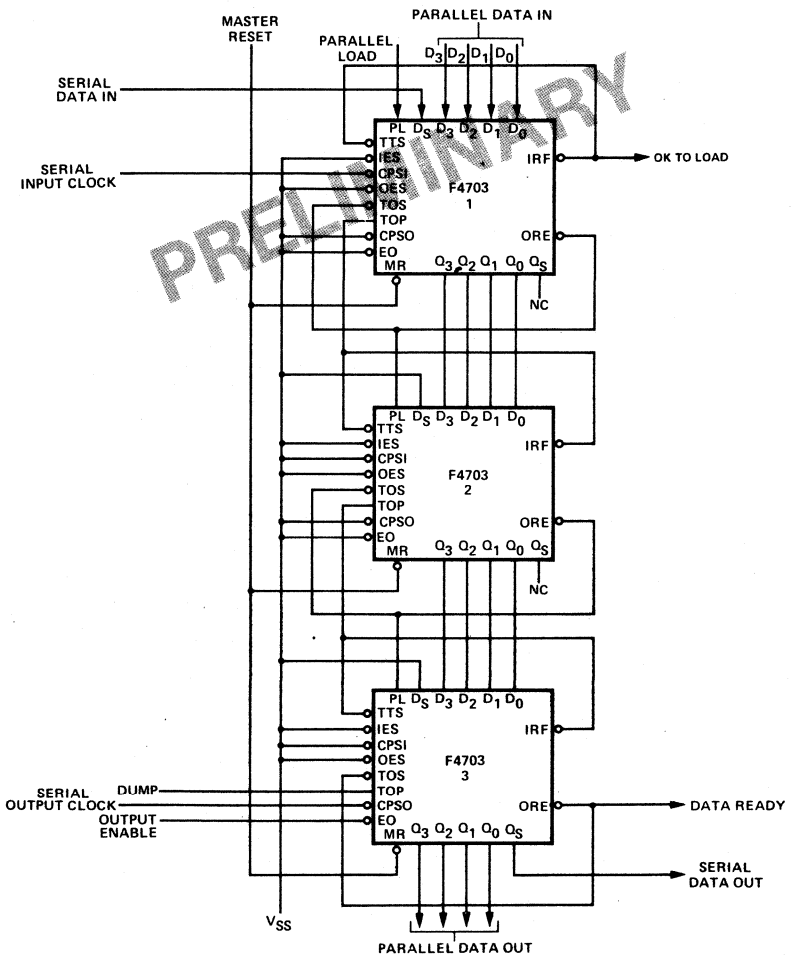


Fig. 4 A VERTICAL EXPANSION SCHEME FOR THE F4703

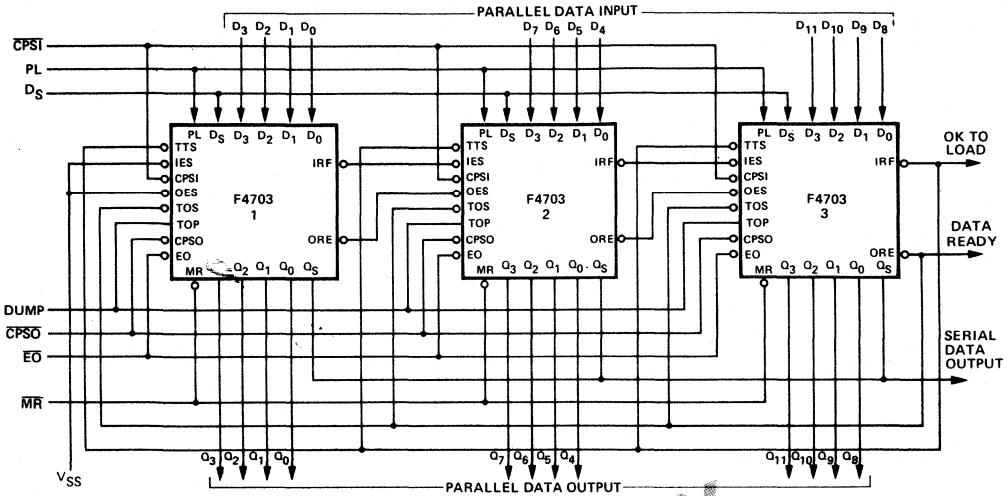


Fig. 5 A HORIZONTAL EXPANSION SCHEME FOR THE F4703

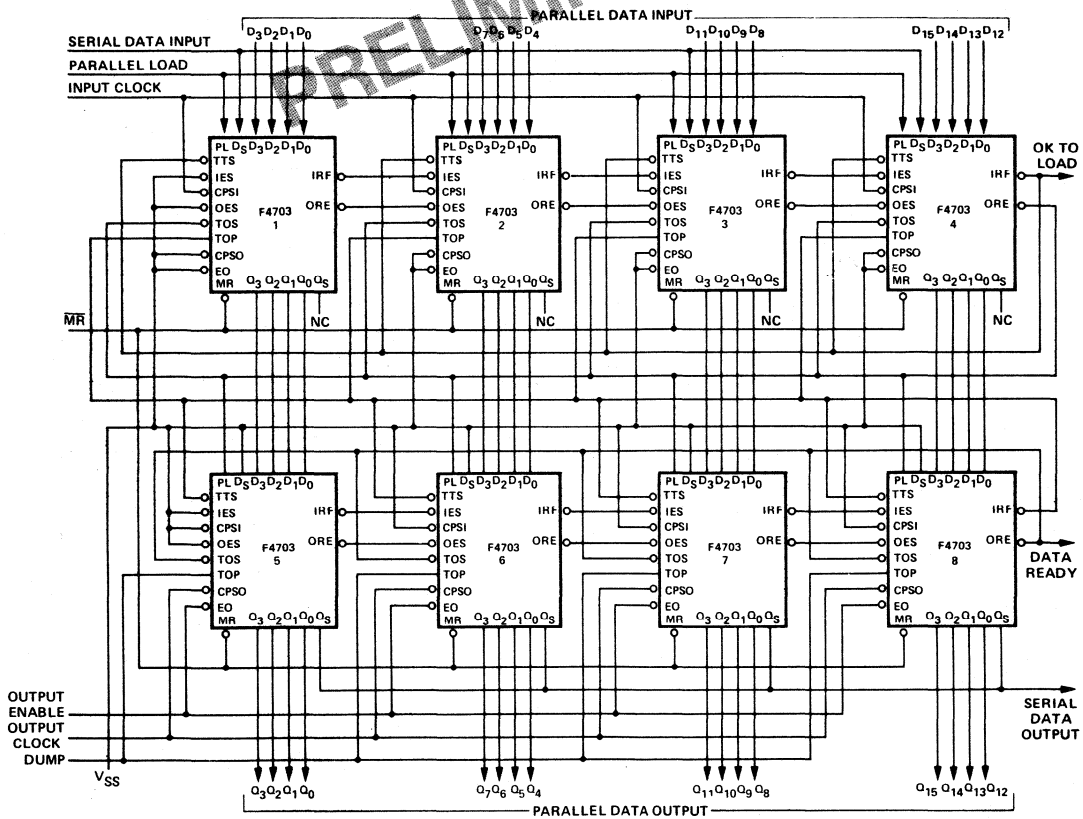


Fig. 6 A 31 X 16 FIFO ARRAY

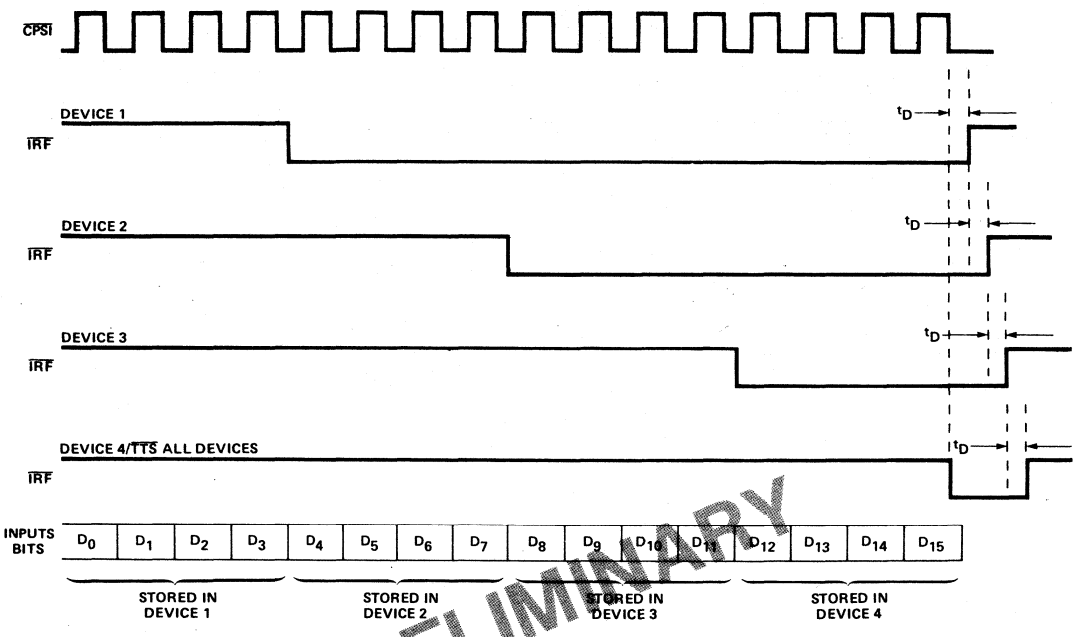


Fig. 7 SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

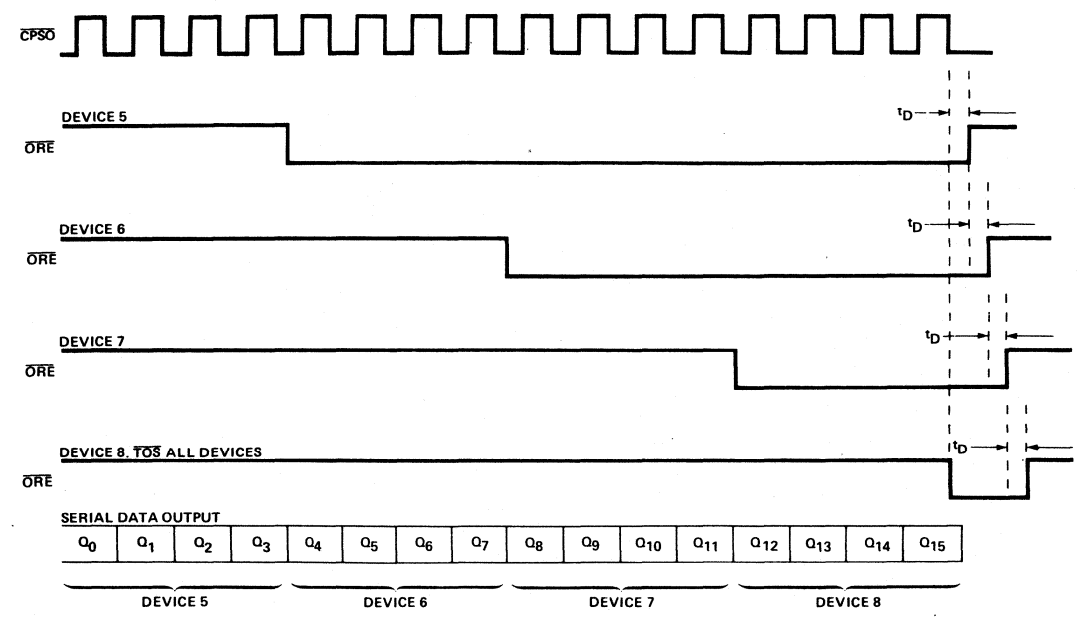


Fig. 8 SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

INTERLOCKING CIRCUITRY

Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$; however, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The F4703 incorporates simple but effective "Master-Slave" interlocking circuitry to eliminate the need for external gating.

In the F4703 array of Figure 6 Devices 1 and 5 are defined as "Row Masters" and the other devices are slaves to the Master in their row. No slave in a given row will initialize its input register until it has received a LOW on its $\overline{IES}$ input from a Row Master or a Slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ input has gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The Row Master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of F4703 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the Row Master receives a LOW on the $\overline{IES}$ input during initialization. Figure 10 is a conceptual logic diagram of the internal circuitry which determines Master-Slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization flip-flop will be set. If the Master latch is HIGH, the input register will be immediately initialized and the Request Initialization flip-flop reset. If the Master latch is reset, the input register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the Row Master to the last Slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ Request flip-flop. If the Master latch is set, the last output register flip-flop is set, and $\overline{ORE}$ goes HIGH. If the Master latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

Table 1 summarizes Master-Slave status outputs.

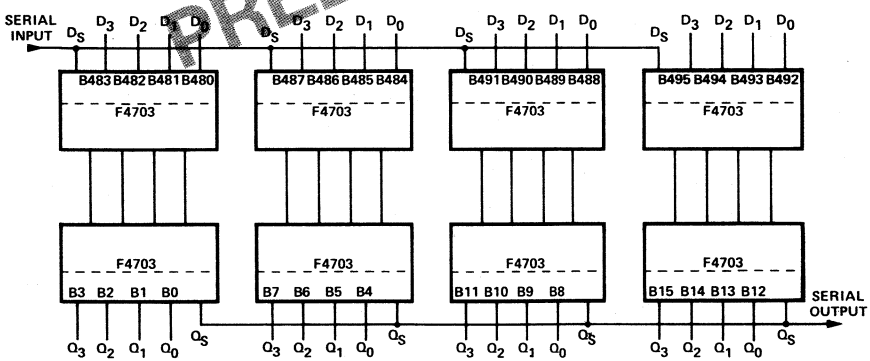


Fig. 9 FINAL POSITION OF A 496-BIT SERIAL INPUT

TABLE 1

OUTPUT CONDITION	INTERNAL STATE	
	Master Operation — $\overline{IES}$ LOW when initialized	Slave Operation — $\overline{IES}$ HIGH when initialized
$\overline{IRF}$ LOW	Input Register Full	Input Register Full and $\overline{IES}$ LOW
$\overline{ORE}$ LOW	Output Register not full	Output Register not full & $\overline{OES}$ LOW

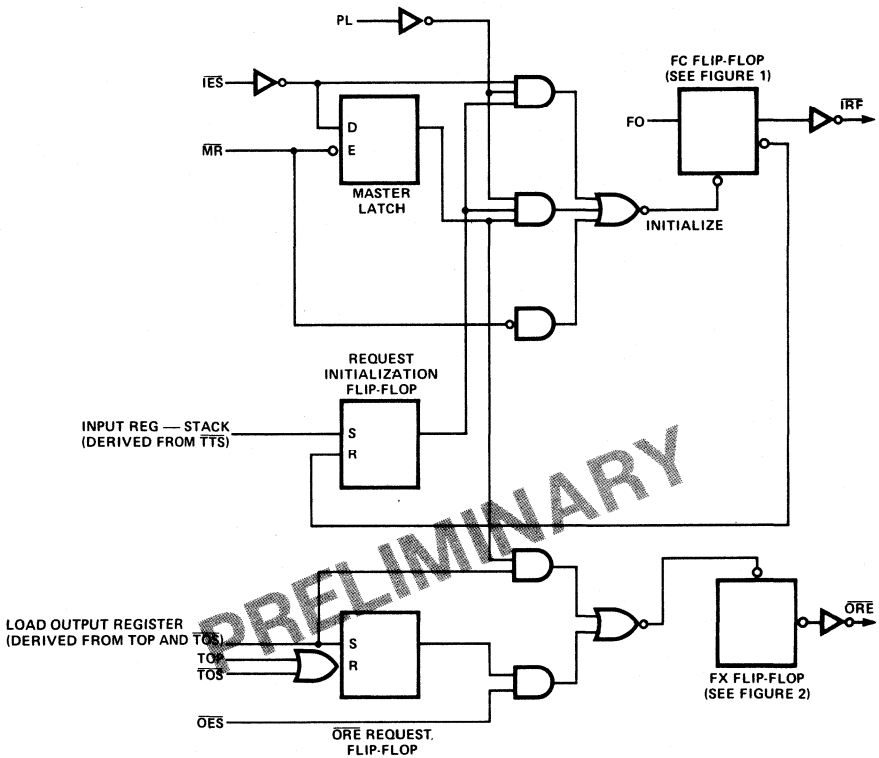


Fig. 10 CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC										μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
													MAX	
		XM										μA	MIN, 25°C	
													MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PHL}	Propagation Delay, $\overline{CPSI}$ to $\overline{IRF}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH}	Propagation Delay, $\overline{TTS}$ to $\overline{IRF}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CPSO}$ to Q_S										ns	
t_{PLH} t_{PHL}	Propagation Delay, TOP to Q_n										ns	
t_{PHL}	Propagation Delay, $\overline{CPSO}$ to $\overline{ORE}$										ns	
t_{PLH}	Propagation Delay, $\overline{TOS}$ to $\overline{ORE}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{TOP}$ to $\overline{ORE}$										ns	
t_{PHL}	Propagation Delay, PL to $\overline{IRF}$										ns	
t_{FT}	Fall Through Time										ns	
t_{PZH} t_{PZL}	Output Enable Time										ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time										ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time										ns	
t_{PHL}	Propagation Delay, $\overline{CPSI}$ to $\overline{IRF}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH}	Propagation Delay, $\overline{TTS}$ to $\overline{IRF}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CPSO}$ to Q_S										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{TOP}$ to Q_n										ns	
t_{PHL}	Propagation Delay, $\overline{CPSO}$ to $\overline{ORE}$										ns	
t_{PLH}	Propagation Delay, $\overline{TOS}$ to $\overline{ORE}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, TOP to $\overline{ORE}$										ns	
t_{PHL}	Propagation Delay, PL to $\overline{IRF}$										ns	
t_{FT}	Fall Through Time										ns	

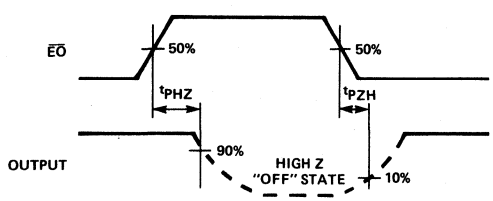
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (Cont'd)

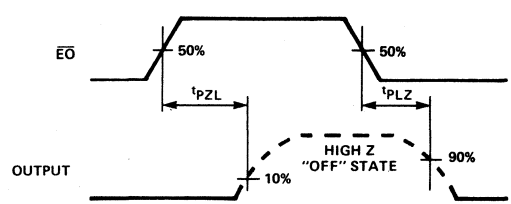
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PZH} t_{PZL}	Output Enable Time										ns	(R_L = 1-kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time										ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time										ns	
$t_W\overline{CP}(H)$	Min $\overline{CPSI}$ Pulse Width (HIGH)										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
$t_W\overline{CP}(L)$	Min $\overline{CPSI}$ Pulse Width (LOW)										ns	
$t_W\overline{CP}(L)$	Min $\overline{CPSO}$ Pulse Width (LOW)										ns	
$t_W\overline{CP}(H)$	Min $\overline{CPSO}$ Pulse Width (HIGH)										ns	
$t_WPL(H)$	Min PL Pulse Width (HIGH)										ns	
$t_W\overline{TTS}(L)$	Min $\overline{TTS}$ Pulse Width (LOW)										ns	
$t_WTOS(L)$	Min. TOS Pulse width (LOW)										ns	
$t_WTOP(L)$	Min TOP Pulse Width (LOW)										ns	
$t_W\overline{MR}(L)$	Min $\overline{MR}$ Pulse Width (LOW)										ns	
t_{rec}	$\overline{MR}$ Recovery Time										ns	
t_s, t_h	Set-up and Hold Times, D_s to $\overline{CPSI}$										ns	
t_s, t_h	Set-up and Hold Times, $\overline{TTS}$ to $\overline{IRF}$ IRF, Serial or Parallel Mode										ns	
t_s	Set-Up Time, $\overline{ORE}$ to $\overline{TOS}$										ns	
f_{MAX}	Input CLOCK Frequency (Note 4)										MHz	

SWITCHING WAVEFORMS

OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})

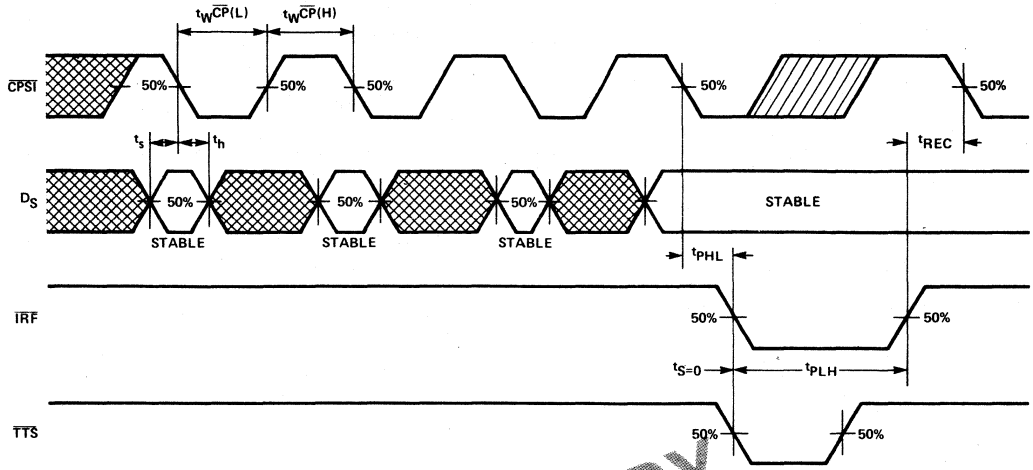


OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



SWITCHING WAVEFORMS (Cont'd)

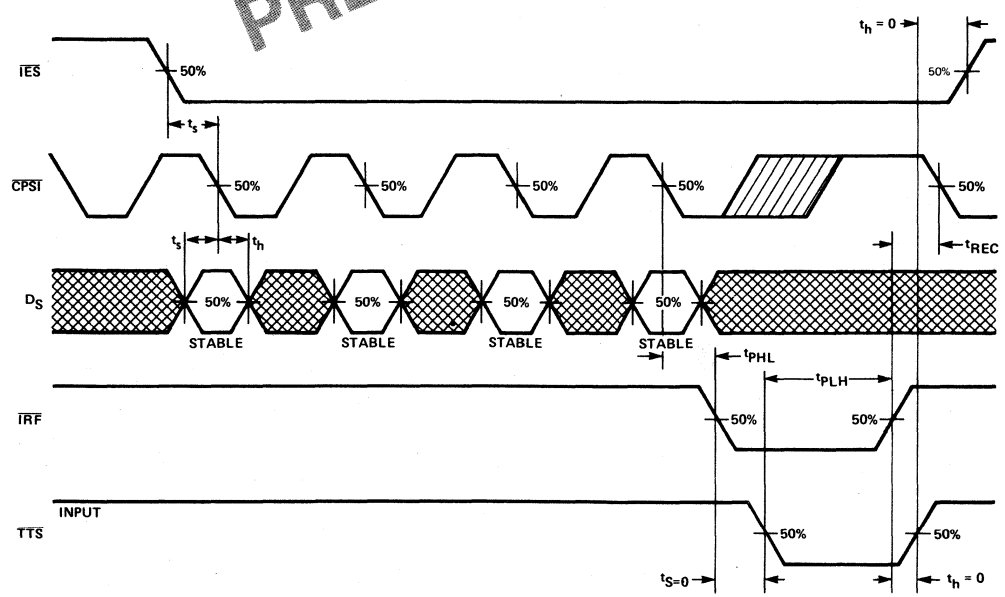
SERIAL INPUT UNEXPANDED OR MASTER OPERATION



MINIMUM $\overline{CPSI}$ PULSE WIDTH, PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$ RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$, AND SET-UP AND HOLD TIMES, D_S TO $\overline{CPSI}$, AND $\overline{TTS}$ TO $\overline{IRF}$.

CONDITIONS: STACK NOT FULL, $\overline{IES}$, = PL = LOW

SERIAL INPUT EXPANDED SLAVE OPERATION



PROPAGATION DELAY, $\overline{CPSI}$ TO $\overline{IRF}$ AND $\overline{TTS}$ TO $\overline{IRF}$, RECOVERY TIME, $\overline{IRF}$ TO $\overline{CPSI}$ AND SET-UP AND HOLD TIMES, $\overline{IES}$ TO $\overline{CPSI}$, D_S TO $\overline{CPSI}$ AND $\overline{TTS}$ TO $\overline{IRF}$.

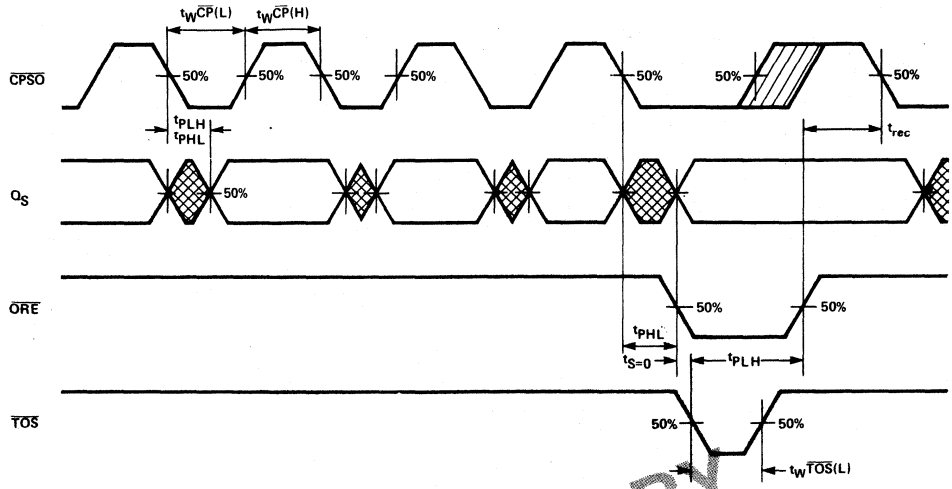
CONDITIONS: STACK NOT FULL $\overline{IES}$ = HIGH
WHEN INITIALIZED, PL = LOW

NOTE:
Set-up and hold times are shown as positive values but may be specified as negative values.

4

SWITCHING WAVEFORMS (Cont'd)

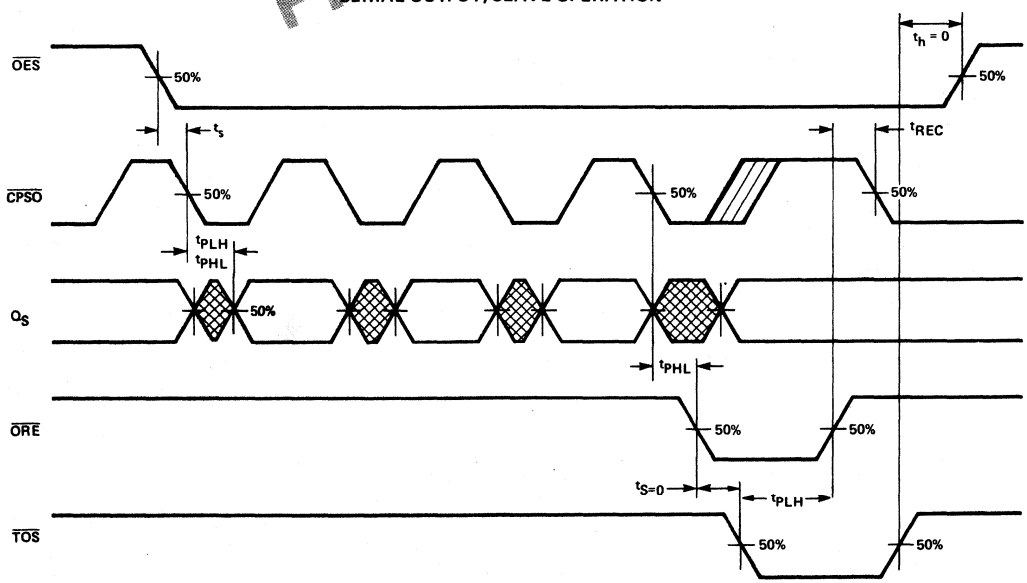
SERIAL OUTPUT, UNEXPANDED OR MASTER OPERATION



$\overline{ORE}$ RECOVERY TIME, PROPAGATION DELAY $\overline{CPSO}$ TO Q_S, $\overline{CPSO}$ TO $\overline{ORE}$, $\overline{TOS}$ TO $\overline{ORE}$, MINIMUM $\overline{CPSO}$ PULSE WIDTH, MINIMUM $\overline{TOS}$ PULSE WIDTH AND SET-UP TIME $\overline{ORE}$ TO $\overline{TOS}$.

CONDITIONS: DATA IN STACK, $\overline{TOP}$ = HIGH, $\overline{IES}$ = LOW WHEN INITIALIZED, $\overline{OES}$ = LOW

SERIAL OUTPUT, SLAVE OPERATION



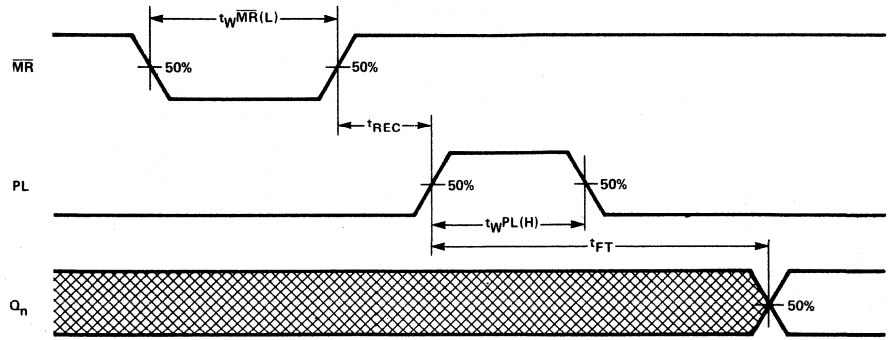
$\overline{ORE}$ RECOVERY TIME, PROPAGATION DELAY $\overline{CPSO}$ TO Q_S, $\overline{CPSO}$ TO $\overline{ORE}$, $\overline{TOS}$ TO $\overline{ORE}$, AND SET-UP AND HOLD TIMES, $\overline{OES}$ TO $\overline{CPSO}$, $\overline{ORE}$ TO $\overline{TOS}$, $\overline{TOS}$ TO $\overline{OES}$

CONDITIONS: DATA IN STACK, TOP = HIGH, $\overline{IES}$ = HIGH WHEN INITIALIZED

NOTE:
Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS (Cont'd)

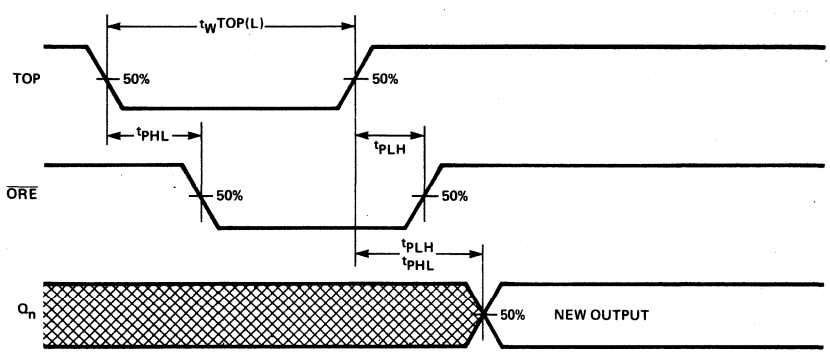
FALL THROUGH TIME



MINIMUM $\overline{MR}$ AND PL PULSE WIDTHS, RECOVERY TIME FOR $\overline{MR}$ AND FALL THROUGH TIME

CONDITIONS: $\overline{TTS}$ CONNECTED TO $\overline{IRF}$, $\overline{TOS}$ CONNECTED TO $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{EO}$, $\overline{CPSO}$ = LOW, TOP = HIGH

PARALLEL OUTPUT, FOUR BIT WORD OR MASTER IN PARALLEL EXPANSION

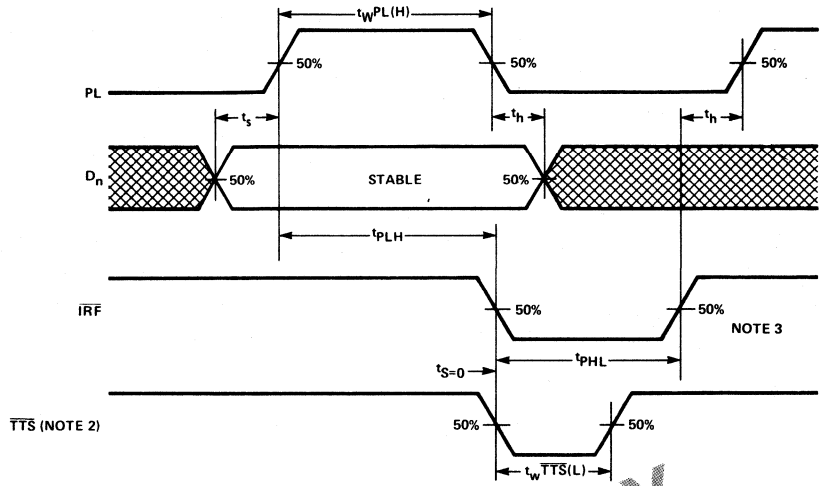


PROPAGATION DELAY, TOP TO $\overline{ORE}$, TOP TO Q_n, AND MINIMUM TOP PULSE WIDTH

CONDITIONS: $\overline{IES}$ = LOW WHEN INITIALIZED, $\overline{EO}$ = $\overline{CPSO}$ = LOW. DATA AVAILABLE IN STACK

SWITCHING WAVEFORMS (Cont'd)

PARALLEL LOAD MODE, FOUR BIT WORD (UNEXPANDED) OR MASTER IN PARALLEL EXPANSION

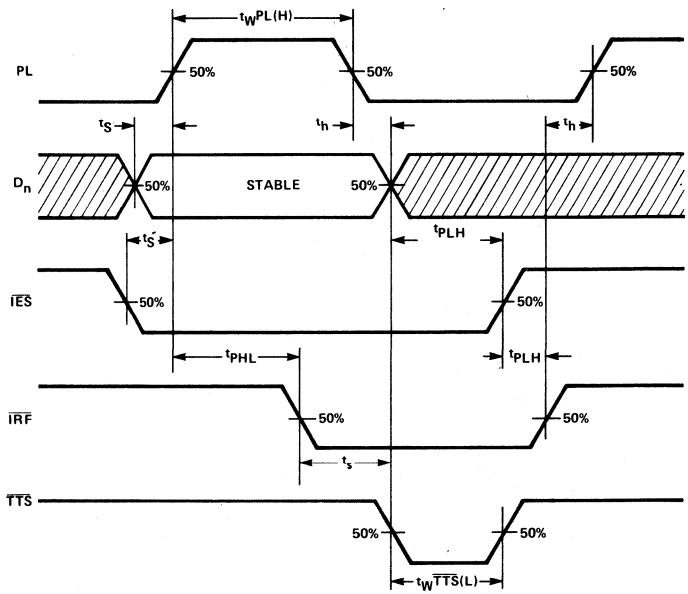


PROPAGATION DELAY PL TO $\overline{IRF}$, $\overline{TTS}$ TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES D_n TO PL, $\overline{IRF}$ TO PL, $\overline{TTS}$ TO $\overline{IRF}$

CONDITIONS: STACK NOT FULL, $\overline{IES}$ = LOW WHEN INITIALIZED

NOTES:
1. Initialization requires a master reset to occur after power has been applied.
2. $\overline{TTS}$ normally connected to $\overline{IRF}$.
3. If stack is full, $\overline{IRF}$ will stay LOW.

PARALLEL LOAD, SLAVE MODE



PROPAGATION DELAY, $\overline{TTS}$ TO $\overline{IES}$, $\overline{IES}$ TO $\overline{IRF}$, PL TO $\overline{IRF}$, MINIMUM PL AND $\overline{TTS}$ PULSE WIDTHS, AND SET-UP AND HOLD TIMES, D_n TO PL, $\overline{IRF}$ TO $\overline{TTS}$, $\overline{IRF}$ TO PL

CONDITIONS: STACK NOT FULL, DEVICE INITIALIZED (NOTE 1) WITH $\overline{IES}$ HIGH

NOTE:
Set-up (t_s) and hold times (t_h) are shown as positive values but may be specified as negative values.

F4704/34704

DATA PATH SWITCH

FAIRCHILD MACROLOGIC™ CMOS

DESCRIPTION – The F4704 Data Path Switch (DPS) is a combinatorial array for closing data path loops around arithmetic/logic networks such as the F4705 (Arithmetic Logic Register Stack). A total of 32 instructions (see Table 1) facilitate logic shifting, byte swapping, masking, sign extension, introduction of common constants and other operations.

The 5-bit Instruction word (I_0-I_4) selects one of the 32 instructions operating on two sets of 4-bit Data Inputs ($\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$). Shift Left Input ($\overline{LI}$) and Output ($\overline{LO}$) and Shift Right Input ($\overline{RI}$) and Output ($\overline{RO}$) are available for expansion in 4-bit increments. An active LOW Output Enable Input ($\overline{EO}$) provides for 3-state control of the Data Outputs ($\overline{O}_0$-$\overline{O}_3$) for bus oriented applications.

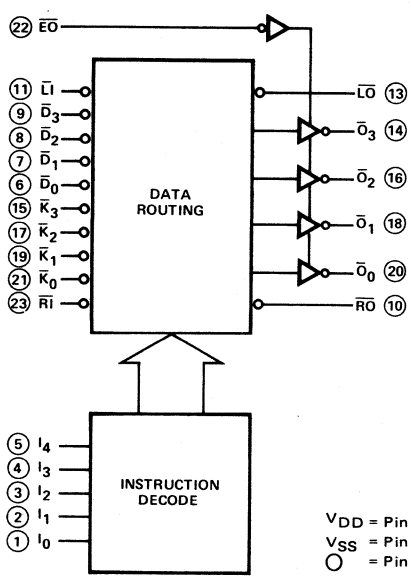
The F4704 is packaged in the new slim 24-pin Dual In-line package.

- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **TWO 4-BIT DATA INPUT BUSES**
- **4-BIT DATA OUTPUT BUS WITH 3-STATE OUTPUT BUFFERS**
- **USEFUL FOR BYTE MASKING AND SWAPPING**
- **PROVIDES ARITHMETIC OR LOGIC SHIFT**
- **PROVIDES FOR SIGN EXTENSION**
- **GENERATES COMMONLY USED CONSTANTS**
- **NEW SLIM 24-PIN DIP**

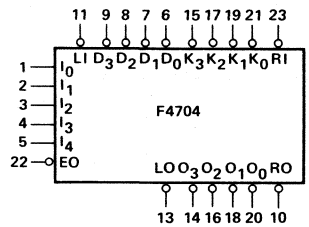
PIN NAMES

$\overline{D}_0$-$\overline{D}_3$, $\overline{K}_0$-$\overline{K}_3$	Data Inputs (Active LOW)
I_0-I_4	Instruction Word Input
$\overline{LI}$	Shift Left Input (Active LOW)
$\overline{LO}$	Shift Left Output (Active LOW)
$\overline{RI}$	Shift Right Input (Active LOW)
$\overline{RO}$	Shift Right Output (Active LOW)
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Data Output (Active LOW)

BLOCK DIAGRAM

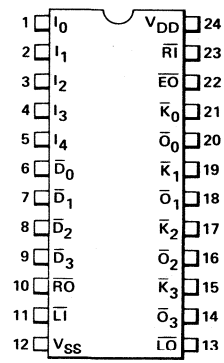


LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

TABLE 1
INSTRUCTION SET FOR THE F4704

INPUTS					OUTPUTS				FUNCTION	INPUTS					OUTPUTS						FUNCTION
I_4	I_3	I_2	I_1	I_0	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$		I_4	I_3	I_2	I_1	I_0	$\overline{LO}$	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$	$\overline{RO}$	
L	L	L	L	L	L	L	L	L	Byte Mask	H	L	L	L	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		K-Bus Sign Extend
L	L	L	L	H	H	H	H	H	Byte Mask	H	L	L	L	H	$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		K-Bus Sign Extend
L	L	L	H	L	L	L	L	H	Minus "2" in 2s Comp[1]	H	L	L	H	L	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$	$\overline{RI}$		D-Bus Sign Extend
L	L	L	H	H	L	L	L	L	Minus "1" in 2s Comp[1]	H	L	L	H	H	$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$		D-Bus Sign Extend
L	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	$\overline{RI}$		D-Bus Shift Left
L	L	H	L	H	H	H	H	H	Byte Mask D-Bus	H	L	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	$\overline{RI}$		K-Bus Shift Left
L	L	H	H	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Byte Mask D-Bus	H	L	H	H	L		$\overline{LI}$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right
L	L	H	H	H	L	L	L	L	Byte Mask D-Bus	H	L	H	H	H		$\overline{D}_3$	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	D-Bus Shift Right Arith[2]
L	H	L	L	L	L	H	H	H	Negative Byte Sign Mask	H	H	L	L	L		$\overline{LI}$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right
L	H	L	L	H	H	H	H	H	Positive Byte Sign Mask	H	H	L	L	H		$\overline{K}_3$	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	K-Bus Shift Right Arith[2]
L	H	L	H	L	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Byte Mask K-Bus	H	H	L	H	L		$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$		Byte Mask K-Bus
L	H	L	H	H	L	L	L	L	Byte Mask K-Bus	H	H	L	H	H		H	H	H	H		Byte Mask K-Bus
L	H	H	L	L	$\overline{D}_3$	$\overline{D}_2$	$\overline{D}_1$	$\overline{D}_0$	Load Byte	H	H	H	L	L		D_3	D_2	D_1	D_0		Complement D-Bus
L	H	H	L	H	$\overline{K}_3$	$\overline{K}_2$	$\overline{K}_1$	$\overline{K}_0$	Load Byte	H	H	H	L	H		K_3	K_2	K_1	K_0		Complement K-Bus
L	H	H	H	L	H	H	H	L	Plus "1"	H	H	H	H	L							Undefined
L	H	H	H	H	H	H	H	H	Zero	H	H	H	H	H							Undefined

H = HIGH Level
L = LOW Level

(1) Comp = Complement
(2) Arith = Arithmetic

FUNCTIONAL DESCRIPTION

The F4704 Data Path Switch combines the functions of a dual four-input multiplexer, a true/complement one/zero generator, and a shift left/shift right array.

As shown in Table 1, there are two shift right modes. The arithmetic right shift preserves the sign bit in the most significant position while the logic shift moves all positions. Right shift is defined as a one-bit shift toward the least significant position.

For half word arithmetic the F4704 provides instructions which extend the sign bit left through the more significant slices. Shift linkages are available as individual inputs and outputs for complete flexibility.

The F4704 may be used to generate constants +1, 0, –1 and –2 in two's complement notation.

ARRAYS

Arrays of larger than 4-bit word lengths are easily obtained. Figure 1 illustrates a 16-bit array constructed using 4 devices; device 1 is the least significant and device 4 is the most significant slice. Within each slice, inputs and outputs with '0' subscript are the least significant bits.

The I_1 through I_4 inputs of all devices are bussed. These four bus lines together with the I_0 inputs of the devices form an 8-bit instruction bus to control the array. In some applications, it may be possible to connect the I_0 inputs of devices 1 & 2 together and the I_0 inputs of devices 3 & 4 together, so that only 6 bits are needed to control the arrays. Connecting the $\overline{LO}$ of device 1 to $\overline{RI}$ of device 2, $\overline{LO}$ of device 2 to $\overline{RI}$ of device 3, etc. provides left shift (i.e., shift towards most significant bit) and sign extension. From Table 1 it can be seen that "sign extend" consists of two adjacent instructions differing only in I_0; one of these instructions connects the most significant bit of the selected input bus (i.e., $\overline{D}_3$ or $\overline{K}_3$) to the $\overline{LO}$ output while the other instruction forces the output bus and $\overline{LO}$ to the $\overline{RI}$ input. In a similar fashion right shift operation is accomplished by connecting the $\overline{LI}$ input of a device to the $\overline{RO}$ of the next more significant device.

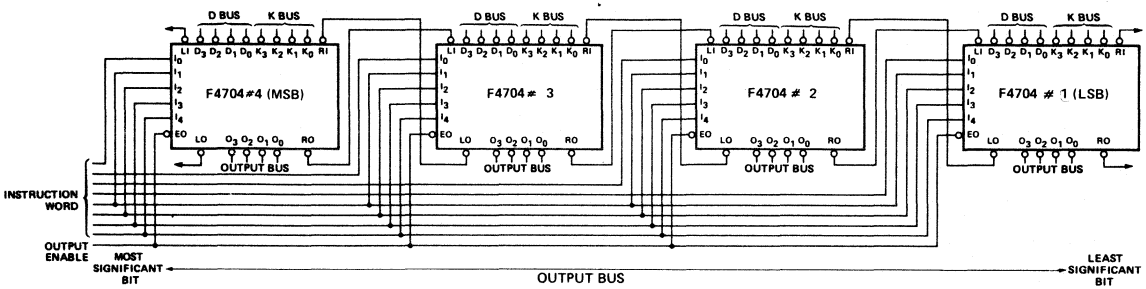


Fig. 1 16-BIT F4707 ARRAY

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC										μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
													MAX	
		XM										μA	MIN, 25°C	
													MAX	

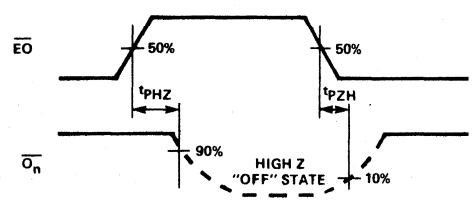
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

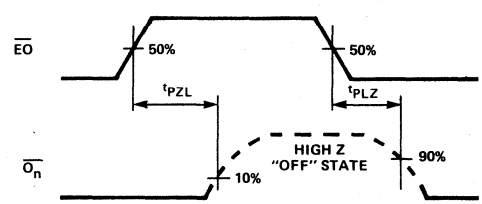
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D_n}$, $\overline{K_n}$ to $\overline{O_n}$		100 100								ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D_n}$, $\overline{K_n}$ to $\overline{L_O}$, $\overline{R_O}$		100 100								ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{R_I}$ to $\overline{L_O}$		50 50								ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{L_I}$ to $\overline{R_O}$		50 50								ns	
t_{PLH} t_{PHL}	Propagation Delay, I_n to $\overline{Q_n}$		100 100								ns	
t_{PLH} t_{PHL}	Propagation Delay, I_n to $\overline{R_O}$, $\overline{L_O}$		100 100								ns	
t_{PZH} t_{PZL}	Output Enable Time		30 30								ns	(R$_L$ = 1 kΩ to V_{SS}) (R$_L$ = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time		30 30								ns	
t_{TLH} t_{THL}	Output Transition Time		45 45								ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D_n}$, $\overline{K_n}$ to $\overline{O_n}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D_n}$, $\overline{K_n}$ to $\overline{L_O}$, $\overline{R_O}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{R_I}$ to $\overline{L_O}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{L_I}$ to $\overline{R_O}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, I_n to O_n										ns	
t_{PLH} t_{PHL}	Propagation Delay, I_n to $\overline{R_O}$, $\overline{L_O}$										ns	
t_{PZH} t_{PZL}	Output Enable Time										ns	(R$_L$ = 1 kΩ to V_{SS}) (R$_L$ = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time										ns	
t_{TLH} t_{THL}	Output Transition Time										ns	

NOTE:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

F4705/34705

ARITHMETIC LOGIC REGISTER STACK

FAIRCHILD MACROLOGIC™ CMOS

DESCRIPTION – The Arithmetic Logic Register Stack (ALRS) is designed to implement general registers in programmable digital systems. The device contains a 4-bit arithmetic logic unit (ALU), an 8-word by 4-bit RAM and associated control logic. The ALU implements eight arithmetic and logic functions where one 4-bit operand is supplied from an external source (input data bus) and the second 4-bit operand is supplied internally from one of the eight RAM words selected by the Address Inputs (A_0–A_2). The result of the operation performed on the operands is loaded into the same RAM location and simultaneously loaded into the output register, making it available at the 3-state output data bus.

The F4705 operates on four bits of data but features are provided for expansion to longer word lengths. Carry Propagate and Carry Generate outputs are provided for an external carry lookahead where maximum operating speed is required. In applications where high speed arithmetic is not needed, ripple expansion may also be implemented. The F4705 provides three status signals – Zero, Negative and Overflow – to qualify the result of an operation.

The F4705 is a member of Fairchild's F4000 CMOS Macrologic family and is available in the new slim 24-pin Dual In-line package.

- **EIGHT GENERAL REGISTERS/ACCUMULATORS IN A SINGLE PACKAGE**
- **2 MHz MICROINSTUCTION RATE**
- **VERY LOW POWER – IDEAL FOR BATTERY OPERATION**
- **EXPANDABLE IN MULTIPLES OF FOUR BITS**
- **PROVIDES FOR RIPPLE OR CARRY LOOKAHEAD**
- **IMPLEMENTS 64 MICROINSTRUCTIONS**
- **PROVIDES THREE STATUS SIGNALS – ZERO, NEGATIVE AND OVERFLOW**
- **3-STATE OUTPUTS**
- **NEW SLIM 24-PIN DIP**

PIN NAMES

$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)
A_0-A_2	Address Instruction Inputs
I_0-I_2	ALU Instruction Inputs (Note a)
MSS	Most Significant Slice Input
CP	Clock Input
$\overline{EO}$	Output Enable Input (Active LOW)
$\overline{EX}$	Execute Input (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Data Outputs (Active LOW)
$\overline{W}$	Ripple Carry Output Active LOW, Note b)
$\overline{X}$	Carry Propagate Output (Active LOW, Note c)
$\overline{Y}$	Carry Generate Output (Active LOW, Note d)
Z	Zero Status Output (Active HIGH, Open Drain, Note e)

NOTES:
a. I_0 is also used for Carry Input on lesser significant slices.
b. $\overline{W}$ output also carries instruction information.
c. $\overline{X}$ output provides negative status on most significant slice.
d. $\overline{Y}$ output provides overflow status on most significant slice.
e. An external pull-up resistor is required to supply HIGH level output drive.

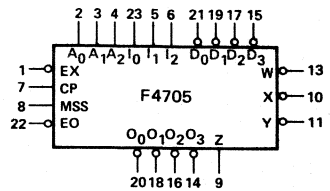
TABLE 1 INSTRUCTION FIELD ASSIGNMENT

I_2	I_1	I_0	INTERNAL OPERATION	FUNCTION
L	L	L	Rx plus D-Bus plus 1 → Rx	Accumulate
L	L	H	Rx plus D-Bus → Rx	Accumulate
L	H	L	Rx · D-Bus → Rx	Logic AND
L	H	H	D-Bus → Rx	
H	L	L	Rx → R_X + Output Register	Load Output
H	L	H	Rx + D-Bus → Rx	Logic OR
H	H	L	Rx ⊕ D-Bus → Rx	Exclusive OR
H	H	H	$\overline{\text{D-Bus}}$ → Rx	Load Complement

H = Logic HIGH Level L = Logic LOW Level

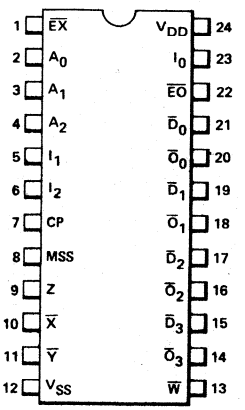
NOTES:
1. Rx is the RAM location addressed by A_0–A_2.
2. The result of any operation is always loaded into the Output Register.

LOGIC SYMBOL



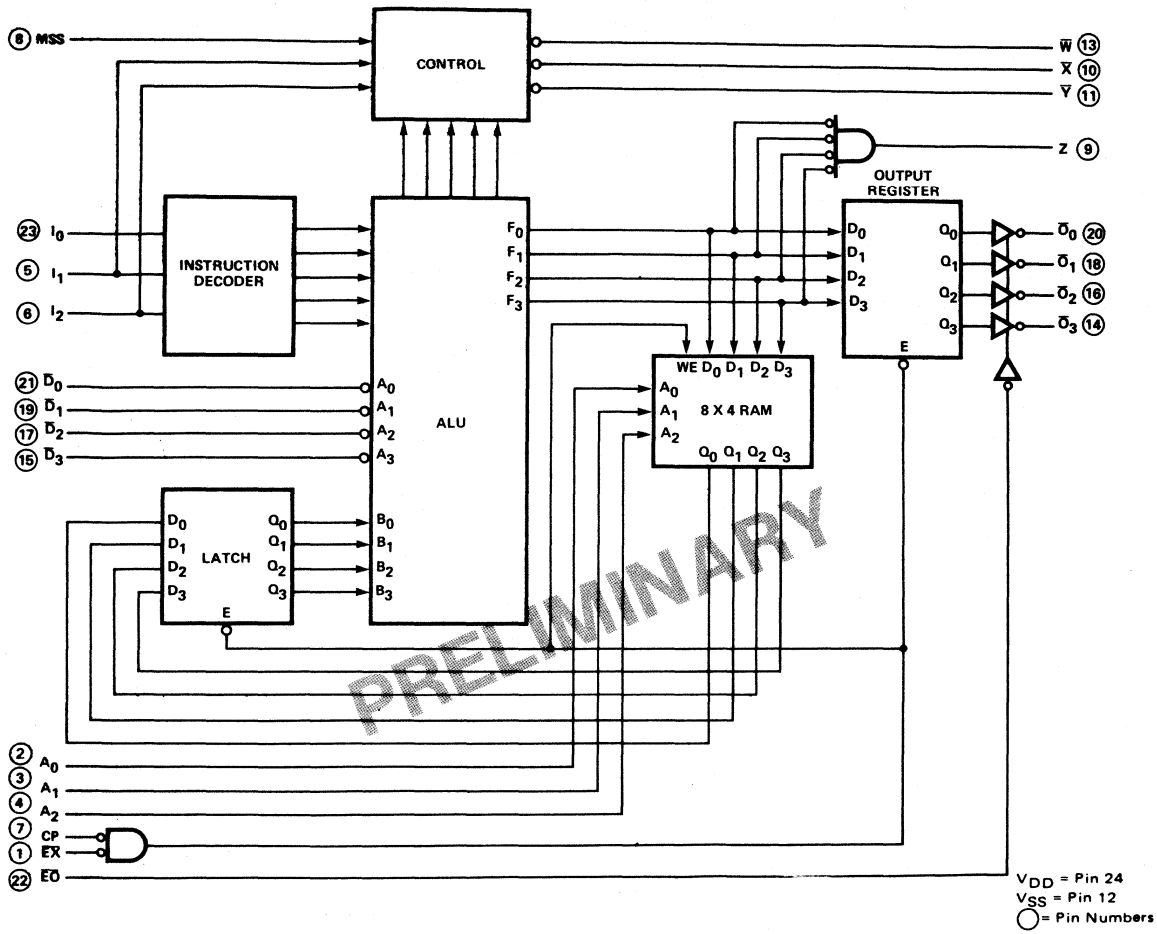
V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – As shown in the Block Diagram, the F4705 Arithmetic Logic Register Stack (ALRS) consists of a 4-bit ALU, an 8-word by 4-bit RAM with output latches, an instruction decode network, control logic, and a 4-bit output register.

The ALU receives the active LOW input data ($\overline{D}_0$–$\overline{D}_3$) as one operand while the RAM provides the second operand through latches. The ALU output is stored in both the RAM and output register. The active LOW output data bus ($\overline{O}_0$–$\overline{O}_3$) is obtained from the output register through 3-state buffers. An active LOW Output Enable ($\overline{EO}$) input controls these buffers; a HIGH level on $\overline{EO}$ disables them (high impedance state).

The instruction bus for the F4705 consists of two fields, A and I; A_0, A_1, A_2 specify the desired location on the RAM and I_0, I_1, I_2 specify the desired function to be performed. Table 1 lists Instruction Field Code assignments. Thus, the F4705 provides eight registers (R_0–R_7) and eight different operations may be performed on any of these registers. The I_0, I_1, I_2 inputs are decoded by the instruction decode network to generate necessary control signals for the ALU. The ALU also generates and transmits to the control logic the following signals: carry out, carry propagate, carry generate, negative status and overflow status. The control logic manipulates the status signals as a function of I_0, I_1, I_2 and a control input MSS. A HIGH level on the MSS (Most Significant Slice Input) declares the most significant slice in a F4705 array. All devices, except the most significant F4705 should have a LOW level (ground) on the MSS input. The control logic generates three device outputs, $\overline{W}$, $\overline{X}$ and $\overline{Y}$ for arrayed operation of F4705 arrays. An all zero result from the ALU is decoded and presented at the open drain Zero Status (Z) Output.

The I_0 input serves a dual purpose: for arithmetic instructions, it is used as the carry input and for non-arithmetic instructions it serves as an instruction input. This is possible because only two arithmetic instructions require carry. The dual purpose use of I_0 plays an important role in F4705 expansion schemes.

OPERATION – The F4705 operates on a single clock. CP and $\overline{EX}$ are inputs to a 2-input active LOW AND gate. A microcycle starts as the clock goes HIGH. For normal operation the Execute ($\overline{EX}$) is LOW. Data is read from the RAM through enabled latches and applied as one operand to the ALU. Data inputs ($\overline{D}_0$–$\overline{D}_3$) are applied to the ALU as the other operand and the operation as determined by instruction lines I_0, I_1, I_2 is executed. When CP is LOW, the latches are disabled and the result of the operation is written back into the RAM provided that $\overline{EX}$ is LOW. Then A lines must obviously be held stable during this time. On the LOW-to-HIGH CP transition, the result of the operation is loaded into the output register and a new microcycle can start. If $\overline{EX}$ is held HIGH, the operation selected by the I and A inputs is performed, but the result is not written back into the RAM and is not clocked into the output register.

F4705 ARRAYS

The F4705 is organized to operate on a 4-bit wide data bus but can easily be expanded for longer words. Expansion requires that carries from lesser significant slices be propagated towards the most significant slice. The F4705 provides full lookahead capability for high speed arithmetic. Appropriate Carry Generate ($\overline{Y}$) and Carry Propagate ($\overline{X}$) outputs are provided so that only one external carry lookahead generator is needed for every four F4705s. When speed is not a prime consideration, it is possible to implement ripple carry expansion.

In arrayed operation, it is common to bus $\overline{EX}$, CP and $\overline{EO}$ inputs of all devices. The Z output is open drain and is normally OR-tied with the other devices and to an external load resistor so that a HIGH level indicates a zero result from an operation in the array.

Figure 1 shows a ripple carry 16-bit wide array using four F4705s. The MSS input is tied to V_{DD} on the most significant slice (ALRS 4). The MSS input of the other devices are tied to ground (V_{SS}). The instruction bus of this array consists of A-Field and I-Field. A-Field is obtained by connecting corresponding A inputs of all 4 devices. The I_0 input of device 1 (i.e., least significant slice) in conjunction with the bussed I_1, I_2 inputs forms the I-Field for the array. The I_0 inputs of devices 2, 3 and 4 are connected to the $\overline{W}$ outputs of devices 1, 2 and 3 respectively. The ALU network generates the carry propagate output. The control logic operates on this signal as a function of I_1 and I_2 to generate the $\overline{W}$ output. If both I_1 and I_2 are LOW (i.e., an arithmetic instruction), the $\overline{W}$ output is the carry output of that slice. In case of non-arithmetic instructions, it will assume the state of the I_0 input. Thus, in Figure 1, if an arithmetic instruction is specified, carry will propagate through the $\overline{W}$ output to I_0 input of the next higher significant slice. On the other hand, non-arithmetic instructions will effectively connect all I_0 inputs together to form the I-Field for the array. The $\overline{W}$ output of device 4 is the carry output from the array. The control logic also generates $\overline{X}$ and $\overline{Y}$ outputs which participate in expansion when full carry lookahead is required. These outputs are normally ignored in ripple expansion except for the most significant slice. If a device is the most significant slice, $\overline{X}$ and $\overline{Y}$ correspond to negative and overflow status signals. Thus $\overline{X}$ output of Device 4 will be LOW, if the result of an operation has its most significant bit as "1" (i.e., negative result). Similarly a LOW level on $\overline{Y}$ output of device 4 indicates that arithmetic overflow has occurred. If the two operands have the same sign and the result has the opposite sign. then it is assumed that an overflow has occurred. It should be noted that W, X and Y are not controlled by EX or CP. Figure 2 shows a 16-bit array with full carry lookahead expansion. Implementation of the lookahead scheme requires the use of an external F4582 in addition to the four F4705s in the array. Since device 1 is the least significant and device 4 is the most significant slice, the MSS inputs of the first three devices are connected to ground while device 4 has a HIGH level at this input. The A-Field for the array instruction bus is obtained by connecting corresponding A inputs of all four devices. Bussed I_1 and I_2 inputs together with the I_0 input of device 1 form the I-Field for the array. The I_0 inputs for devices 2, 3 and 4 are obtained from the F4582 carry outputs (Cn+x, Cn+y and Cn+z respectively). Also the P and G inputs of F4582 are connected to $\overline{X}$ and $\overline{Y}$ outputs of the F4705s as shown. The control logic in the F4705 (see Block Diagram) generates $\overline{X}$ and $\overline{Y}$ outputs as a function of I_1, I_2 and MSS inputs as well as the carry generate and carry propagate outputs of the ALU. If the MSS input of a slice is LOW and an arithmetic instruction is specified, its $\overline{X}$ output will reflect carry propagate and $\overline{Y}$ will reflect carry generate outputs from that slice. For an arithmetic instruction the I_0 input will be treated as carry-in into a slice irrespective of MSS. Thus, whenever I_1 and I_2 are LOW, the array behaves as an adder with full carry lookahead. The $\overline{W}$ outputs still reflect carry output, which is ignored for devices 1, 2 and 3. The $\overline{W}$ carry input to the array so the I_0 input of device 1 must be connected to the appropriate F4582 input as shown.

When a non-arithmetic instruction is specified to the array, the control logic of the F4705 forces a LOW level on $\overline{X}$ and a HIGH level on $\overline{Y}$ outputs on all except the most significant slice. An examination of the F4582 logic reveals that whenever P is LOW and G is HIGH, the associated carry output is the same as the carry input. Thus, in Figure 2, devices 2 3 and 4 will assume the logic level as that presented to the I_0 input of device 1 during non-arithmetic instructions effectively bussing I_0 through all four devices. As in the case of ripple expansion, $\overline{X}$ and $\overline{Y}$ outputs of device 4 represent negative and overflow from the array.

Fig. 1 16-BIT ALRS RIPPLE CARRY EXPANSION SCHEME

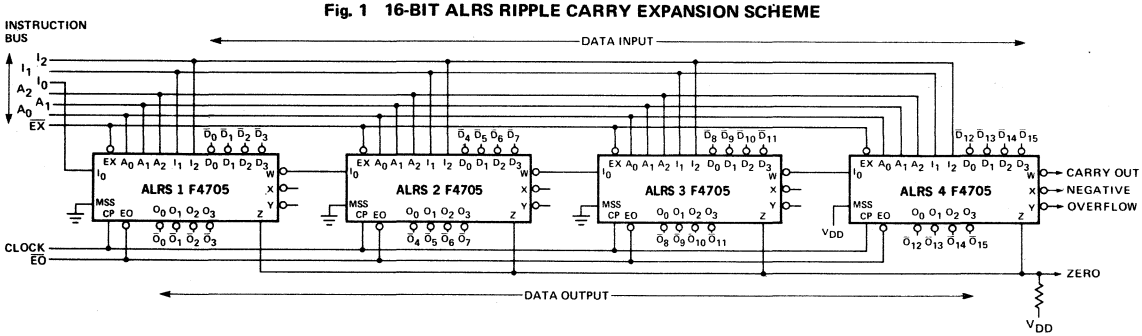
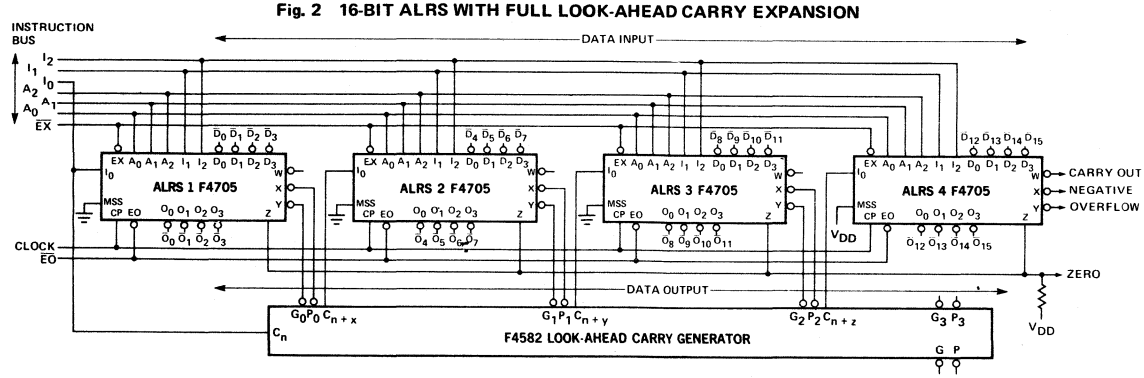


Fig. 2 16-BIT ALRS WITH FULL LOOK-AHEAD CARRY EXPANSION



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 3)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC										μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
													MAX	
		XM											MIN, 25°C	
													MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 4)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} / t_{PHL}	Propagation Delay, CP to $\overline{O_n}$		125 125								ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} / t_{PHL}	Propagation Delay, I_0 to $\overline{W}$		100								ns	
t_{PLH} / t_{PHL}	Propagation Delay, $\overline{D_n}$ to $\overline{W}$		150 150								ns	
t_{PLH} / t_{PHL}	Propagation Delay, $\overline{D_n}$ to $\overline{X}$, $\overline{Y}$		275 275								ns	
t_{PLH} / t_{PHL}	Propagation Delay, $\overline{D_n}$ to Z		275 275								ns	
t_{PZH} / t_{PZL}	Output Enable Time		60 60								ns	
t_{PHZ} / t_{PLZ}	Output Disable Time		50 50								ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} / t_{THL}	Output Transition Time		45 45								ns	
t_{PLH} / t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} / t_{PHL}	Propagation Delay, I_0 to $\overline{W}$										ns	
t_{PLH} / t_{PHL}	Propagation Delay, $\overline{D_n}$ to $\overline{W}$										ns	
t_{PLH} / t_{PHL}	Propagation Delay, $\overline{D_n}$ to $\overline{X}$, $\overline{Y}$										ns	
t_{PLH} / t_{PHL}	Propagation Delay, $\overline{D_n}$ to Z										ns	
t_{PZH} / t_{PZL}	Output Enable Time										ns	
t_{PHZ} / t_{PLZ}	Output Disable Time										ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} / t_{THL}	Output Transition Time										ns	

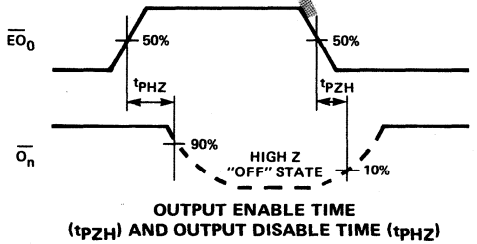
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (Cont'd)

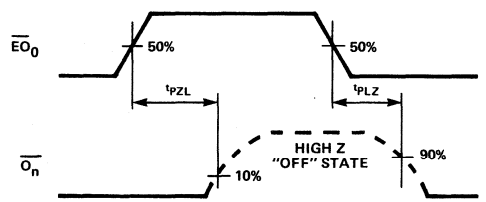
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{CW}	Minimum Clock Period		375								ns	C_L = 15 pF Input Transition Times ≤ 20 ns
$t_wCP(L)$	CP Minimum Pulse Width, LOW		100								ns	
$t_wCP(H)$	CP Minimum Pulse Width, HIGH		200								ns	
t_s	Set-Up Time, $\overline{EX}$ to CP		0								ns	
t_h	Hold Time, $\overline{EX}$ to CP		0									
t_s	Set-Up Time, A_n to CP		75								ns	
t_h	Hold Time, A_n to CP		0									
t_s	Set-Up Time, $\overline{D_n}$ to CP		275								ns	
t_h	Hold Time, $\overline{D_n}$ to CP		0									
t_s	Set-Up Time, I_n to CP		250								ns	
t_h	Hold Time, I_n to CP		0									
f_{MAX}	Input Count Frequency (Note 1)		2.6								MHz	

NOTES:
1. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
2. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.
3. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
4. Propagation Delays and Output transition times are graphically described in this section under F4000 Series CMOS Family Characteristcs.
5. Both Set-up times must be met simultaneously.
6. The Internal Clock is generated from CP and $\overline{EX}$. The Internal Clock is HIGH if $\overline{EX}$ or CP is HIGH; LOW if $\overline{EX}$ and CP are LOW. For timing considerations the $\overline{EX}$, CP two input active LOW AND gate is considered to exhibit no propagation delay. Actual timing requirements are referenced to the extrenal CP and $\overline{EX}$ inputs.

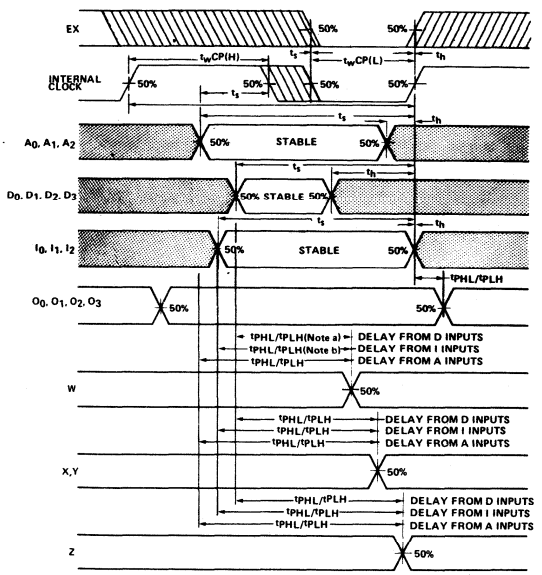
SWITCHING WAVEFORMS



OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})



PROPAGATION DELAYS, A_n to Z, I_n to Z, $\overline{D}_n$ to Z, A_n to $\overline{X}$, $\overline{Y}$, I_n to $\overline{X}$, $\overline{Y}$, $\overline{D}_n$ to $\overline{X}$, $\overline{Y}$, A_n to $\overline{W}$, I_n to $\overline{W}$, $\overline{D}_n$ to $\overline{W}$, I_n to $\overline{O}_n$ SET-UP AND HOLD TIMES $\overline{EX}$ TO CP, A_n TO CP, $\overline{D}_n$ to CP, I_n to CP, MINIMUM INTERNAL CLOCK PULSE

NOTES:
a. Delay for logical operation (I_1 or I_2 = HIGH)
b. Delay for arithmetic operation (I_1 = I_2 = LOW)
c. Set-up Times (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.

F4706/34706
PROGRAM STACK
FAIRCHILD MACROLOGIC™ CMOS

DESCRIPTION – The F4706 is a 16-word by 4-bit "Push-Down Pop-Up" Program Stack. It is designed to implement Program Counter (PC) and return address storage for nested subroutines in programmable digital systems. The F4706 executes four instructions: Return, Branch, Call and Fetch as specified by a 2-bit instruction. When the device is initialized, the program counter (PC) is in the top location of the stack. As a new PC value is "pushed" into the stack (Call Operation), all previous PC values effectively move down one level. The top location of the stack is the current PC. Up to 16 PC values can be stored, which gives the F4706 a 15 level nesting capability. "Popping" the stack (Return Operation) brings the most recent PC to the top of the stack and makes it available at the two output buses. The remaining two instructions affect only the top location of the stack. In the Branch Operation a new PC value is loaded into the top location of the stack from the $\overline{D}_0 - \overline{D}_3$ inputs. In the Fetch Operation, the contents of the top stack location (current PC value) are put on the $X_0 - X_3$ bus and the current PC value is incremented.

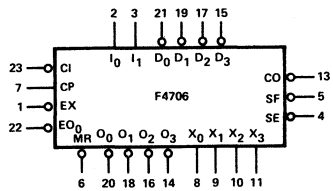
The F4706 may be expanded to any word length without additional logic. Three-state output drivers are provided on the 4-bit Address ($X_0 - X_3$) and Data Outputs, ($\overline{O}_0 - \overline{O}_3$); the X-bus outputs are enabled internally and only during the Fetch Instruction whereas the O-bus outputs are controlled by an Output Enable ($\overline{EO}_0$). Two status outputs, Stack Full ($\overline{SF}$) and Stack Empty ($\overline{SE}$) are provided. The F4706 is a member of Fairchild's F4000 Macrologic CMOS family, and is available in the new slim 24-pin package.

- 16-WORD BY 4-BIT LIFO
- 15-LEVEL NESTING CAPABILITY
- VERY LOW POWER – IDEAL FOR BATTERY OPERATION
- RELATIVE ADDRESSING CAPABILITY
- 2 MHz MICROINSTRUCTION RATE
- PROGRAM COUNTER LOADABLE FROM DATA BUS
- OPTIONAL AUTOMATIC INCREMENT OF PROGRAM COUNTER
- STACK LIMIT STATUS INDICATORS
- 3-STATE OUTPUTS
- EXPANDABLE IN MULTIPLES OF 4 BITS
- NEW SLIM 24-PIN DIP

PIN NAMES

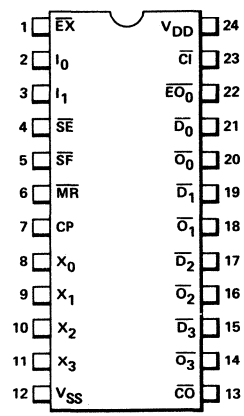
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)
I_0, I_1	Instruction Inputs
$\overline{EX}$	Execute Input (Active LOW)
CP	Clock Input
$\overline{MR}$	Master Reset Input (Active LOW)
$\overline{CI}$	Carry Input (Active LOW)
$\overline{EO}_0$	Output Enable Input (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Output Data Outputs (Active LOW)
X_0-X_3	Address Outputs
$\overline{CO}$	Carry Output (Active LOW)
$\overline{SF}$	Stack Full Output (Active LOW)
$\overline{SE}$	Stack Empty Output (Active LOW)

LOGIC SYMBOL



V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



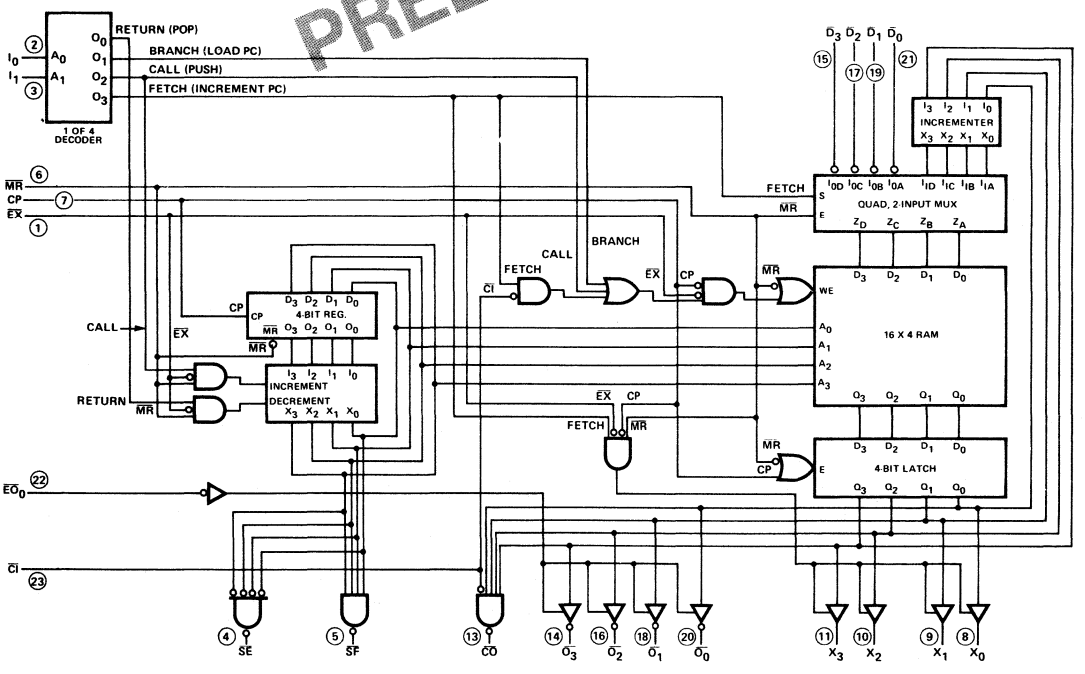
NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

TABLE I
INSTRUCTION SET FOR THE F4706

I_1	I_0	INSTRUCTION	INTERNAL OPERATION	X-BUS	O-BUS (WITH $\overline{EO}_0$ LOW)
L	L	Return (Pop)	Decrement Stack Pointer	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the new value while CP is LOW. When CP goes HIGH again, the output will reflect the new value.
L	H	Branch (Load PC)	Load D-Bus into current Program Counter location	Disabled	Current Program Counter until CP goes HIGH again, then updated with newly entered PC value.
H	L	Call (Push)	Increment Stack Pointer and Load D-Bus into new Program Counter Location	Disabled	Depending on the relative timing of $\overline{EX}$ and CP, the outputs will reflect the current program counter or the previous contents of the incremented SP location. When CP goes HIGH again, the outputs will reflect the newly entered PC value. See Timing Diagrams for details.
H	H	Fetch (Increment PC)	Increment Current Program Counter if $\overline{CI}$ is LOW	Current Program Counter while both CP and $\overline{EX}$ are LOW, disabled while CP or $\overline{EX}$ is HIGH	Current Program Counter until CP goes HIGH again, then updated with incremented PC value.

H = HIGH Level; L = LOW Level

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
◯ = Pin Number

FUNCTIONAL DESCRIPTION – As shown in the Block Diagram, the F4706 consists of an input multiplexer, a 16 x 4 RAM with output latches addressed by the Stack Pointer (SP), an incrementor, control logic, and output buffers. The F4706 is organized around three 4-bit buses; the Input Data (D) Bus ($\overline{D}_0, \overline{D}_1, \overline{D}_2, \overline{D}_3$), Output Data (O) Bus ($\overline{O}_0, \overline{O}_1, \overline{O}_2, \overline{O}_3$) and the Address (X) Bus (X_0, X_1, X_2, X_3). The F4706 implements four instructions as determined by inputs I_0 and I_1. (See Table I). The O-bus is derived from the RAM output latches and enabled by the active LOW Output Enable ($\overline{EO}_0$) input. The X-bus is also derived from the output latches; it is enabled internally during the Fetch Instruction. Execution of instructions is controlled by the Execute ($\overline{EX}$) and Clock (CP) inputs.

FETCH OPERATION – The Fetch Operation places the content of the current Program Counter (PC) on the X-bus. If the Carry In ($\overline{CI}$) is LOW, the current PC is incremented in preparation for the next Fetch. If $\overline{CI}$ is HIGH, the value of the current program is unchanged, (Iterative Fetch).

The instruction code is set up on the I lines when CP is HIGH. The active level LOW Execute ($\overline{EX}$) is normally set up at this time as well. The control logic interprets I_0 and I_1 and selects the incrementor output as the data source to the RAM via the input multiplexer. The current PC value is loaded into the latches and is available on the O-bus if $\overline{EO}_0$ is LOW. When CP is LOW (assuming $\overline{EX}$ is also LOW) the output latches are disabled from following the RAM output and the X-bus Output buffers are enabled, applying the current PC to the X-bus. The output of the incrementor is written into the RAM during the period when CP and $\overline{EX}$ are LOW. If $\overline{CI}$ is LOW, the value stored in the current PC, plus one, is written into the RAM. If $\overline{CI}$ is HIGH, the current PC is not incremented. Carry Out ($\overline{CO}$) is LOW when the contents of the current PC is at its maximum, i.e., all ones. When CP or $\overline{EX}$ goes HIGH, writing into the RAM is inhibited and the Address buffers ($X_0 - X_3$) are disabled.

BRANCH OPERATION – During a Branch Operation, the Data Inputs ($\overline{D}_0 - \overline{D}_3$) are loaded into the current program counter.

The instruction code and the $\overline{EX}$ input are set up when CP is HIGH. The stack pointer remains unchanged. When CP goes LOW (assuming $\overline{EX}$ is LOW), the D-bus inputs are written into the current PC. The X-bus drivers are not enabled during a Branch Operation.

CALL OPERATION – During a Call Operation the content of the data bus is loaded into the top location of the stack and all previous PC values are effectively moved down one level.

The instruction code and the $\overline{EX}$ input are set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is added to the stack pointer value thus incrementing the RAM address. When CP is LOW (assuming $\overline{EX}$ is LOW), the D-bus inputs are written into this new RAM location. On the LOW-to-HIGH CP transition, the incremented stack pointer value is loaded into the stack pointer register. When the RAM address is "1111" the Stack Full output ($\overline{SF}$) is LOW, indicating that no further Call Operations should be initiated. If an additional Call Operation is performed SP is incremented to "0000", the contents of that location will be written over, $\overline{SF}$ will go HIGH and the Stack Empty ($\overline{SE}$) will go LOW.

The X-bus drivers are not enabled during a Call Operation.

RETURN OPERATION – During the Return Operation the previous PC is "popped" to become the current PC.

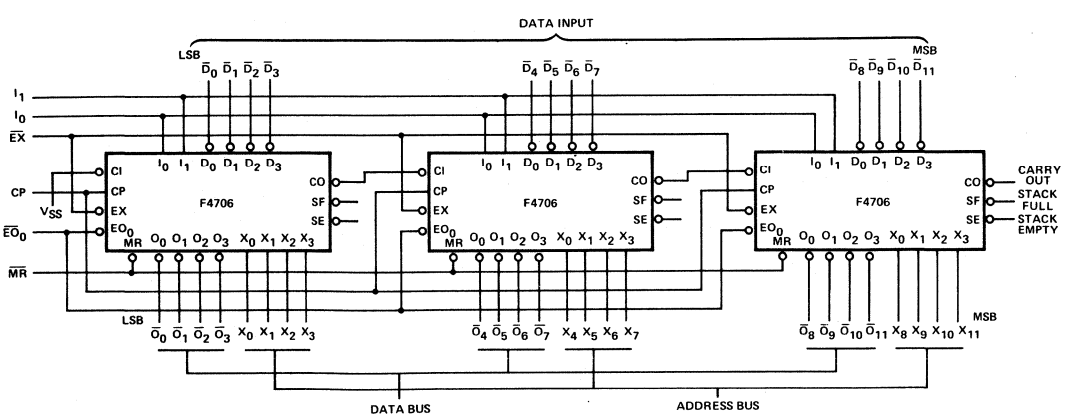
The instruction is set up when CP is HIGH. When $\overline{EX}$ is LOW, a "one" is subtracted from the stack pointer value, thus decrementing the RAM address, presenting the "popped" PC value through the enabled latches to the three-state O-bus drivers. When CP is LOW, the latches are disabled, thereby holding the new current value of the PC. On the LOW-to-HIGH CP transition the decremented stack pointer value is loaded into the stack pointer register.

The X-bus drivers are not enabled during a return operation.

When the RAM address is "0000", the Stack Empty output ($\overline{SE}$) is LOW, indicating that no further return operations should be initiated. If an additional Return Operation is performed, SP is decremented to "1111", the $\overline{SE}$ will go HIGH and the Stack Full output ($\overline{SF}$) will go LOW. Operation of the active LOW Master Reset ($\overline{MR}$) causes the SP to be reset and the contents of that RAM location (0000) to be cleared. The Stack Empty ($\overline{SE}$) output goes LOW. This operation overrides all other inputs.

MULTIPLE **F4706** OPERATION – The F4706 may be expanded to any word length in multiples of four without external logic. The connection for expanded operation is shown in Figure 1. Carry In ($\overline{CI}$) and Carry Out ($\overline{CO}$) are connected to provide automatic increment of the current program counter during the Fetch Operation. The $\overline{CI}$ input of the least significant F4706 is tied LOW to ground; the $\overline{CO}$ input of the least significant F4706 is connected to the $\overline{CI}$ input of the next significant F4706. If automatic increment during fetch is not desired, the $\overline{CI}$ input of the least significant F4706 is held high.

Fig. 1 F4706 EXPANSION, A 16 BY 12 PROGRAM STACK



*Tie to V_{DD} to disable automatic increment.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

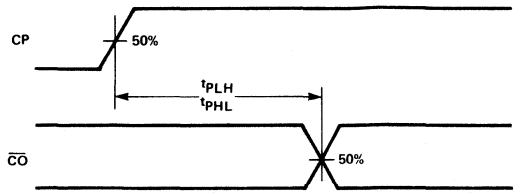
SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}_0 = V_{DD}$
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}_0 = V_{DD}$
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC										μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
													MAX	
		XM											MIN, 25°C	
													MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (ALL MODES OF OPERATION)

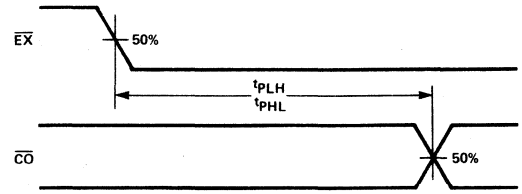
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{CO}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{CO}$										ns	
t_{PZH} t_{PZL}	Output Enable Time										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Output Disable Time										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{CO}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{CO}$										ns	
t_{PZH} t_{PZL}	Output Enable Time										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Output Disable Time										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time										ns	
t_{rec}	$\overline{MR}$ Recovery Time										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
$t_w\overline{MR}(L)$	$\overline{MR}$ Minimum Pulse Width										ns	
$t_wCP(L)$ $t_wCP(H)$	CP Minimum Pulse Width, LOW CP Minimum Pulse Width, HIGH										ns	
t_{CW}	Clock Period										ns	
t_s t_h	Set-Up Time, $\overline{EX}$ to CP Hold Time, $\overline{EX}$ to CP										ns	
t_s t_h	Set-Up Time, I_n to CP Hold Time, I_n to CP										ns	
t_s t_h	Set-Up Time, $\overline{CI}$ to CP Hold Time, $\overline{CI}$ to CP										ns	

Notes on following pages.

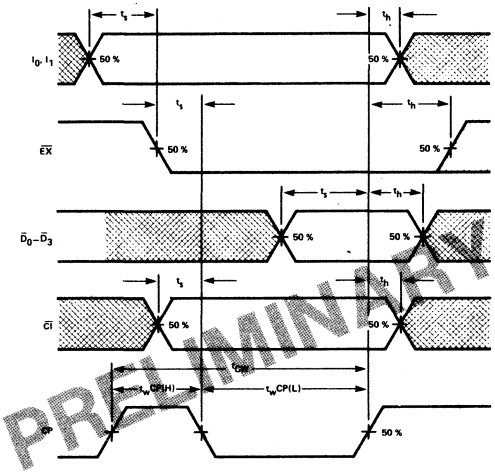
SWITCHING WAVEFORMS FOR ALL MODES OF OPERATION



PROPAGATION DELAY, CP TO $\overline{CO}$

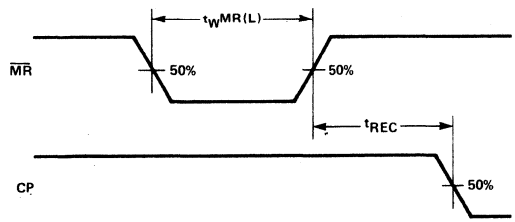


PROPAGATION DELAY, $\overline{EX}$ TO $\overline{CO}$

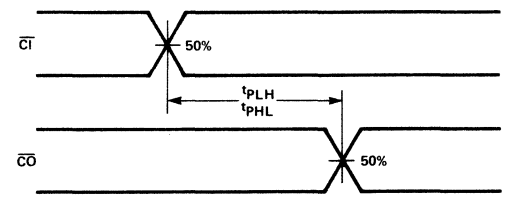


CLOCK PERIOD, MINIMUM CP PULSE WIDTH, AND
SET-UP AND HOLD TIMES $\overline{CI}$ TO CP, $\overline{D_n}$ TO CP, $\overline{EX}$ TO CP, I_n TO CP

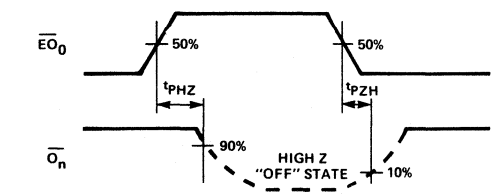
RESET OPERATION

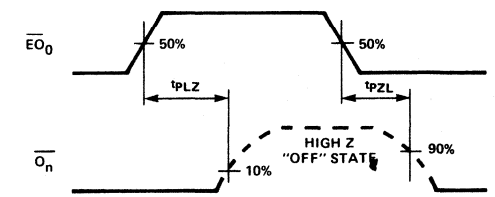


MINIMUM $\overline{MR}$ PULSE WIDTH AND $\overline{MR}$ RECOVERY TIME



PROPAGATION DELAY, $\overline{CI}$ TO $\overline{CO}$





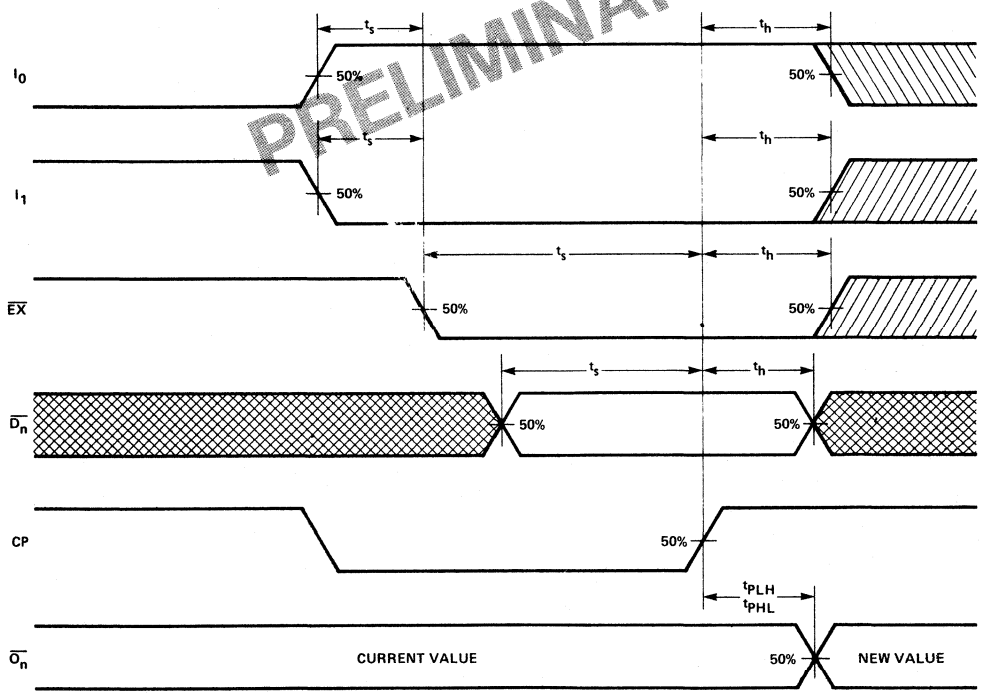
$\overline{EO}_0$ TO OUTPUT ENABLE AND DISABLE TIMES

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (BRANCH OPERATION)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, I_n to $\overline{EX}$ Hold Time, I_n to $\overline{EX}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, $\overline{D_n}$ to CP Hold Time, $\overline{D_n}$ to CP										ns	
t_h	Hold Time, I_n to CP										ns	
$t_w\overline{EX}$	Min. $\overline{EX}$ Pulse Width										ns	

BRANCH OPERATION, CP GOES HIGH BEFORE $\overline{EX}$

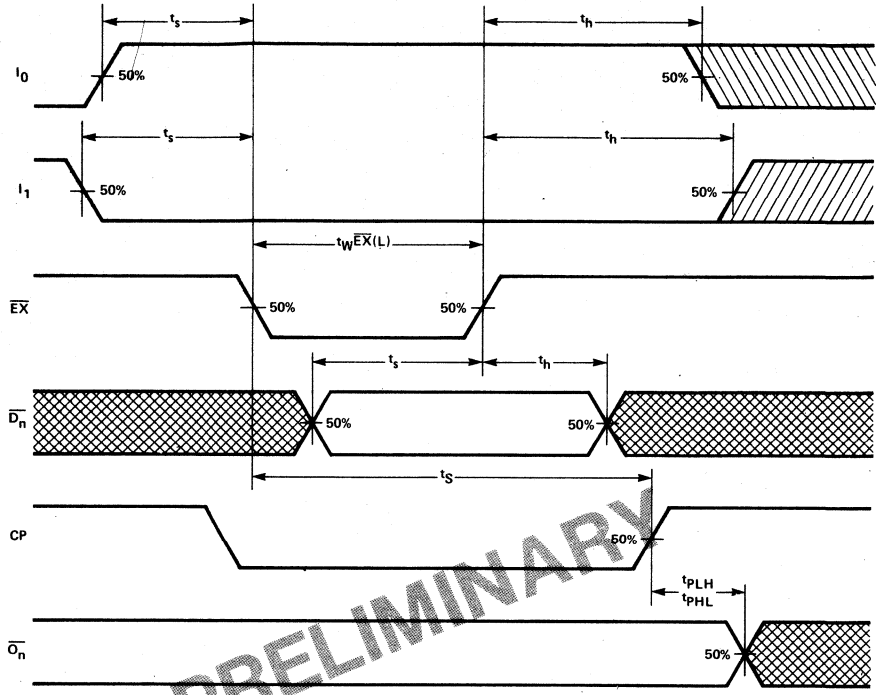


PROPAGATION DELAY CP TO $\overline{O_n}$ AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{D_n}$ TO CP AND I_n TO CP.

CONDITIONS: $\overline{EO}_0$ = LOW

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS FOR A BRANCH OPERATION
$\overline{EX}$ GOES HIGH BEFORE CP



PROPAGATION DELAY, CP TO $\overline{O_n}$, MINIMUM $\overline{EX}$ PULSE WIDTH AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{EX}$ TO CP AND I_n TO CP

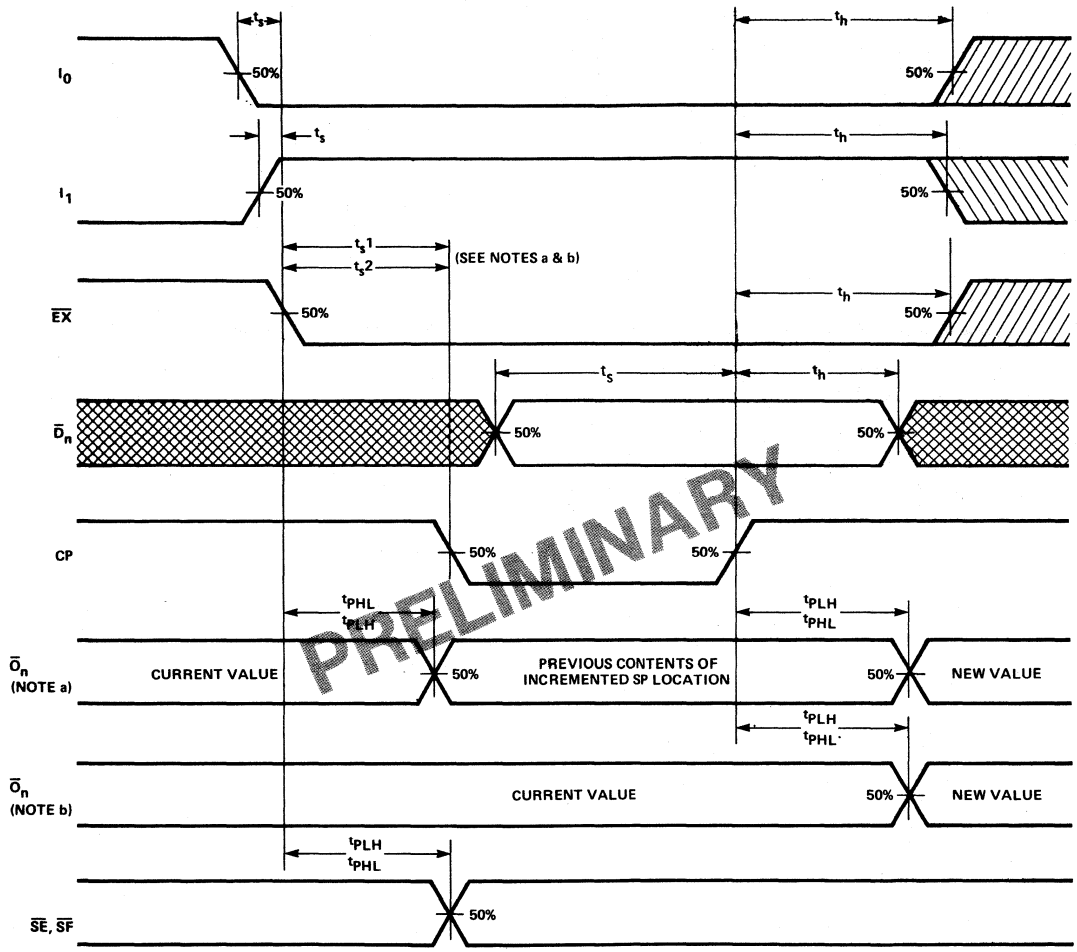
CONDITIONS: $\overline{EO_0}$ = LOW

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (CALL OPERATION ONLY)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O_n}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O_n}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$										ns	
t_s	Set-Up Time, $\overline{EX}$ to I_n										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_h	Hold Time, CP to I_n											
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP With Data On $\overline{O_n}$ While CP = LOW										ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP With No Change In $\overline{O_n}$ While CP = LOW										ns	
$t_h\overline{EX}$	Hold Time, CP to $\overline{EX}$										ns	
t_s	Set-Up Time, $\overline{D_n}$ to CP										ns	
t_h	Hold Time, $\overline{D_n}$ to CP											

SWITCHING WAVEFORMS FOR A CALL (PUSH) OPERATION



PROPAGATION DELAY, CP TO $\overline{O_n}$, $\overline{EX}$ TO $\overline{O_n}$, $\overline{EX}$ TO $\overline{SE}$ OR $\overline{SF}$, AND SET-UP AND HOLD TIMES, $\overline{EX}$ TO I_n, CP TO I_n, $\overline{D_n}$ TO CP, CP TO $\overline{EX}$.

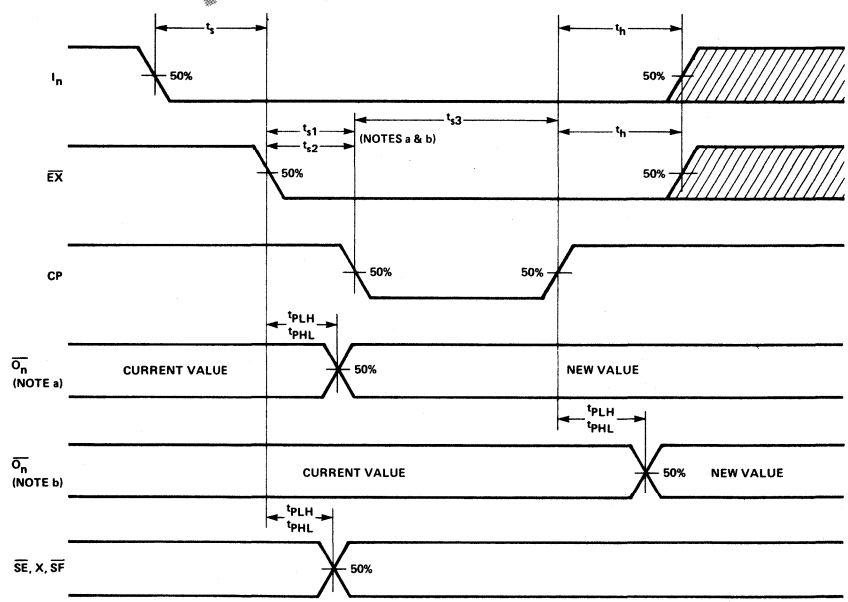
CONDITIONS: $\overline{EO}_0$ = LOW

NOTES: a. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW (t_{s1} EX is met).
b. Condition which occurs when $\overline{EX}$ goes LOW slightly before CP goes LOW (t_{s2} EX is met).
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

AC CHARACTERISTICS AND SWITCHING REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (RETURN OPERATION ONLY)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O_n}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{O_n}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{EX}$ to $\overline{SE}$ or $\overline{SF}$										ns	
t_s	Set-Up Time, $\overline{EX}$ to I_n										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_h	Hold Time, I_n to CP										ns	
$t_{s1}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP Which Guarantees a New Value On $\overline{O_n}$ While CP is LOW.										ns	
$t_{s2}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ Must Be Met For Proper Operation										ns	
$t_{s3}\overline{EX}$	Set-Up Time, $\overline{EX}$ to CP Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ Must Be Met For Proper Operation										ns	

SWITCHING WAVEFORMS FOR A RETURN (POP) OPERATION



PROPAGATION DELAY, CP TO $\overline{O_n}$, $\overline{EX}$ TO $\overline{O_n}$, $\overline{EX}$ TO $\overline{SE}$ OR $\overline{SF}$, AND SET-UP AND HOLD TIMES, $\overline{EX}$ TO I_n, I_n TO CP, $\overline{EX}$ TO CP

CONDITIONS: $\overline{EO_0}$ = LOW

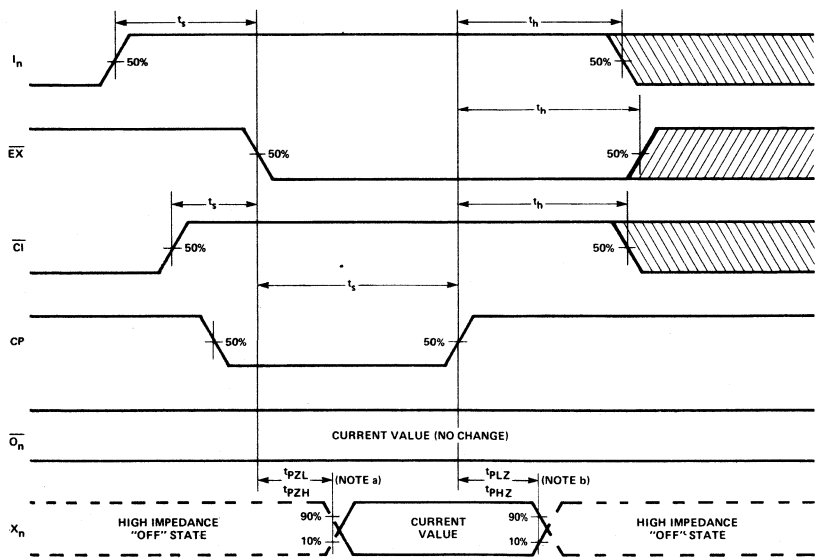
NOTES: a. Condition which occurs when $\overline{EX}$ goes LOW considerably before CP goes LOW ($T_{s1}\overline{EX}$ is met).
b. Condition which occurs when $\overline{EX}$ goes LOW slightly before or after CP goes LOW (Either $t_{s2}\overline{EX}$ or $t_{s3}\overline{EX}$ are met).
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (FETCH OPERATION ONLY)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Output Enable Time (X_n)										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Output Disable Time (X_n)										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PLH} t_{PHL}	Propagation Delay, CP to $\overline{O_n}$										ns	C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Output Enable Time (X_n)										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Output Disable Time (X_n)										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_s	Set-Up Time, I_n to $\overline{EX}$										ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_h	Hold Time, I_n to CP or $\overline{EX}$										ns	
t_s	Set-Up Time, $\overline{EX}$ to CP										ns	
t_s	Set-Up Time, $\overline{CI}$ to CP										ns	
t_h	Hold Time, $\overline{CI}$ to $\overline{EX}$										ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS FOR AN ITERATIVE FETCH

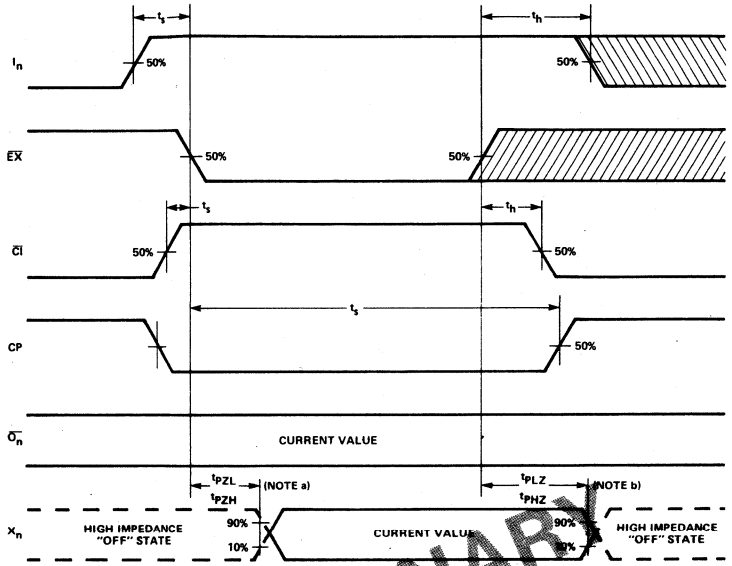


OUTPUT X_n DISABLE DELAY, OUTPUT X_n ENABLE DELAY, AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, I_n TO CP, $\overline{EX}$ TO CP, AND $\overline{CI}$ TO $\overline{EX}$.

CONDITIONS: $\overline{EO}_0$ = LOW, CP GOES HIGH BEFORE $\overline{EX}$

NOTES: a. $X_0 - X_3$ turn on delay measured from time both EX and CP go LOW.
b. $X_0 - X_3$ turn off delay measured from time either EX or CP goes HIGH.
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

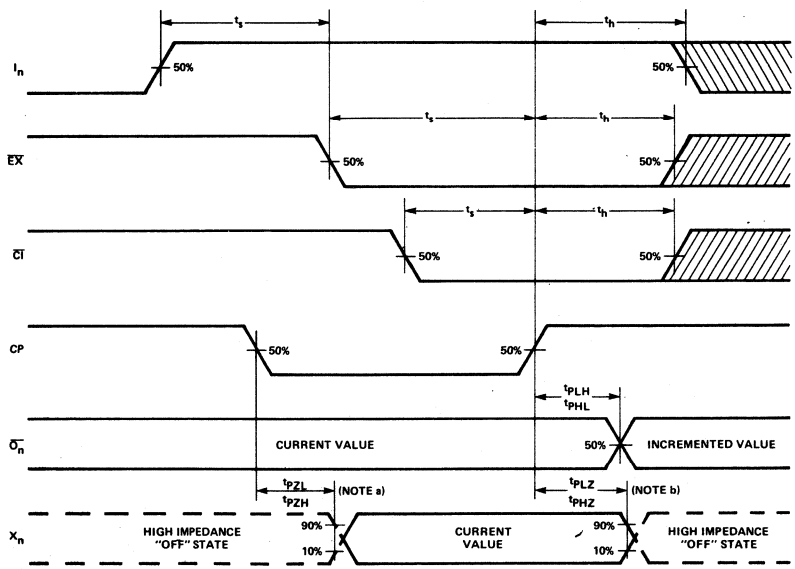
SWITCHING WAVEFORMS FOR AN ITERATIVE FETCH (Cont.)



OUTPUT X_n ENABLE AND DISABLE TIMES AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{CI}$ TO $\overline{EX}$ AND $\overline{EX}$ TO CP.

CONDITIONS: $\overline{EO}_0$ = LOW, $\overline{EX}$ GOES HIGH BEFORE CP

SWITCHING WAVEFORMS FOR A FETCH OPERATION WITH INCREMENT PC

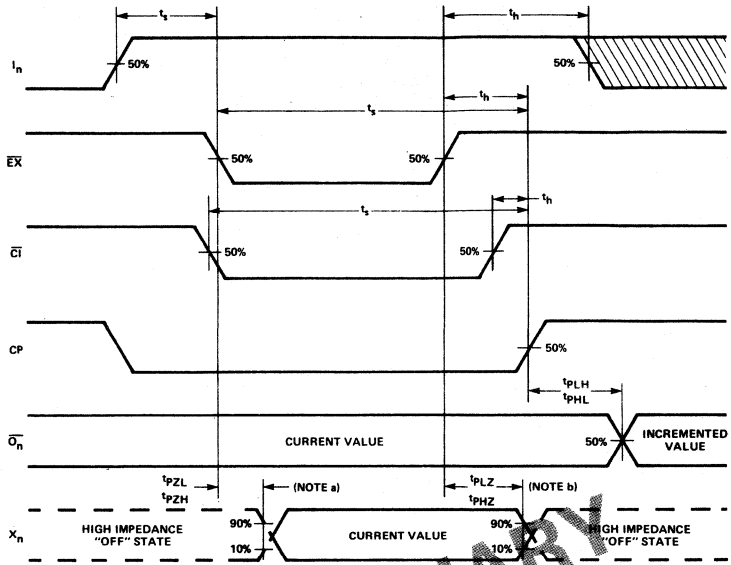


PROPAGATION DELAY, CP TO $\overline{O}_n$, OUTPUT X_n ENABLE AND DISABLE TIMES AND SET-UP AND HOLD TIMES, I_n TO $\overline{EX}$, $\overline{EX}$ TO CP, AND $\overline{CI}$ TO CP

CONDITIONS: $\overline{EO}_0$ = LOW, CP GOES HIGH BEFORE $\overline{EX}$

NOTES: a. $X_0 - X_3$ turn on delay measured from time both $\overline{EX}$ and CP go LOW.
b. $X_0 - X_3$ turn off delay measured from time either $\overline{EX}$ or CP goes HIGH.
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

SWITCHING WAVEFORMS FOR A FETCH OPERATION WITH INCREMENT PC



PROPAGATION DELAY CP TO $\overline{O_n}$, OUTPUT X_n ENABLE AND DISABLE TIMES, AND SET-UP AND HOLD TIMES I_n TO $\overline{EX}$, $\overline{EX}$ TO CP AND $\overline{CI}$ TO CP

CONDITIONS: $\overline{EO}_0$ = LOW, $\overline{EX}$ GOES HIGH BEFORE CP

NOTES:
a. $X_0 - X_3$ turn on delay measured from the time both $\overline{EX}$ and CP go LOW.
b. $X_0 - X_3$ turn on delay measured from the time either $\overline{EX}$ or CP go HIGH.
c. Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4707/34707
DATA ACCESS REGISTER
FAIRCHILD MACROLOGIC™ CMOS

DESCRIPTION – The F4707 Data Access Register (DAR) performs memory address arithmetic for RAM resident stack applications. It contains three 4-bit registers intended for program counter (R_0), stack pointer (R_1) and operand address (R_2). The F4707 implements 16 instructions (see Table 1) which allow either pre or post decrement/increment and register-to-register transfer in a single clock cycle. It is expandable in 4-bit increments and can operate at a 2 MHz microinstruction rate on a 16-bit word. The 3-state outputs are provided for bus oriented applications. The F4707 is packaged in the new slim 24-pin Dual In-line Package.

- **16 INSTRUCTIONS FOR ADDRESS MANIPULATION**
- **EXPANDABLE IN 4-BIT INCREMENTS**
- **OPTIONAL PRE OR POST INCREMENT/DECREMENT**
- **3-STATE OUTPUTS**
- **2 MHz MICROINSTRUCTION RATE ON A 16-BIT WORD**
- **NEW SLIM 24-PIN DIP**

PIN NAMES

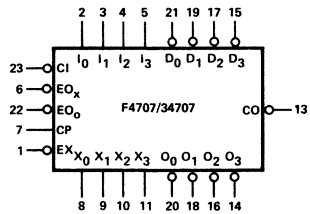
I_0-I_3	Instruction Word Inputs
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
$\overline{CI}$	Carry Input (Active LOW)
$\overline{CO}$	Carry Output (Active LOW)
$\overline{EX}$	Execute Input (Active LOW)
$\overline{EO}_X$	Address Output Enable Input (Active LOW)
$\overline{EO}_o$	Data Output Enable Input (Active LOW)
X_0-X_3	Address Outputs
$\overline{O}_0$-$\overline{O}_3$	Data Outputs (Active LOW)

TABLE 1
INSTRUCTION SET FOR THE F4707

INSTRUCTION				COMBINATORIAL FUNCTION AVAILABLE ON THE X-BUS	SEQUENTIAL FUNCTION OCCURRING ON THE NEXT RISING CP EDGE
I_3	I_2	I_1	I_0		
L	L	L	L	R_0	R_0 plus D plus CI → R_0 and 0-register
L	L	L	H	R_0 plus D plus CI	
L	L	H	L	R_0	R_0 plus D plus CI → R_1 and 0-register
L	L	H	H	R_0 plus D plus CI	
L	H	L	L	R_0	R_0 plus D plus CI → R_2 and 0-register
L	H	L	H	R_0 plus D plus CI	
L	H	H	L	R_1	R_1 plus D plus CI → R_1 and 0-register
L	H	H	H	R_1 plus D plus CI	
H	L	L	L	R_2	D plus CI → R_2 and 0-register
H	L	L	H	D plus CI	
H	L	H	L	R_0	D plus CI → R_0 and 0-register
H	L	H	H	D plus CI	
H	H	L	L	R_2	R_2 plus D plus CI → R_2 and 0-register
H	H	L	H	R_2 plus D plus CI	
H	H	H	L	R_1	D plus CI → R_1 and 0-register
H	H	H	H	D plus CI	

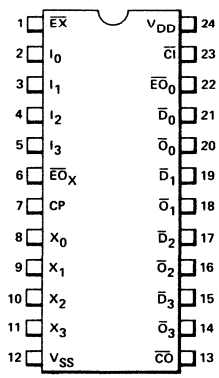
L = LOW Level H = HIGH Level

LOGIC SYMBOL



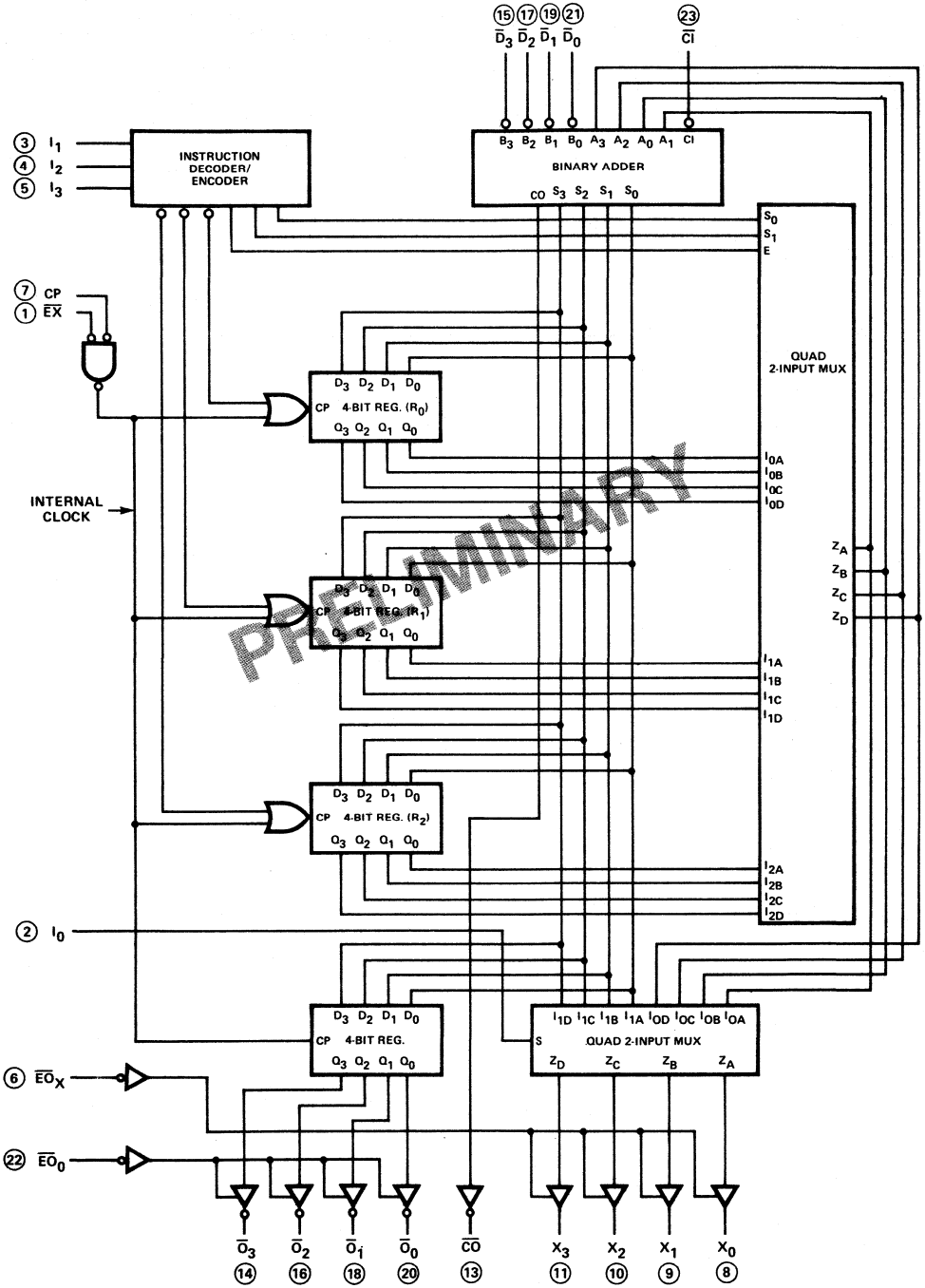
V_{DD} = Pin 24
V_{SS} = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION – The F4707 contains a 4-bit slice of three registers (R_0, R_1, R_2), a 4-bit adder, a 3-state address output buffer (X_0-X_3), and a separate output register with 3-state buffers ($\overline{O}_0$-$\overline{O}_3$), that can put the register contents on the data bus (refer to the Block Diagram). The DAR can perform 16 instructions, selected by I_0-I_3, as listed in Table 1.

OPERATION – The F4707 operates on a single clock. CP and $\overline{EX}$ are inputs to a two input, active LOW NAND gate. For normal operation $\overline{EX}$ is LOW. A microcycle starts as the clock goes HIGH. Data inputs $\overline{D}_0$-$\overline{D}_3$ are applied to the Adder as one of the operands. Three (I_1, I_2, I_3) of the four instruction lines select which of the three registers, if any, is to be used as the other operand. The next LOW-to-HIGH CP transition writes the result from the Adder into one register (R_0, R_1, R_2) and into the output register provided $\overline{EX}$ is LOW. If the I_0 instruction input is HIGH, the multiplexer routes the result from the Adder to the 3-state buffer controlling the address bus (X_0-X_3) independent of $\overline{EX}$ and CP. If I_0 is LOW the multiplexer routes the output of the selected register directly into the 3-state buffer controlling the address bus (X_0-X_3), independent of $\overline{EX}$ and CP.

F4707 ARRAYS – The F4707 is organized as a 4-bit register slice. The active LOW $\overline{CI}$ and $\overline{CO}$ lines allow ripple-carry expansion over longer word lengths.

APPLICATIONS – In a typical application, the register utilization in the DAR may be as follows: R_0 is the program counter (PC), R_1 is the stack pointer (SP) for memory resident stacks and R_2 contains the operand address. For an instruction fetch, PC can be gated on the X-bus while it is being incremented (i.e., D-bus = 1). If the instruction fetched calls for an effective address for execution, which is displaced from the PC, the displacement can be added to the PC and loaded into R_2 during the next microcycle.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}_0$ = V_{DD}, $\overline{EO}_x$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}_0$ = V_{DD}, $\overline{EO}_x$ = V_{DD}
					−30			−60		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC										μA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM										μA	MIN, 25°C MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to $\overline{Q}_n$										ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, I_1-I_3 to X_n With I_0 = LOW										ns	
t_{PLH} t_{PHL}	Propagation Delay, I_1-I_3 to X_n With I_0 = HIGH										ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n With I_0 = LOW										ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n With I_0 = HIGH										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D}_n$ to X_n										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to X_n										ns	
t_{PLH} t_{PHL}	Propagation Delay, I_0 to X_n										ns	
t_{PLH} t_{PHL}	Propagation Delay, Positive-going Internal Clock to $\overline{CO}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$										ns	

Notes on following pages.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D_n}$ to $\overline{CO}$										ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, I_1-I_3 to $\overline{CO}$										ns	
t_{PZH} t_{PZL}	Output Enable Time										ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time										ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time										ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to $\overline{Q}_n$										ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, I_1-I_3 to X_n With I_0 = LOW										ns	
t_{PLH} t_{PHL}	Propagation Delay, I_1-I_3 to X_n With I_0 = HIGH										ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n With I_0 = LOW										ns	
t_{PLH} t_{PHL}	Propagation Delay, Internal Clock to X_n With I_0 = HIGH										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D_n}$ to X_n										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to X_n										ns	
t_{PLH} t_{PHL}	Propagation Delay, I_0 to X_n										ns	
t_{PLH} t_{PHL}	Propagation Delay, Positive-going Internal Clock to $\overline{CO}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CI}$ to $\overline{CO}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{D_n}$ to $\overline{CO}$										ns	
t_{PLH} t_{PHL}	Propagation Delay, I_1-I_3 to $\overline{CO}$										ns	
t_{PZH} t_{PZL}	Output Enable Time										ns	(R_L = 1 kΩto V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{PHZ} t_{PLZ}	Output Disable Time										ns	(R_L = 1 kΩ to V_{SS}) (R_L = 1 kΩ to V_{DD})
t_{TLH} t_{THL}	Output Transition Time										ns	
t_WCP(H)	Internal CP Minimum Pulse Width (HIGH)										ns	
t_WCP(L)	Internal CP Minimum Pulse Width (LOW)										ns	
t_s t_h	Set-up Time, I_1-I_3 to Internal Clock Hold Time, I_1-I_3 to Internal Clock										ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_s t_h	Set-up Time, $\overline{D_n}$, $\overline{CI}$ to Internal Clock Hold Time, $\overline{D_n}$, $\overline{CI}$ to Internal Clock										ns	

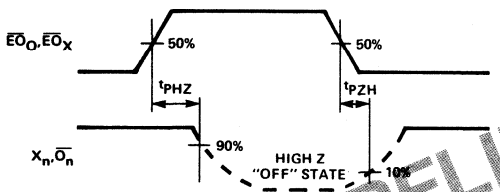
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS (Cont'd): V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

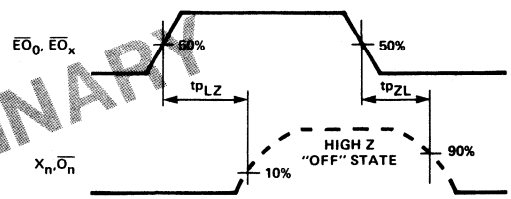
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_s t_h	Set-up Time, $\overline{CI}$ to Internal Clock Hold Time, $\overline{CI}$ to Internal Clock										ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{CW}	Internal Clock Period (Note 3)										ns	
f_{MAX}	Input Count Frequency (Note 5)										MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. The Internal Clock is generated from CP and $\overline{EX}$. The Internal Clock is HIGH if $\overline{EX}$ or CP is HIGH, LOW if $\overline{EX}$ and CP are LOW. For timing considerations the $\overline{EX}$, CP two input active LOW NAND gate is considered to exhibit no propagation delay. Actual timing requirements are referenced to the external CP and $\overline{EX}$ inputs.
4. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
5. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
6. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

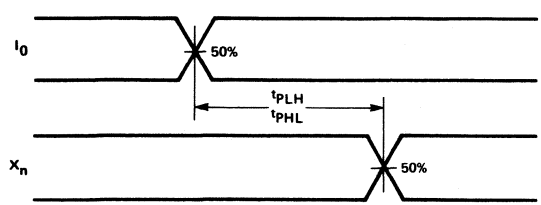
SWITCHING WAVEFORMS



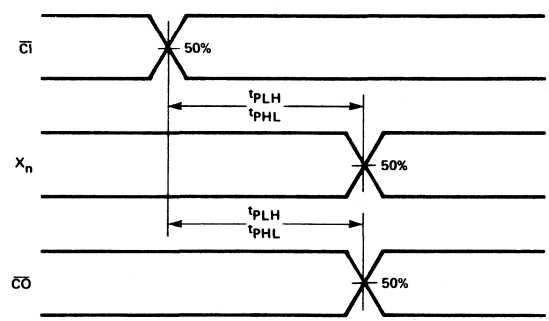
OUTPUT ENABLE TIME (t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME (t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

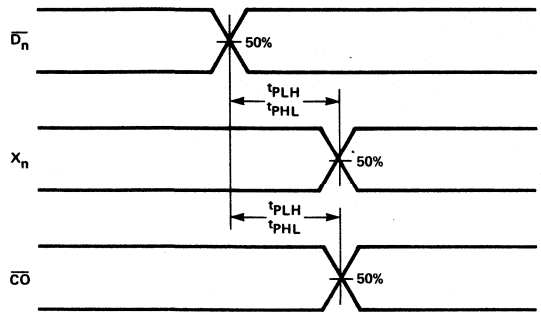


PROPAGATION DELAY, I_0 TO X_n
CONDITIONS: $\overline{EO}_X$ = LOW



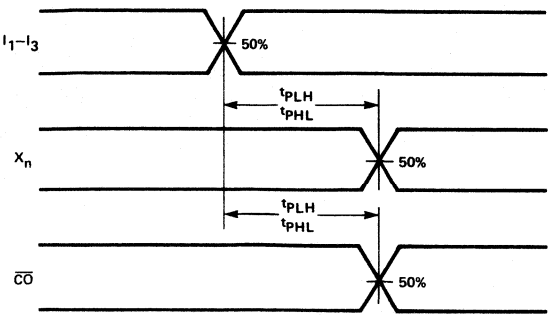
PROPAGATION DELAY, $\overline{CI}$ TO X_n AND $\overline{CI}$ TO $\overline{CO}$
CONDITIONS: $\overline{EO}_X$ = LOW, I_0 = HIGH

SWITCHING WAVEFORMS (Cont'd)



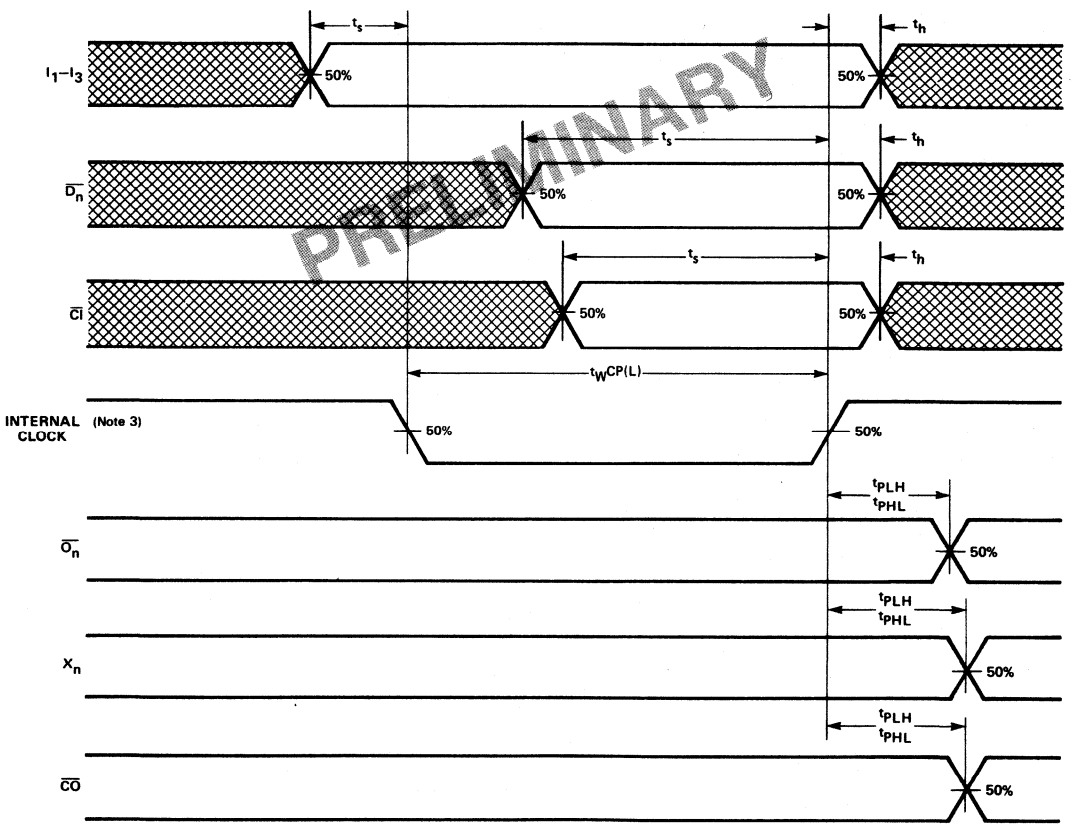
PROPAGATION DELAY, $\overline{D_n}$ TO X_n AND $\overline{D_n}$ TO $\overline{CO}$

CONDITIONS: $\overline{EO}_X$ = LOW, I_0 = HIGH



PROPAGATION DELAY, I_1–I_3 TO $\overline{CO}$ AND I_1–I_3 TO X_n

CONDITIONS: $\overline{EO}_X$ = LOW



PROPAGATION DELAYS, INTERNAL CLOCK TO $\overline{O_n}$, INTERNAL CLOCK TO X_n, INTERNAL CLOCK TO $\overline{CO}$, SET-UP AND HOLD TIMES, I_1–I_3 TO INTERNAL CLOCK, $\overline{D_n}$ TO INTERNAL CLOCK, $\overline{CI}$ TO INTERNAL CLOCK, AND MINIMUM INTERNAL CLOCK PULSE WIDTH

CONDITIONS: $\overline{EO}_X$ = $\overline{EO}_O$ = LOW

NOTE: Set-up (t_s) and Hold (t_h) Times are shown as positive values but may be specified as negative values.

F4710/34710

16 × 4 BIT CLOCKED RAM WITH 3-STATE OUTPUT REGISTER

FAIRCHILD MACROLOGIC™ CMOS

DESCRIPTION — The F4710 is a register-oriented 64-Bit Read/Write Memory organized as 16 words by four bits. An edge-triggered 4-bit output register allows new data to be written while the previous data is held. The 3-state data outputs provide flexibility and make the F4710 compatible with the other bus oriented circuits in the CMOS Macrologic family.

The F4710 consists of a 16 x 4-bit RAM selected by the four Address Inputs (A_0-A_3) and an edge-triggered 4-bit output register with 3-state output buffers.

WRITE OPERATION — When the three control inputs; Write Enable ($\overline{WE}$), Chip Select ($\overline{CS}$), and Clock (CP), are LOW the information on the Data Inputs ($\overline{D}_0$-$\overline{D}_3$) is written into the memory location selected by the Address Inputs (A_0-A_3). If the input data changes while $\overline{WE}$, $\overline{CS}$, and CP are LOW, the contents of the selected memory location follows these changes, provided set-up time criteria are met.

READ OPERATION — Whenever CS is LOW, WE is HIGH and CP goes from LOW-to-HIGH, the contents of the memory location selected by the Address Inputs (A_0-A_3) is edge-triggered into the Output Register.

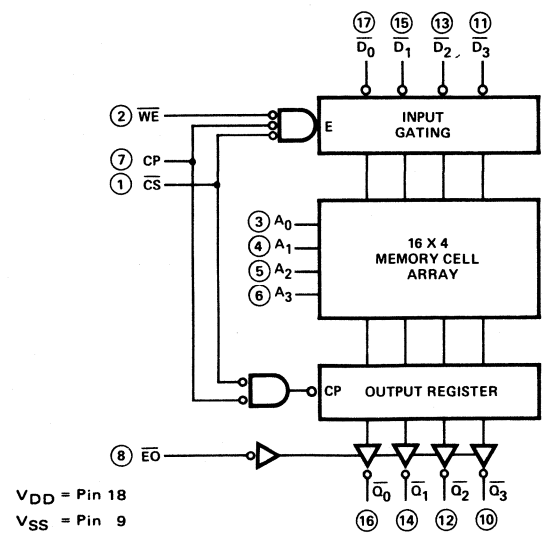
A 3-State Output Enable ($\overline{EO}$) controls the output buffers. When $\overline{EO}$ is HIGH the four Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are in a high impedance or OFF state; when $\overline{EO}$ is LOW, the Outputs are determined by the state of the output register.

- **2 MHz CLOCK RATE**
- **EDGE-TRIGGERED OUTPUT REGISTER**
- **3-STATE OUTPUTS**
- **OPTIMIZED FOR REGISTER STACK OPERATION**
- **18-PIN PACKAGE**

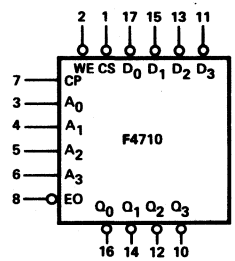
PIN NAMES

A_0-A_3	Address Inputs
$\overline{D}_0$-$\overline{D}_3$	Data Inputs (Active LOW)
$\overline{CS}$	Chip Select (Active LOW) Input
$\overline{EO}$	Output Enable (Active LOW) Input
$\overline{WE}$	Write Enable (Active LOW) Input
CP	Clock Input (L → H Edge-Triggered)
$\overline{Q}_0$-$\overline{Q}_3$	Buffered Outputs (Active LOW)

BLOCK DIAGRAM

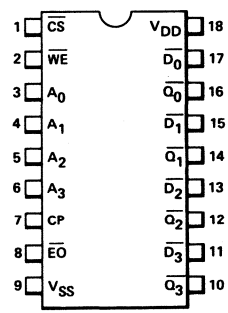


LOGIC SYMBOL



V_{DD} = Pin 18
V_{SS} = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{EO}$ = V_{DD}
					30			60		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			60		1.2			MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{EO}$ = V_{DD}
					−30			−6.0		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC		2.5			5			10		μA	MIN, 25°C	All Inputs common and at 0 V or V_{DD}
				15			30			60			MAX	
		XM		2.5			5			10		μA	MIN, 25°C	
				15			30			60			MAX	

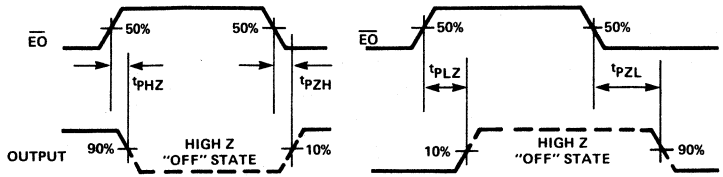
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
	READ MODE											C_L = 15 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to Output										ns	
t_{PZH} t_{PZL}	Enable Time, $\overline{EO}$ to Output										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{EO}$ to Output										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time										ns	
	READ MODE											C_L = 50 pF Input Transition Times ⩽ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, CP to Output										ns	
t_{PZH} t_{PZL}	Enable Time, $\overline{EO}$ to Output										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{EO}$ to Output										ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time										ns	
	WRITE MODE											C_L = 15 pF Input Transition Times ⩽ 20 ns
$t_W\overline{WE}$	Minimum $\overline{WE}$ Pulse Width (Note 4)										ns	
$t_W\overline{CS}$	Minimum $\overline{CS}$ Pulse Width (Note 4)										ns	
t_WCP	Minimum CP Pulse Width (Note 4)										ns	
t_s t_h	Set-Up Time $\overline{D_n}$ to $\overline{WE}$ (Note 5) Hold Time, $\overline{D_n}$ to $\overline{WE}$										ns	
t_s t_h	Set-Up Time, Address to $\overline{WE}$ Hold Time, Address to $\overline{WE}$ (Note 5)										ns	
	READ MODE											
t_s t_h	Set-Up Time Address to CP Hold Time Address to CP										ns	

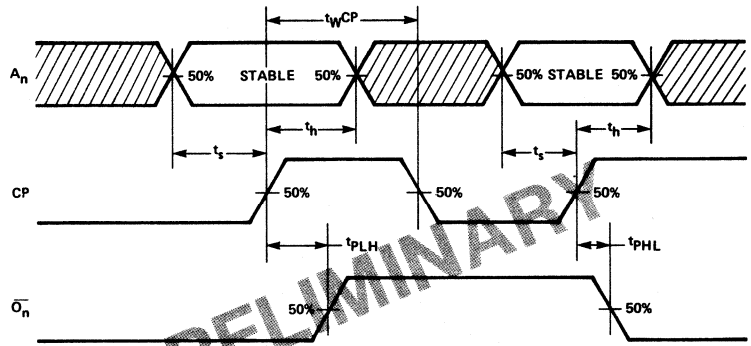
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation delays and Output Transition times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and Output Transition Times (t_{TLH} and t_{THL}) will change with output load capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. Writing occurs when $\overline{WE}$, $\overline{CE}$, and CP are LOW.
5. Assuming $\overline{WE}$ is utilized as a Writing STROBE.

SWITCHING WAVEFORMS

READ MODE



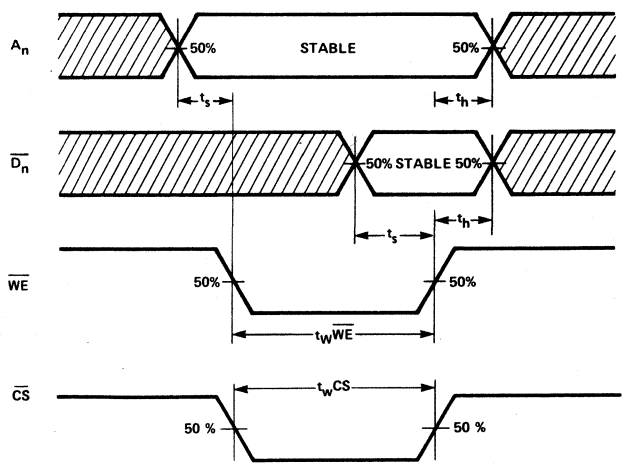
$\overline{EO}$ TO OUTPUT ENABLE AND DISABLE TIMES



MINIMUM CP PULSE WIDTH, PROPAGATION DELAY CLOCK TO OUTPUT, AND SET-UP AND HOLD TIMES ADDRESS TO CLOCK

CONDITIONS: $\overline{CS}$ = $\overline{EO}$ = LOW, $\overline{WE}$ = HIGH

WRITE MODE



MINIMUM $\overline{CS}$ PULSE WIDTH, MINIMUM WRITE ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES ADDRESS TO WE AND DATA TO $\overline{WE}$

CONDITIONS: CP = LOW

NOTE:
Set-up (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.

F4720/34720

256-BIT RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

FAIRCHILD CMOS LSI

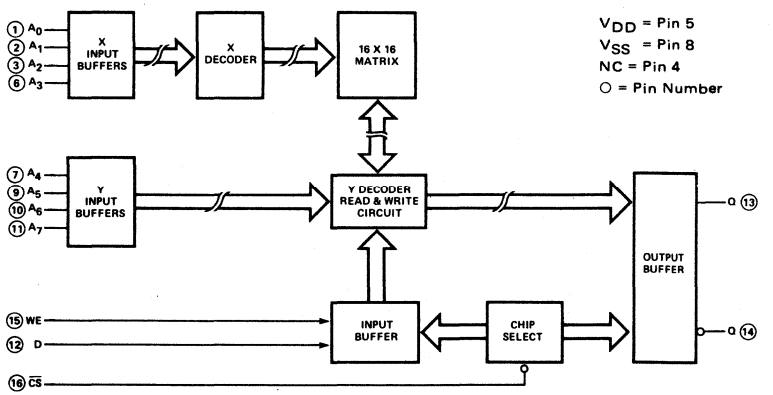
DESCRIPTION – The F4720 is a 256-Bit Random Access Memory with 3-State Outputs. It has a Data Input (D), eight Address Inputs (A_0-A_7), an active HIGH Write Enable Input (WE), an active LOW Chip Select Input ($\overline{CS}$), an active HIGH 3-State Output (Q) and an active LOW 3-State Output ($\overline{Q}$). Information on the Data Input (D) is written into the memory location selected by the Address Inputs (A_0-A_7) when the Chip Select Input ($\overline{CS}$) is LOW and the Write Enable Input (WE) is HIGH. Under these conditions, the device is transparent, i.e. the data input is reflected at the True and Complementary Outputs (Q, $\overline{Q}$). Information is read from the memory location selected by the Address Inputs (A_0-A_7) while the Chip Select ($\overline{CS}$) and the Write Enable (WE) Inputs are LOW. The Q Output is the information written into the memory, $\overline{Q}$ is its complement. When the Chip Select Input ($\overline{CS}$) is HIGH, both Outputs (Q, $\overline{Q}$) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The F4720 offers fully static operation.

- **3-STATE OUTPUTS**
- **ORGANIZATION – 256 WORDS X 1-BIT**
- **ON-CHIP DECODING**
- **TRUE AND COMPLEMENT OUTPUTS AVAILABLE**
- **FULLY STATIC**
- **LOW POWER DISSIPATION**
- **HIGH SPEED**

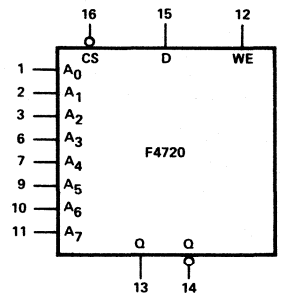
MODE SELECTION

$\overline{CS}$	WE	Q	$\overline{Q}$	MODE
L	H	Data Written Into Memory	Complement of Data Written Into Memory	Write
L	L	Data Written Into Memory	Complement of Data Written Into Memory	Read
H	X	High Impedance	High Impedance	Inhibit

BLOCK DIAGRAM

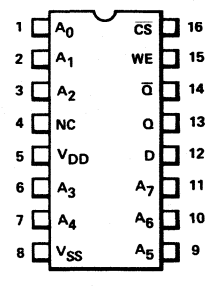


LOGIC SYMBOL



V_{DD} = Pin 5
V_{SS} = Pin 8
NC = Pin 4

CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

$\overline{CS}$	Chip Select Input (Active LOW)
WE	Write Enable Input
D	Data Input
A_0-A_7	Address Inputs
Q	3-State Output (Active HIGH)
$\overline{Q}$	3-State Output (Active LOW)

NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current, HIGH	XC			0.5			1.0		0.2		μA	MIN, 25°C	Output Returned to V_{DD}, $\overline{CS}$ = V_{DD}
					30.0			60.0		12			MAX	
		XM			0.05			0.1		0.02			MIN, 25°C	
					3.0			6.0		1.2			MAX	
I_{OZL}	Output OFF Current, LOW	XC			−0.5			−1.0		−0.2		μA	MIN, 25°C	Output Returned to V_{SS}, $\overline{CS}$ = V_{DD}
					−30.0			−60.0		−12			MAX	
		XM			−0.05			−0.1		−0.02			MIN, 25°C	
					−3.0			−6.0		−1.2			MAX	
I_{DD}	Quiescent Power Supply Current	XC		20			40			8		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
				280			560			112			MAX	
		XM		10			20			4		μA	MIN, 25°C	
				140			280			56			MAX	

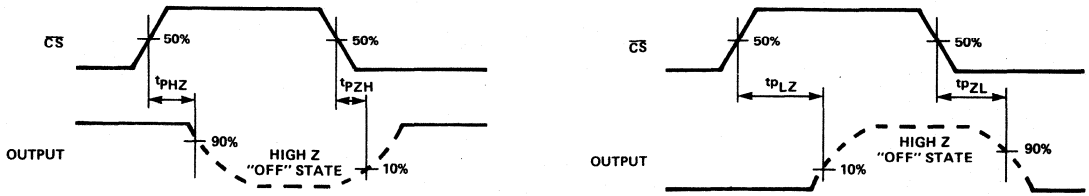
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
	READ MODE											C_L = 15 pF
t_{PLH}	Propagation Delay,		200			100			75		ns	Input Transition
t_{PHL}	Address to Output		200			100			75			Times ≤ 20 ns
t_{PZH}	Enable Time, $\overline{CS}$ to Output		125			60			40		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}			125			60			40			R_L = 1 kΩ to V_{DD}
t_{PHZ}	Disable Time $\overline{CS}$ to Output		125			60			40		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}			125			60			40			R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition Time		40			20			15		ns	
t_{THL}			40			20			15			
	WRITE MODE											
t_{PLH}	Propagation Delay,		125			60			40		ns	
t_{PHL}	WE to Output		125			60			40			
	READ MODE											C_L = 50 pF
t_{PLH}	Propagation Delay,		250			125			100		ns	Input Transition
t_{PHL}	Address to Output		250			125			100			Times ≤ 20 ns
t_{PZH}	Enable Time, $\overline{CS}$ to Output		150			70			50		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}			150			70			50			R_L = 1 kΩ to V_{DD}
t_{PHZ}	Disable Time, $\overline{CS}$ to Output		150			70			50		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}			150			70			50			R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition Time		75			35			25		ns	
t_{THL}			75			35			25			
	WRITE MODE											
t_{PLH}	Propagation Delay,		150			70			50		ns	
t_{PHL}	WE to Output		150			70			50			
	WRITE MODE											C_L = 15 pF
t_wWE	Minimum WE Pulse Width		100			80			60		ns	Input Transition
t_s	Set-Up Time, D to WE		50			20			15		ns	Times ≤ 20 ns
t_h	Hold Time, D to WE		40			20			15			
t_s	Set-Up Time, Address to WE		50			20			15		ns	
t_h	Hold Time, Address to WE		40			20			15			
t_s	Set-Up Time, $\overline{CS}$ to WE		50			20			15		ns	
t_h	Hold Time, $\overline{CS}$ to WE		40			20			15			

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

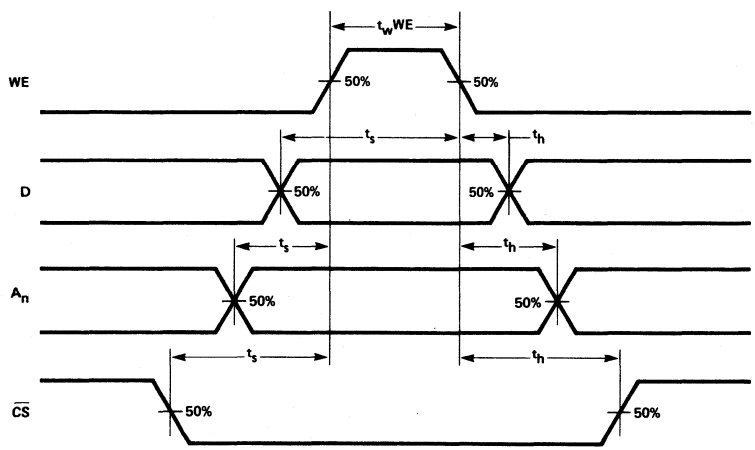
SWITCHING WAVEFORMS

READ MODE



$\overline{CS}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



MINIMUM PULSE WIDTH FOR WE AND SET-UP AND HOLD TIMES,
D TO WE, A_n TO WE, AND $\overline{CS}$ TO WE

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

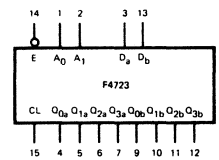
F4723/34723
DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION – The F4723 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address Inputs (A_0, A_1), an active LOW Enable Input ($\overline{E}$) and an active HIGH Clear Input (CL). Each latch has a Data Input (D) and four Outputs (Q_0-Q_3).

When the Enable ($\overline{E}$) and Clear (CL) Inputs are HIGH, all Outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the Clear Input (CL) is HIGH and the Enable Input ($\overline{E}$) is LOW.

When the Clear (CL) and Enable ($\overline{E}$) inputs are LOW, the selected Output (Q_0-Q_3), determined by the Address Inputs (A_0, A_1), follows the Data Input (D). When the Enable Input ($\overline{E}$) goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of the address (A_0, A_1) could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

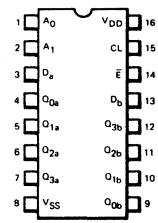
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **SERIAL-TO-PARALLEL CAPABILITY**
- **OUTPUT FROM EACH STORAGE BIT IS AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DECODING OR DEMULTIPLEXING CAPABILITY**
- **EASILY EXPANDABLE**
- **ACTIVE HIGH COMMON CLEAR**

CONNECTION DIAGRAM
DIP (TOP VIEW)

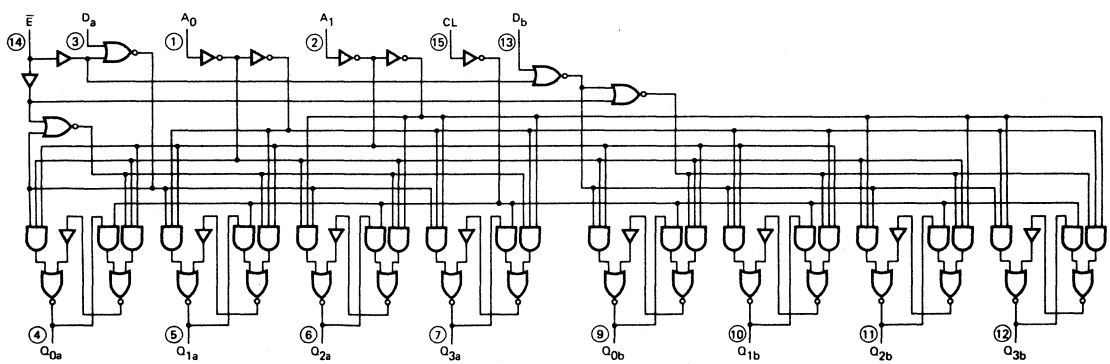


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

A_0, A_1	Address Inputs
D_a, D_b	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
CL	Clear Input (Active HIGH)
Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}	Parallel Latch Outputs

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Numbers

MODE SELECTION

$\overline{E}$	CL	MODE
L	L	Addressable Latch
H	L	Memory
L	H	Dual 4-Channel Demultiplexer
H	H	Clear

H = HIGH Level
L = LOW Level

TRUTH TABLE

CL	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
H	H	X	X	X	L	L	L	L	Clear
H	L	L	L	L	L	L	L	L	Demultiplex
H	L	H	L	L	H	L	L	L	
H	L	L	H	L	L	L	L	L	
H	L	H	H	L	L	H	L	L	
H	L	L	L	H	L	L	L	L	
H	L	H	L	H	L	L	H	L	
H	L	L	H	H	L	L	L	L	
H	L	H	H	H	L	L	L	H	
L	H	X	X	X	Q_{N-1}	Q_{N-1}	Q_{N-1}	Q_{N-1}	Memory
L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}	Addressable
L	L	H	L	L	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	Latch
L	L	L	H	L	Q_{N-1}	L	Q_{N-1}	Q_{N-1}	
L	L	H	H	L	Q_{N-1}	H	Q_{N-1}	Q_{N-1}	
L	L	L	L	H	Q_{N-1}	Q_{N-1}	L	Q_{N-1}	
L	L	H	L	H	Q_{N-1}	Q_{N-1}	H	Q_{N-1}	
L	L	L	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	L	
L	L	H	H	H	Q_{N-1}	Q_{N-1}	Q_{N-1}	H	

L = LOW Level
H = HIGH Level
X = Don't Care
Q_{N-1} = State before the positive transition of the Enable Input

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					100			200		40			MAX	
		XM			1			2		0.4		µA	MIN, 25°C	
					15			30		6			MAX	

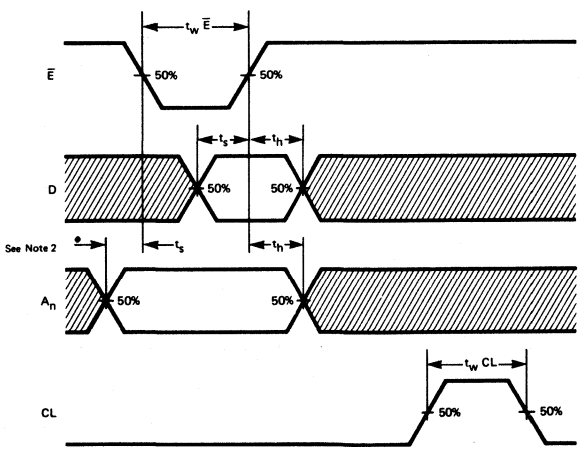
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to Q_n		90 90			40 40			30 30		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		75 75			35 35			25 25		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		100 100			45 45			35 35		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		75			35			25		ns	
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{E}$ to Q_n		110 100			50 50			35 35		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		95 95			45 45			30 30		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		120 120			55 55			40 40		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		95			45			30		ns	
t_{TLH} t_{THL}	Output Transition Time		75 75			40 40			25 25		ns ns	
t_s t_h	Set-Up Time, D to $\overline{E}$ Hold Time, D to $\overline{E}$		30 40			10 20			5 20		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_s t_h	Set-Up Time, Address to $\overline{E}$ Hold Time, Address to $\overline{E}$		30 40			10 20			5 20		ns ns	
$t_w\overline{E}$	Minimum $\overline{E}$ Pulse Width		50			20			15		ns	
t_wCL	Minimum CL Pulse Width		50			20			15		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with output load capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTH FOR $\overline{E}$ AND CL AND SET-UP AND HOLD TIMES, D TO $\overline{E}$ AND A_n TO $\overline{E}$

NOTES:
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.
2. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

F4724/34724
8-BIT ADDRESSABLE LATCH

ESCRIPTION – The F4724 is an 8-Bit Addressable Latch with three Address Inputs (A_0–A_2), a ıta Input (D), an active LOW Enable Input (E), an active HIGH Clear Input (CL) and eight Parallel ıtch Outputs (Q_0–Q_7).

hen the Enable ($\overline{E}$) and the Clear (CL) Inputs are HIGH, all Outputs (Q_0-Q_7) are LOW. Eight- ıannel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when e Clear Input (CL) is HIGH and the Enable Input ($\overline{E}$) is LOW.

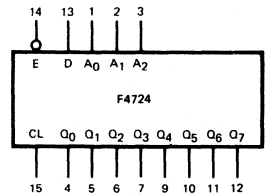
hen the Clear (CL) and Enable ($\overline{E}$) Inputs are LOW, the selected Output (Q_0-Q_7) (determined by the ldress Inputs A_0-A_2) follows the Data Input (D). When the Enable Input ($\overline{E}$) goes HIGH, the ıntents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), anging more than one bit of the address (A_0-A_2) could impose a transient wrong address. Therefore, is should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).

SERIAL-TO-PARALLEL CAPABILITY
EIGHT BITS OF STORAGE WITH THE OUTPUT OF EACH BIT AVAILABLE
RANDOM (ADDRESSABLE) DATA ENTRY
ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY
EASILY EXPANDABLE
COMMON ACTIVE HIGH CLEAR

N NAMES

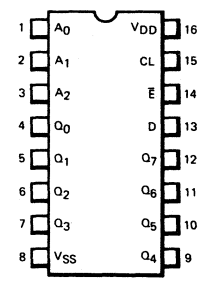
ɔ-A_2	Address Inputs
	Data Input
	Enable Input (Active LOW)
-	Clear Input (Active HIGH)
ɔ-Q_7	Parallel Latch Outputs

LOGIC SYMBOL



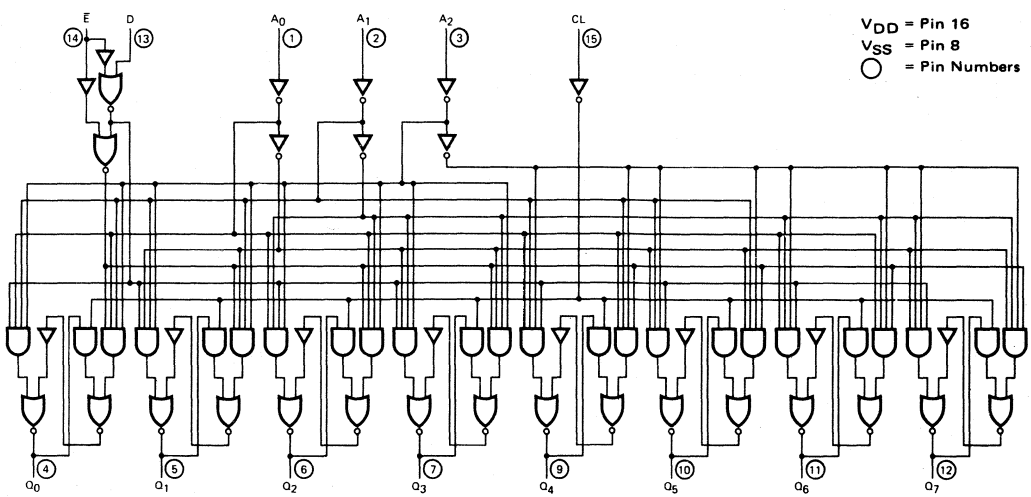
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

MODE SELECTION

$\overline{E}$	CL	MODE
L	L	Addressable Latch
H	L	Memory
L	H	Active HIGH 8-Channel Demultiplexer
H	H	Clear

L = LOW Level
H = HIGH Level
Q_{N-1} = State Before the Positive Transition of the Enable Input

TRUTH TABLE

						PRESENT OUTPUT STATES								
CL	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
H	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
H	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
H	L	H	L	L	L	H	L	L	L	L	L	L	L	
H	L	L	H	L	L	L	L	L	L	L	L	L	L	
H	L	H	H	L	L	L	H	L	L	L	L	L	L	
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
H	L	H	H	H	H	L	L	L	L	L	L	L	H	
L	H	X	X	X	X	Q_{N-1} →								MEMORY
L	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
L	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮						
L	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
L	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			10			20		4		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					100			200		40			MAX	
		XM			1			2		0.4		μA	MIN, 25°C	
					15			30		6			MAX	

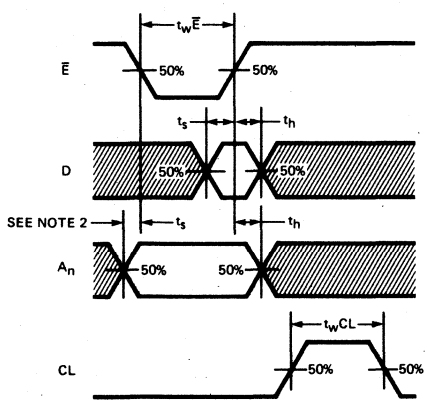
Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, $\bar{E}$ to Q_n		90 90			40 40			30 30		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		75 75			35 35			25 25		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		100 100			45 45			35 35		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		75			35			25		ns	
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, $\bar{E}$ to Q_n		110 110			50 50			35 35		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, D to Q_n		95 95			45 45			30 30		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, Address to Q_n		120 120			55 55			40 40		ns ns	
t_{PHL}	Propagation Delay, CL to Q_n		95			45			30		ns	
t_{TLH} t_{THL}	Output Transition Time		75 75			40 40			25 25		ns ns	
t_s t_h	Set-Up Time, D to $\bar{E}$ Hold Time, D to $\bar{E}$		30 40			10 20			5 20		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_s t_h	Set-Up Time, Address to $\bar{E}$ Hold Time, Address to $\bar{E}$		30 40			10 20			5 20		ns ns	
$t_w\bar{E}$	Minimum $\bar{E}$ Pulse Width		50			20			15		ns	
t_wCL	Minimum CL Pulse Width		50			20			15		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTH FOR $\bar{E}$ AND CL AND SET-UP AND HOLD TIMES, D TO $\bar{E}$ AND A_n TO $\bar{E}$

NOTES:
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.
2. The Address to Enable Set-up Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

F4725/34725

64-BIT (16×4) RANDOM ACCESS MEMORY WITH 3-STATE OUTPUTS

DESCRIPTION – The F4725 is a 64-Bit Random Access Memory with 3-State Outputs organized as 16 words by four bits with four Data Inputs (D_0-D_3), four Address Inputs (A_0-A_3), an active LOW Write Enable Input ($\overline{WE}$), an active LOW Chip Select Input ($\overline{CS}$) and four active LOW 3-State Outputs ($\overline{Q}_0$-$\overline{Q}_3$).

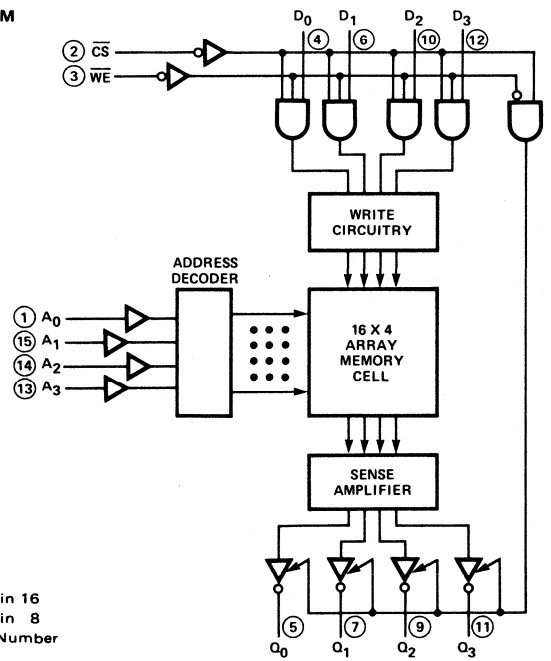
Information on the four Data Inputs (D_0-D_3) is written into the memory location selected by the Address Inputs (A_0-A_3) when both the Chip Select Input ($\overline{CS}$) and the Write Enable Input ($\overline{WE}$) are LOW. Under these conditions, the Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are held in a high impedance OFF state. Information is read from the memory location selected by the Address Inputs (A_0-A_3) while the Chip Select Input ($\overline{CS}$) is LOW and the Write Enable Input ($\overline{WE}$) is HIGH. The Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are the complement of the information written into the memory. When the Chip Select Input ($\overline{CS}$) is HIGH, all Outputs ($\overline{Q}_0$-$\overline{Q}_3$) are held in the high impedance OFF state. This allows other 3-State outputs to be wired together in a bus arrangement. The F4725 offers fully static operation.

- **3-STATE OUTPUTS**
- **ORGANIZATION – 16 WORDS X 4 BITS**
- **ON-CHIP DECODING**
- **INVERTED DATA OUTPUT**
- **FULLY STATIC OPERATION**

MODE SELECTION

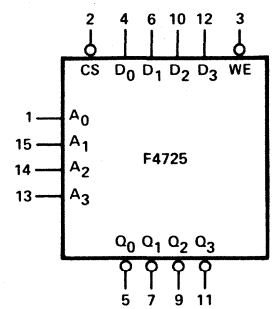
$\overline{CS}$	$\overline{WE}$	OUTPUTS	MODE
L	L	High Impedance	Write
L	H	Outputs are Complement of Data Written into Location	Read
H	X	High Impedance	Inhibit

LOGIC DIAGRAM

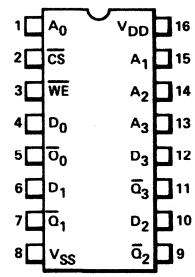


V_{DD} = Pin 16
V_{SS} = Pin 8
O = Pin Number

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{DD} = Pin 16
V_{SS} = Pin 8

NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

$\overline{CS}$	Chip Select Input (Active LOW)
$\overline{WE}$	Write Enable Input (Active LOW)
D_0-D_3	Data Inputs
A_0-A_3	Address Inputs
$\overline{Q}_0$-$\overline{Q}_3$	3-State Outputs (Active LOW)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{OZH}	Output OFF Current HIGH	XC			0.5 30.0			1.0 60.0		0.2 12.0		μA	MIN, 25°C MAX	Output Returned to V_{DD}, $\overline{CS}$ = V_{DD}
		XM			0.05 3.0			0.1 6.0		0.02 1.2			MIN, 25°C MAX	
I_{OZL}	Output OFF Current LOW	XC			−0.5 −30.0			−1.0 −60.0		−0.2 −12.0		μA	MIN, 25°C MAX	Output Returned to V_{SS}, $\overline{CS}$ = V_{DD}
		XM			−0.05 −30.0			−0.1 −6.0		−0.02 −1.2			MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC		2.5 15			5 30			10 60		μA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM		2.5 15			5 30			10 60		μA	MIN, 25°C MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

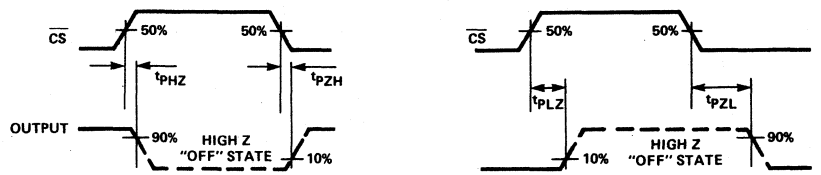
SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
	READ MODE											C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		180 180			70 70			50 50		ns	Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Enable Time, $\overline{CS}$ to Output		135 135			60 60			45 45		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{CS}$ to Output		135 135			60 60			45 45		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		40 40			20 20			15 15		ns	
	WRITE MODE											
t_{PZH} t_{PZL}	Enable Time $\overline{WE}$ to Output		135 135			60 60			45 45		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{WE}$ to Output		135 135			60 60			45 45		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
	READ MODE											C_L = 50 pF
t_{PLH} t_{PHL}	Propagation Delay, Address to Output		200 200			95 95			70 70		ns	Input Transition Times ⩽ 20 ns
t_{PZH} t_{PZL}	Enable Time, $\overline{CS}$ to Output		150 150			70 70			50 50		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{CS}$ to Output		150 150			70 70			50 50		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{TLH} t_{THL}	Output Transition Time		75 75			35 35			25 25		ns	
	WRITE MODE											
t_{PZH} t_{PZL}	Enable Time, $\overline{WE}$ to Output		150 150			70 70			50 50		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
t_{PHZ} t_{PLZ}	Disable Time, $\overline{WE}$ to Output		150 150			70 70			50 50		ns	R_L = 1 kΩ to V_{SS} R_L = 1 kΩ to V_{DD}
	WRITE MODE											
$t_W\overline{WE}$	Minimum $\overline{WE}$ Pulse Width		180			100			80		ns	
t_s t_h	Set-Up Time, D_n to $\overline{WE}$ Hold Time, D_n to $\overline{WE}$		150 40			120 20			115 15		ns	
t_s t_h	Set-Up Time, Address to $\overline{WE}$ Hold Time, Address to $\overline{WE}$		150 40			120 20			115 15		ns	C_L = 15 pF Input Transition Times ⩽ 20 ns
t_s t_h	Set-Up Time, $\overline{CS}$ to $\overline{WE}$ Hold Time, $\overline{CS}$ to $\overline{WE}$		150 40			120 20			115 15		ns	

Notes on following page

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_w) do not vary with load capacitance.

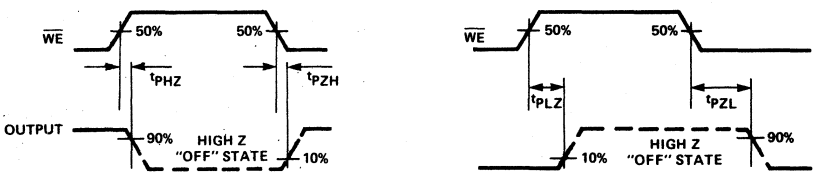
SWITCHING WAVEFORMS

READ MODE

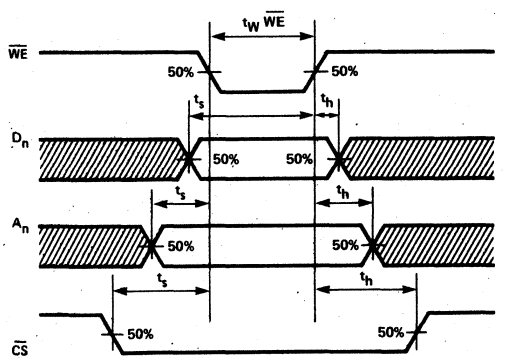


$\overline{CS}$ TO OUTPUT ENABLE AND DISABLE TIMES

WRITE MODE



$\overline{WE}$ TO OUTPUT ENABLE AND DISABLE TIMES



MINIMUM $\overline{WE}$ PULSE WIDTH AND SET-UP AND HOLD TIMES, D_n TO $\overline{WE}$, A_n TO $\overline{WE}$, AND $\overline{CS}$ TO $\overline{WE}$

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4731/34731

QUAD 64-BIT STATIC SHIFT REGISTER

FAIRCHILD CMOS LSI

ESCRIPTION – The F4731 is a Quad 64-Bit Shift Register each with separate Serial Data Inputs (D_A-D_D), Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$) and Data Outputs (Q_{63A}-Q_{63D}) from the 64th register position.

nformation present on the Serial Data Inputs is shifted into the first register position and all the data n the register is shifted one position to the right on a HIGH-to-LOW transition of the Clock Inputs ($\overline{CP}_A$-$\overline{CP}_D$).

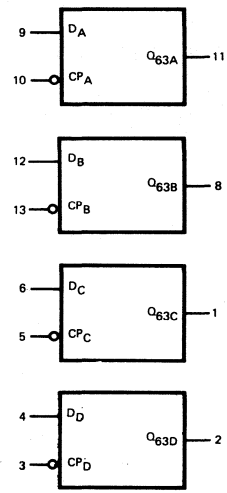
.ow impedance outputs are provided for direct interface to TTL.

- **FREQUENCIES UP TO 4 MHz AT V_{DD} = 10 V**
- **SERIAL-TO-SERIAL DATA TRANSFER**
- **SEPARATE CLOCK INPUTS, DATA INPUTS AND FULLY BUFFERED OUTPUTS FOR EACH REGISTER**
- **DIRECT INTERFACE TO TTL**
- **14-PIN PACKAGE**

'IN NAMES

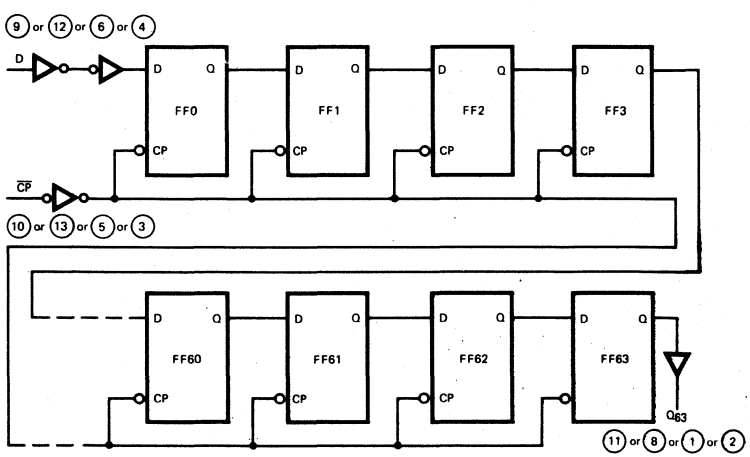
$)_A$-D_D	Serial Data Inputs
$\overline{CP}_A$-$\overline{CP}_D$	Clock Input (H→L Edge-Triggered)
$)_{63A}$-Q_{63D}	Buffered Outputs from the 64th Register Position

LOGIC SYMBOL



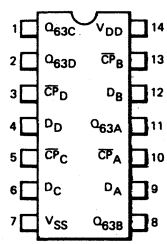
V_{DD} = Pin 14
V_{SS} = Pin 7

LOGIC DIAGRAM
1/4 OF A F4731



V_{DD}= Pin 14
V_{SS} = Pin 7
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

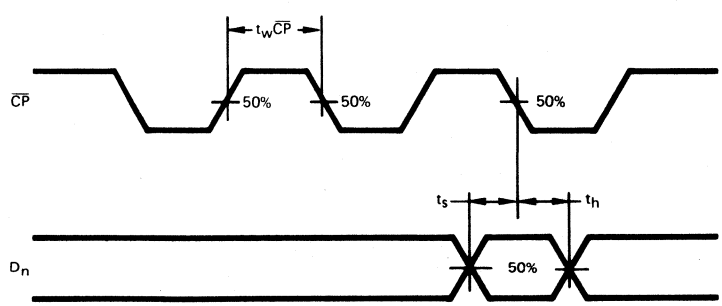
SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC		2.5			5			10		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
				35			70			140			MAX	
		XM		0.25			0.5			1.0		μA	MIN, 25°C	
				15			30			60			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_{63}		175			85			60		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			175			85			60		ns	
t_{TLH}	Output Transition Time		30			20			15		ns	
t_{THL}			30			20			15		ns	
t_{PLH}	Propagation Delay, $\overline{CP}$ to Q_{63}		190			95			65		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			190			95			65		ns	
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20		ns	
$t_W\overline{CP}$	$\overline{CP}$ Minimum Pulse Width		100			50			40		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_s	Set-Up Time D to $\overline{CP}$		75			40			30		ns	
t_h	Hold Time D to $\overline{CP}$		40			20			15		ns	
f_{MAX}	Max. Input Clock Frequency (Note 4)		4			8					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L), Set-up Times (t_s), Hold Times (t_h), and Minimum Pulse Widths (t_W), do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM CLOCK PULSE WIDTH AND SET-UP AND HOLD TIMES, D TO $\overline{CP}$

NOTE:
1. Set-up and Hold Times are shown as positive values but may be specified as negative values.

F4734/34734

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER WITH RIPPLE BLANKING

:SCRIPTION – The F4734 is a BCD-to-7 Segment Latch/Decoder/Driver with Ripple Blanking. It ; four Address Inputs (A_0–A_3), an active LOW Latch Enable Input ($\overline{EL}$), an active LOW Blanking ɔut ($\overline{I_B}$), an active LOW Lamp Test Input ($\overline{I_{LT}}$), a Ripple Blanking Input (I_{RB}), a Ripple Blanking ıtput (O_{RB}) and seven active HIGH NPN bipolar Segment Outputs (a-g).

ıen the Lamp Test Input ($\overline{I_{LT}}$) is LOW, all the Segment Outputs (a-g) are HIGH; independent of all ıer input conditions. The Lamp Test Input ($\overline{I_{LT}}$) does not affect the Ripple Blanking Output $_{RB}$). With the Lamp Test Input ($\overline{I_{LT}}$) HIGH, a LOW on the Blanking Input ($\overline{I_B}$) forces the Segment ıtputs (a-g) LOW; independent of all other input conditions. The Blanking Input ($\overline{I_B}$) does not affect ; Ripple Blanking Output (O_{RB}). The Ripple Blanking Output (O_{RB}) is HIGH when the Ripple ınking Input (I_{RB}) is HIGH and the latch contains binary zero. With the Lamp Test Input ($\overline{I_{LT}}$) GH, the display is blank when the Ripple Blank Output (O_{RB}) is HIGH.

ıen the Latch Enable Input ($\overline{EL}$) is LOW, the state of the latch is determined by the data on the ldress Inputs (A_0–A_3). When the Latch Enable Input ($\overline{EL}$) goes HIGH, the last data present at the ldress Inputs (A_0–A_3) is stored in the latch. The Lamp Test ($\overline{I_{LT}}$), Blanking ($\overline{I_B}$) and Ripple ınking (I_{RB}) inputs do not affect the latch circuit.

HIGH CURRENT SOURCING OUTPUTS (UP TO 25 mA)
BLANKING INPUT (ACTIVE LOW)
LAMP TEST INPUT (ACTIVE LOW)
LAMP INTENSITY MODULATION CAPABILITY
MULTIPLEXING CAPABILITY
RIPPLE BLANKING INPUT/OUTPUT

N NAMES

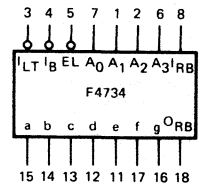
)–A_3	Address (Data) Inputs	$\overline{I_{LT}}$	Lamp Test Input (Active LOW)
	Latch Enalbe Input (Active LOW)	I_{RB}	Ripple Blanking Input
	Blanking Input (Active LOW)	O_{RB}	Ripple Blanking Output
		a–g	Segment Outputs

TRUTH TABLE

INPUTS				OUTPUTS							
A_3	A_2	A_1	A_0	a	b	c	d	e	f	g	DISPLAY
X	X	X	X	H	H	H	H	H	H	H	8
X	X	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	L	H	H	H	H	H	H	L	0
L	L	L	H	L	H	H	L	L	L	L	1
L	L	H	L	H	H	L	H	H	L	H	2
L	L	H	H	H	H	H	H	L	L	H	3
L	H	L	L	L	H	H	L	L	H	H	4
L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	L	H	H	H	H	H	6
L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	H	H	H	H	L	H	H	9
H	L	H	L	L	L	L	L	L	L	L	BLANK
H	L	H	H	L	L	L	L	L	L	L	BLANK
H	H	L	L	L	L	L	L	L	L	L	BLANK
H	H	L	H	L	L	L	L	L	L	L	BLANK
H	H	H	L	L	L	L	L	L	L	L	BLANK
H	H	H	H	L	L	L	L	L	L	L	BLANK

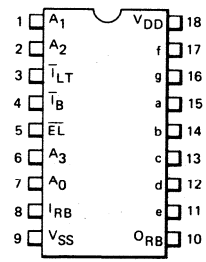
)NDITIONS:
. = LOW, $\overline{I_B}$ = HIGH,
.T = HIGH, and I_{RB} = LOW

LOGIC SYMBOL

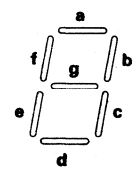


V_{DD} = Pin 18
V_{SS} = Pin 9

CONNECTION DIAGRAM DIP (TOP VIEW)



NUMERICAL DESIGNATIONS



F40085/340085

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION – The F40085 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3,B_0-B_3); A_3,B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

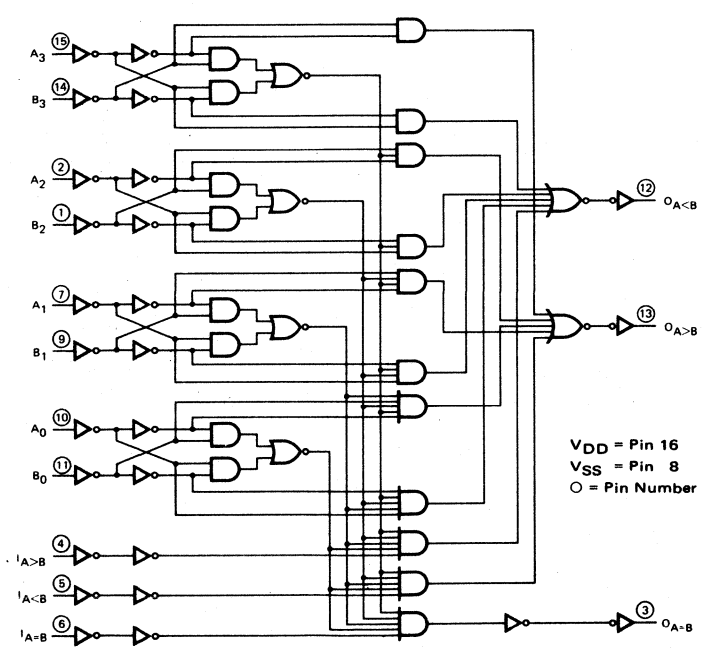
The Truth Table on the following page describes the operation of the F40085 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

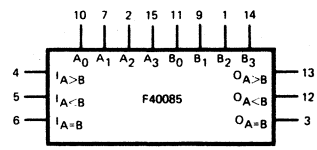
PIN NAMES

A_0-A_3	Word A Parallel Inputs
B_0-B_3	Word B Parallel Inputs
$I_{A>B}$, $I_{A<B}$, $I_{A=B}$	Expander Inputs
$O_{A>B}$	A Greater than B Output
$O_{A<B}$	A Less than B Output
$O_{A=B}$	A Equal to B Output

LOGIC DIAGRAM

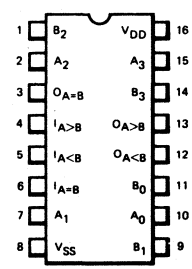


LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	H	L	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	H	H	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	H	H	H	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	H	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	L	L	L

H = HIGH Level
L = LOW Level
X = Don't Care

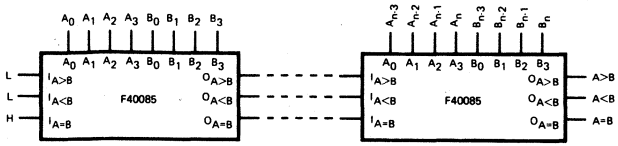
DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		µA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
					700			1400		280				
		XM			5			10		2		µA	MIN, 25°C MAX	
					300			600		120				

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, A_n or B_n to any Output		160			65			45		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			160			65			45		ns	
t_{PLH}	Propagation Delay, Any I to any Output		115			45			30		ns	
t_{PHL}			115			45			30		ns	
t_{TLH}	Output Transition Time		30			17			13		ns	
t_{THL}			30			17			13		ns	
t_{PLH}	Propagation Delay, A_n or B_n to any Output		180			70			50		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			180			70			50		ns	
t_{PLH}	Propagation Delay, Any I to any Output		135			55			40		ns	
t_{PHL}			135			55			40		ns	
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.



L = LOW Level
H = HIGH Level

Fig. 1. COMPARING TWO n-BIT WORDS

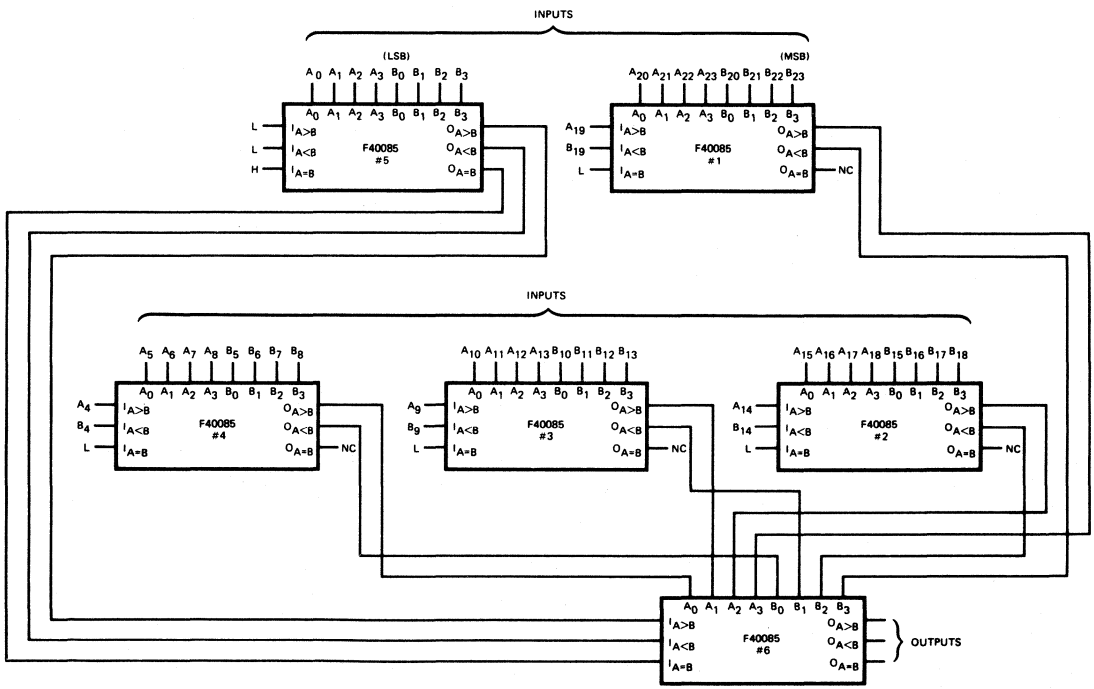
APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE:
The F40085 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another F40085 as shown in Figure 2 in positions #1, 2, 3, and 4.



MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

F40097/340097 · F40098/340098

3-STATE HEX NON-INVERTING AND INVERTING BUFFERS

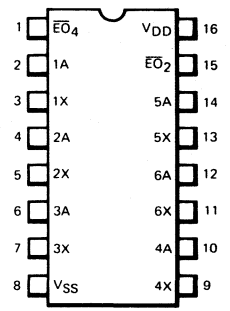
ESCRIPTION – These two CMOS buffers provide high current output capability suitable for driving gh capacitance loads. The F40097 is a Non-Inverting CMOS Buffer with 3-state outputs and the 40098 is an Inverting CMOS Buffer with 3-state outputs. The 3-state outputs of each device are ntrolled by two Enable Inputs ($\overline{EO}_4$, $\overline{EO}_2$). A HIGH on Enable Input $\overline{EO}_4$ causes the Outputs of ur of the six buffer elements to assume a high impedance or OFF state, regardless of other input nditions and a HIGH on Enable Input $\overline{EO}_2$ causes the Outputs of the remaining two buffer elements assume a high impedance or OFF state, regardless of other input conditions.

3-STATE OUTPUTS
TTL COMPATIBLE – FAN OUT OF ONE TTL LOAD
ACTIVE LOW ENABLE INPUTS

N NAMES

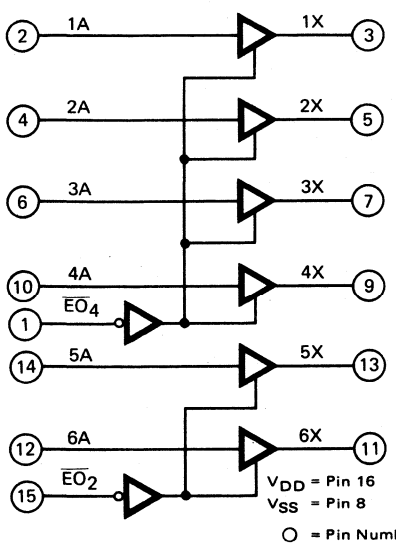
-6A	Buffer Inputs
$\overline{O}_4$, $\overline{EO}_2$	Enable Inputs (Active LOW)
X-6X	Buffer Outputs (Active HIGH for the 340097 and Active LOW for the 340098)

CONNECTION DIAGRAM
DIP (TOP VIEW)

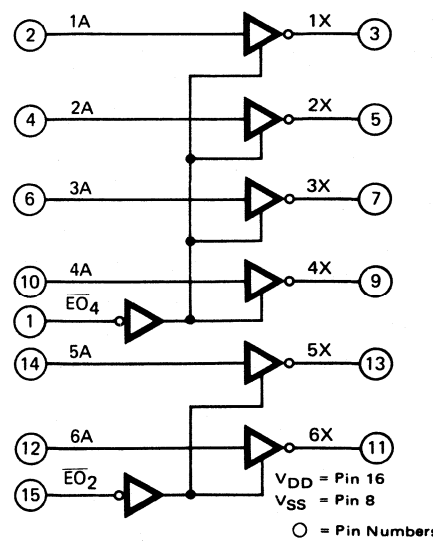


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F40097 LOGIC DIAGRAM



F40098 LOGIC DIAGRAM



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
$I_{SC(H)}$	Output Short Circuit Current		-4.35			-20						mA	All	$V_{IN} = V_{DD}$ or V_{SS} per Function, $V_{OUT} = V_{SS}$
$I_{SC(L)}$	Output Short Circuit Current		4.35			20						mA	All	$V_{IN} = V_{DD}$ or V_{SS} per Function, $V_{OUT} = V_{DD}$
I_{OH}	Output HIGH Current		-1.6 Note 2									mA	All	V_{OUT} = 2.4 V, Inputs at 0 V or V_{DD} per Function
I_{OL}	Output LOW Current		1.6 Note 2									mA	All	V_{OUT} = 0.4 V, Inputs at 0 V or V_{DD} per Function
I_{OZH}	Output OFF Current HIGH	XC			0.5 7			0.5 7			0.5 7	µA	MIN, 25°C MAX	Output Returned to V_{DD}, $\overline{EO}_n = V_{DD}$
		XM			0.05 3			0.05 3			0.05 3		MIN, 25°C MAX	
I_{OZL}	Output OFF Current LOW	XC			-0.5 -7			-0.5 -7			-0.5 -7	µA	MIN, 25°C MAX	Output Returned to V_{SS}, $\overline{EO}_n = V_{DD}$
		XM			-0.05 -3			-0.05 -3			-0.05 -3		MIN, 25°C MAX	
I_{DD}	Quiescent Power Supply Current	XC			3 42			5 70		1 14		µA	MIN, 25°C MAX	All inputs common and at 0 V or V_{DD}
		XM			0.3 20			0.5 30		0.1 6		µA	MIN, 25°C MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 25°C, F40097 only (See Note 3)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay,		40	65		20	35		18		ns	C_L = 15 pF
t_{PHL}	Data to Output		55	85		25	35		18		ns	Input Transition Times ⩽ 20 ns
t_{PZH}	Output Enable		60	95		30	50		25		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		85	135		35	55		28		ns	R_L = 1 kΩ to V_{DD}
t_{PHZ}	Output Disable		35	50		28	50		25		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		55	83		33	50		27		ns	R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition		25	45		12	25		10	20	ns	
t_{THL}	Time		20	35		10	25		10	20	ns	
t_{PLH}	Propagation Delay,		65	100		25	40		20		ns	C_L = 50 pF
t_{PHL}	Data to Output		80	100		28	40		20		ns	Input Transition Times ⩽ 20 ns
t_{PZH}	Output Enable		70	110		35	55		29		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		95	150		40	65		30		ns	R_L = 1 kΩ to V_{DD}
t_{PHZ}	Output Disable		40	65		31	55		29		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		60	95		35	55		30		ns	R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition		40	65		25	40		15	30	ns	
t_{THL}	Time		30	60		15	30		15	30	ns	

Notes on following page.

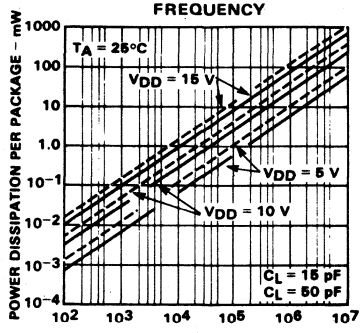
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0V, T_A = 25°C, F40098 only (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		55	105		25	40		25		ns	C_L = 15 pF
t_{PHL}	Data to Output		75	135		33	50		25		ns	Input Transition Times ≤ 20 ns
t_{PZH}	Output Enable		60	100		30	50		25		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		85	145		35	54		28		ns	R_L = 1 kΩ to V_{DD}
t_{PHZ}	Output Disable		35	55		28	50		25		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		55	85		33	50		27		ns	R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition		25	45		12	25		10	20	ns	
t_{THL}	Time		20	35		10	25		10	20	ns	
t_{PLH}	Propagation Delay,		65	120		30	55		30		ns	C_L = 50 pF
t_{PHL}	Data to Output		85	155		35	65		30		ns	Input Transition Times ≤ 20 ns
t_{PZH}	Output Enable		70	110		35	55		29		ns	R_L = 1 kΩ to V_{SS}
t_{PZL}	Time		95	170		40	60		30		ns	R_L = 1 kΩ to V_{DD}
t_{PHZ}	Outside Disable		40	70		31	55		29		ns	R_L = 1 kΩ to V_{SS}
t_{PLZ}	Time		60	105		35	55		30		ns	R_L = 1 kΩ to V_{DD}
t_{TLH}	Output Transition		40	65		25	40		15	30	ns	
t_{THL}	Time		30	60		15	30		15	30	ns	

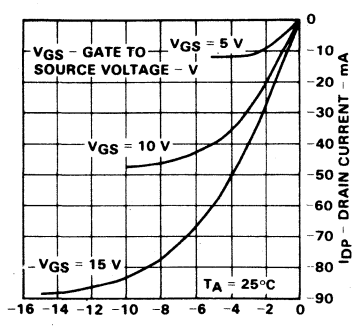
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. For I_{OH} and I_{OL} tests, V_{DD} = 4.5V for military grade product and V_{DD} = 4.75V for commercial grade product.
3. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

TYPICAL ELECTRICAL CHARACTERISTICS

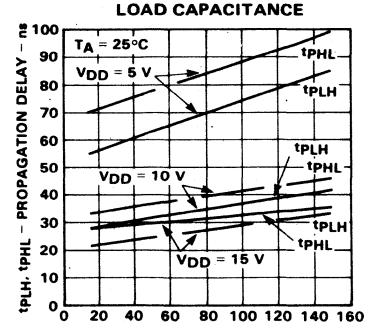
F40097/F40098
POWER DISSIPATION VERSUS FREQUENCY



F40097/F40098
P-CHANNEL DRAIN CHARACTERISTICS

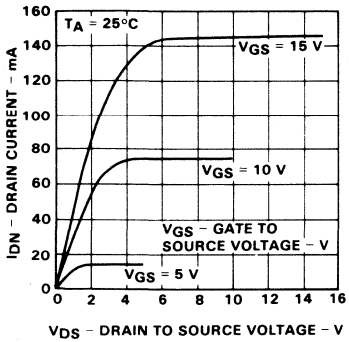


F40098
PROPAGATION DELAY VERSUS LOAD CAPACITANCE

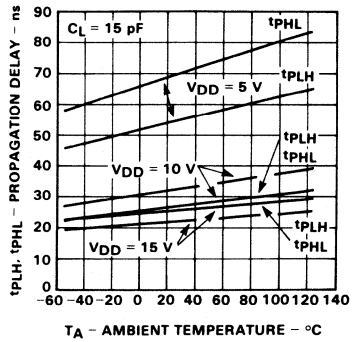


TYPICAL ELECTRICAL CHARACTERISTICS (Cont'd)

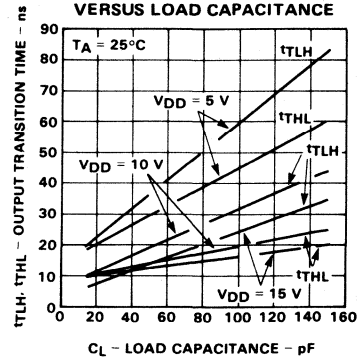
F40098
N-CHANNEL DRAIN CHARACTERISTICS



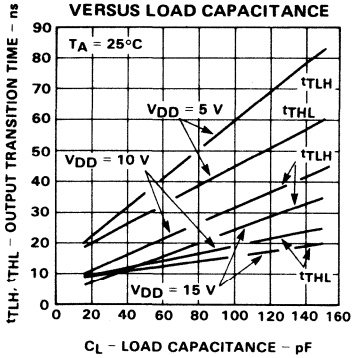
F40098
PROPAGATION DELAY VERSUS TEMPERATURE



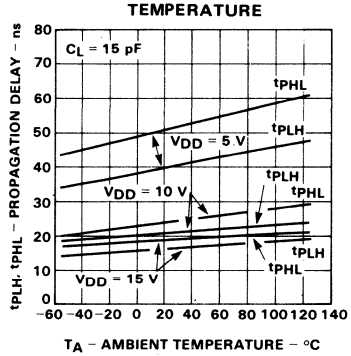
F40098
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



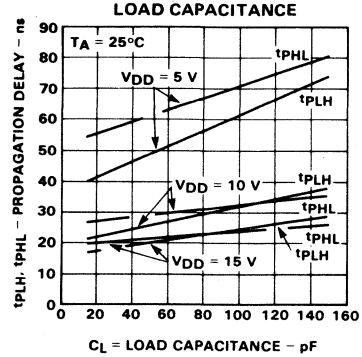
F40097
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



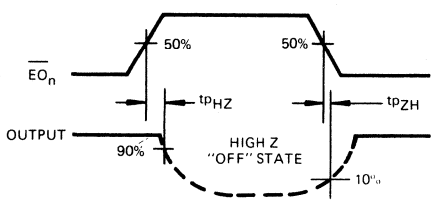
F40097
PROPAGATION DELAY VERSUS TEMPERATURE



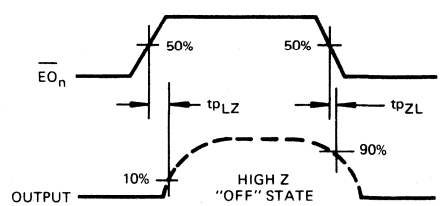
F40097
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORMS



OUTPUT ENABLE TIME
(t_{PZH}) AND OUTPUT DISABLE TIME (t_{PHZ})



OUTPUT ENABLE TIME
(t_{PZL}) AND OUTPUT DISABLE TIME (t_{PLZ})

F40160/340160 • F40161/340161
F40162/340162 • F40163/340163

4-BIT SYNCHRONOUS COUNTERS

DESCRIPTION – The F40160 and the F40162 are fully synchronous edge-triggered 4-Bit Decade Counters. The F40161 and the F40163 are fully synchronous edge-triggered 4-Bit Binary Counters. Each device has a Clock Input (CP); four synchronous Parallel Data Inputs (P_0-P_3); three synchronous Mode Control Inputs, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable trickle (CET); Buffered Outputs from all four bit positions (Q_0-Q_3); and a Terminal Count Output (TC). The F40162 and F40163 have an additional synchronous Mode Control Input, Synchronous Reset ($\overline{SR}$). Alternately, the F40160 and F40161 have an overriding asynchronous Master Reset ($\overline{MR}$).

Operation is fully synchronous (except for Master Reset on the F40160 and F40161 and occurs on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input ($\overline{PE}$) is LOW, the next LOW-to-HIGH transition of the Clock Input (CP) loads data into the counter from Parallel Inputs (P_0-P_3). When the Parallel Enable Input ($\overline{PE}$) is HIGH, the next LOW-to-HIGH transition of the Clock Input (CP) advances the counter to its next state only if both Count Enable Inputs (CEP and CET) are HIGH; otherwise, no change occurs in the state of the counter. The Terminal Count Output (TC) is HIGH when the state of the counter is nine (Q_0= Q_3 = HIGH, Q_1 = Q_2 = LOW) for the F40160 and F40162/fifteen (Q_0 = Q_1 = Q_2 = Q_3 = HIGH) for the F40161 and F40163 and the Count Enable Trickle Input (CET) is HIGH. For the F40162 and F40163, a LOW on the Synchronous Reset Input ($\overline{SR}$) sets all Outputs (Q_0-Q_3 and TC) LOW on the next LOW-to-HIGH transition of the Clock Input (CP) independent of the state of all other synchronous Mode Control Inputs (CEP, CET, $\overline{PE}$). For the F40160 and F40161, a LOW on the overriding asynchronous Master Reset ($\overline{MR}$) sets all outputs (Q_0-Q_3 and TC) LOW, independent of the state of all other inputs.

These devices perform multistage synchronous counting without additional components by using a carry look-ahead counting technique.

The F40160, F40161, F40162, and F40163 are edge-triggered; therefore, the synchronous Mode Control Input (CEP, CET, $\overline{PE}$ for the F40160/F40161 and CEP, CET, $\overline{PE}$, $\overline{SR}$ for the F40162/F40163) must be stable only during the set-up time before the LOW-to-HIGH transition of the Clock Input (CP).

- **12 MHz TYPICAL COUNT FREQUENCY AT V_{DD} = 10 V**
- **DECODED TERMINAL COUNT**
- **FULLY SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **SYNCHRONOUS (F40162/F40163) OR ASYNCHRONOUS (F40160/F40161) RESET**
- **BUILT-IN CARRY CIRCUITRY**
- **FULLY EDGE-TRIGGERED**

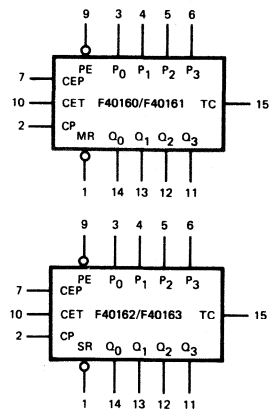
PIN NAMES

$\overline{PE}$	Parallel Enable Input (Active LOW)
P_0-P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW) for the F40160/F40161 Only
$\overline{SR}$	Synchronous Reset Input (Active LOW) for the F40162/F40163 Only
Q_0-Q_3	Parallel Outputs
TC	Terminal Count Output

SELECTOR GUIDE

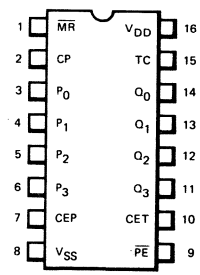
RESET	MODULUS	
	DECADE	BINARY
Asynchronous	F40160	F40161
Synchronous	F40162	F40163

LOGIC SYMBOL

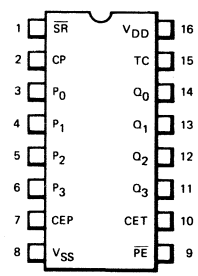


V_{DD} = Pin 16
V_{SS} = Pin 8

F40160/F40161
CONNECTION DIAGRAM
DIP (TOP VIEW)



F40162/F40163
CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

SYNCHRONOUS MODE SELECTION
F40160/F40161

$\overline{PE}$	CEP	CET	MODE
L	X	X	Preset
H	L	X	No Change
H	X	L	No Change
H	H	H	Count

$\overline{MR}$ = HIGH

SYNCHRONOUS MODE SELECTION
F40162/F40163

$\overline{SR}$	$\overline{PE}$	CEP	CET	MODE
H	L	X	X	Preset
H	H	L	X	No Change
H	H	X	L	No Change
H	H	H	H	Count
L	X	X	X	Reset

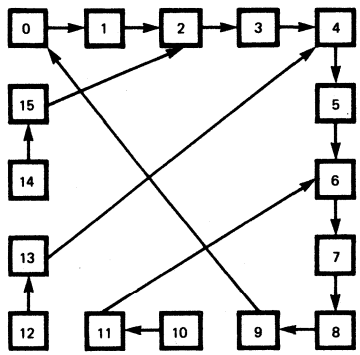
TERMINAL COUNT GENERATION

CET	F40160/F40162 $(Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3)$	F40161/F40163 $(Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3)$	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

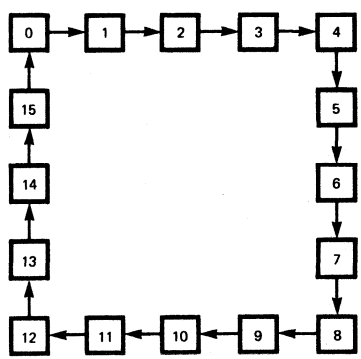
$TC = CET \cdot Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$ (F40160/F40162)
$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$ (F40161/F40163)

H = HIGH Level
L = LOW Level
X = Don't Care

STATE DIAGRAM
F40160 • F40162



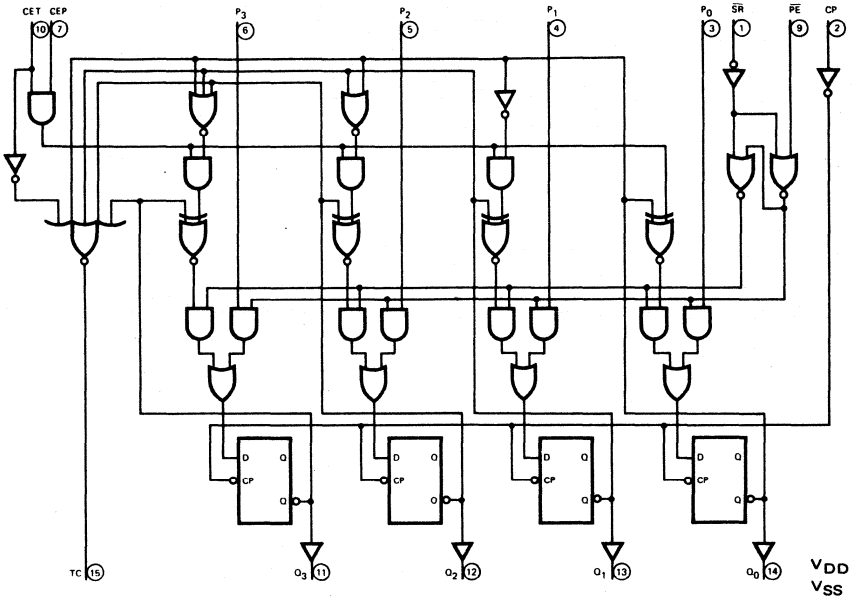
STATE DIAGRAM
F40161 • F40163



NOTE:
The F40160 or F40162 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, they will return to their normal sequence within two clock pulses.

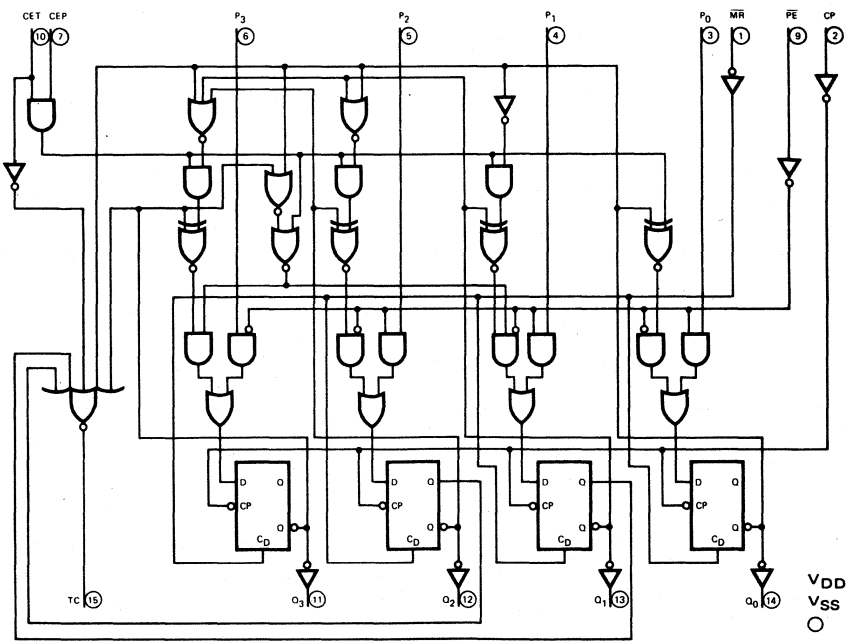
F40161/F40163 LOGIC DIAGRAM

The F40161 and F40163 binary synchronous counters are similar. However, the F40161 has an asynchronous master reset circuit as shown on the F40160/F40162 Logic Diagram.



F40160/F40162 LOGIC DIAGRAM

The F40160 and F40162 BCD synchronous counters are similar. However, the F40162 has a synchronous reset circuit as shown on the F40161/F40163 Logic Diagram.



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			100			200		40		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			20			40		8		µA	MIN, 25°C	
					300			600		120			MAX	

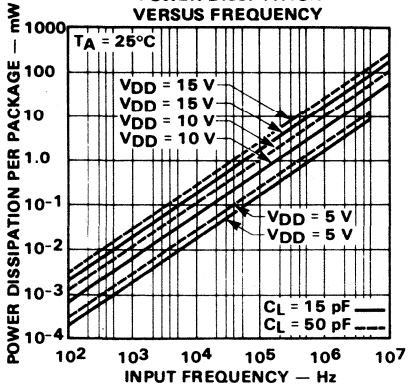
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q		95	185		50	90		33		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			95	185		50	90		35		ns	
t_{PLH}	Propagation Delay, CP to TC		130	250		60	115		37		ns	
t_{PHL}			130	250		60	115		37		ns	
t_{PLH}	Propagation Delay, CET to TC		70	130		32	65		20		ns	
t_{PHL}			75	130		45	80		30		ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		128	250		55	110		37		ns	(F40160/F40161)
t_{PHL}	Propagation Delay, $\overline{MR}$ to TC		153	300		65	130		45		ns	(F40160/F40161)
t_{TLH}	Output Transition Time		35	75		20	40		15	25	ns	
t_{THL}			40	75		20	40		15	25	ns	
t_{PLH}	Propagation Delay, CP to Q		120	220		55	105		40		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			120	220		55	105		38		ns	
t_{PLH}	Propagation Delay, CP to TC		155	285		70	130		45		ns	
t_{PHL}			155	285		70	130		40		ns	
t_{PLH}	Propagation Delay, CET to TC		95	165		40	80		27		ns	
t_{PHL}			95	165		55	95		36		ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		150	285		65	125		44		ns	(F40160/F40161)
t_{PHL}	Propagation Delay, $\overline{MR}$ to TC		175	335		75	145		52		ns	(F40160/F40161)
t_{TLH}	Output Transition Time		60	135		35	70		25	45	ns	
t_{THL}			70	135		30	70		23	45	ns	
t_{rec}	$\overline{MR}$ Recovery Time	50	15		30	10			7		ns	(F40160/F40161)
$t_w\overline{MR}(L)$	$\overline{MR}$ Minimum Pulse Width	110	60		55	27			17		ns	(F40160/F40161)
t_wCP	CP Minimum Pulse Width	90	50		40	20			15		ns	
t_s	Set-Up Time, Data to CP	70	35		35	18			13		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_h	Hold Time, Data to CP	0	-30		0	-15			-10		ns	
t_s	Set-Up Time, $\overline{PE}$ to CP	110	60		60	30			20		ns	
t_h	Hold Time, $\overline{PE}$ to CP	-10	-57		-5	-28			-18		ns	
t_s	Set-Up Time, CEP, CET to CP	200	115		95	50			35		ns	
t_h	Hold Time, CEP, CET to CP	-20	-110		-10	-48			-32		ns	
t_s	Set-Up Time, $\overline{SR}$ to CP	40	15		18	15			4		ns	(F40162/F40163)
t_h	Hold Time, $\overline{SR}$ to CP	0	-5		0	-2			0		ns	(F40162/F40163)
f_{MAX}	Input Count Frequency (Note 4)	3	6		7	12					MHz	

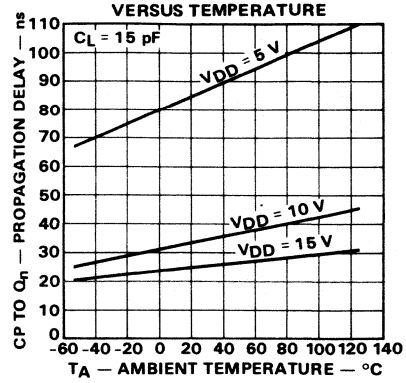
Notes:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 µs.

TYPICAL ELECTRICAL CHARACTERISTICS

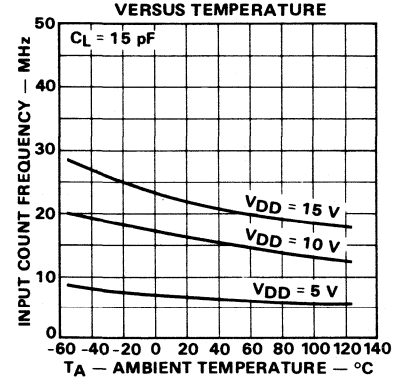
POWER DISSIPATION VERSUS FREQUENCY



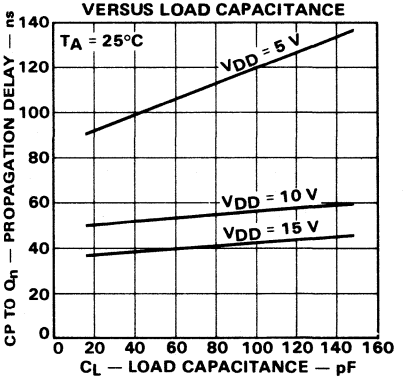
PROPAGATION DELAY VERSUS TEMPERATURE



INPUT COUNT FREQUENCY VERSUS TEMPERATURE

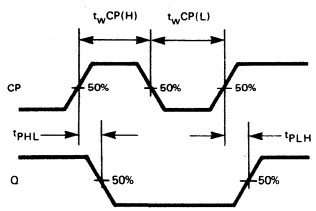


PROPAGATION DELAY VERSUS LOAD CAPACITANCE



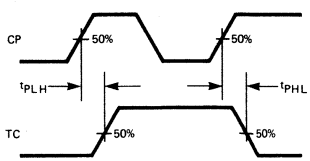
SWITCHING DIAGRAMS

CLOCK (CP) TO OUTPUT (Q) PROPAGATION DELAYS AND MINIMUM CLOCK PULSE WIDTH



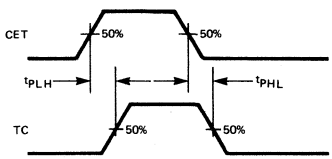
CONDITIONS: $\overline{PE}$ = $\overline{MR}$ = CEP = CET = H for F40160/F40161 and $\overline{PE}$ = $\overline{SR}$ = CEP = CET = H for F40162/F40163.

CLOCK (CP) TO TERMINAL COUNT (TC) PROPAGATION DELAYS



CONDITIONS: See the Terminal Count Generation Table $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H for F40160/F40161 and $\overline{PE}$ = CEP = CET = SR = H for F40162/F40163.

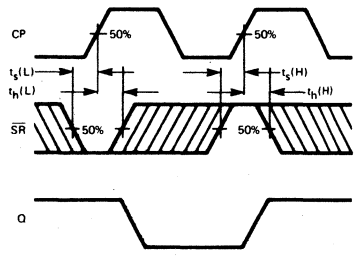
COUNT ENABLE TRICKLE INPUT (CET) TO TERMINAL COUNT OUTPUT (TC) PROPAGATION DELAYS



CONDITIONS: See the Terminal Count Generation Table. CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H for F40160/F40161 and CP = $\overline{PE}$ = CEP = $\overline{SR}$ = H for F40162/F40163.

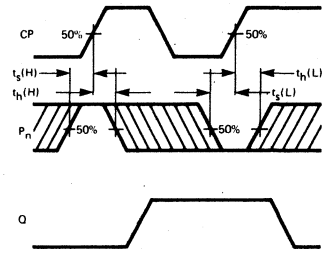
SWITCHING DIAGRAMS (Cont'd)

F40162/F40163
SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR SYNCHRONOUS RESET ($\overline{SR}$)



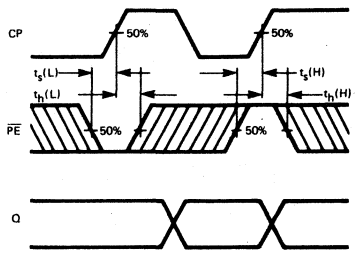
CONDITIONS: $\overline{PE}$ = L, P_0-P_3 = H.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR PARALLEL DATA INPUTS (P_0-P_3).



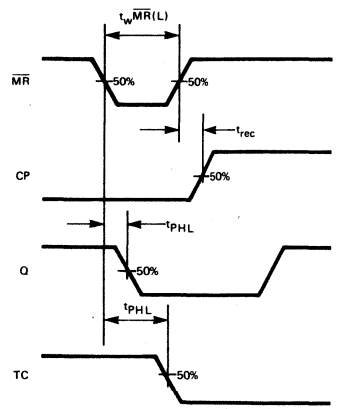
CONDITIONS: $\overline{PE}$ = L, $\overline{MR}$ = H for F40160/F40161 and $\overline{PE}$ = L, $\overline{SR}$ = H for F40162/F40163.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR PARALLEL ENABLE INPUT $\overline{PE}$



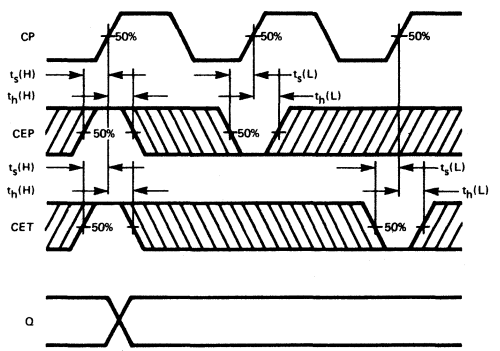
CONDITIONS: $\overline{MR}$ = H for F40160/F40161 and $\overline{SR}$ = H for F40162/F40163.

F40160/F40161
MASTER RESET ($\overline{MR}$) TO OUTPUT (Q) DELAY, MASTER RESET PULSE WIDTH, MASTER RESET RECOVERY TIME, AND MASTER RESET TO TERMINAL COUNT (TC) DELAY



CONDITIONS: $\overline{PE}$ = L and P_0 = P_1 = P_2 = P_3 = H.

SET-UP TIMES (t_s) AND HOLD TIMES (t_h) FOR COUNT ENABLE INPUTS (CEP AND CET)



CONDITIONS: $\overline{PE}$ = $\overline{MR}$ = H for F40160/F40161 and $\overline{PE}$ = $\overline{SR}$ = H for F40162/F40163.

NOTE:
1. Set-up Times (t_s) and Hold Times (t_h) are shown as positive values, but may be specified as negative values.

F40174/340174

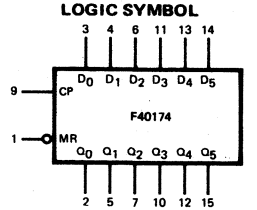
HEX D FLIP-FLOP

DESCRIPTION – The F40174 is a Hex Edge-Triggered D Flip-Flop with six Data Inputs (D_0-D_5), a Clock Input (CP) an overriding asynchronous Master Reset ($\overline{MR}$), and six Buffered Outputs (Q_0-Q_5).

Information on the Data Inputs (D_0-D_5) is transferred to the Buffered Outputs (Q_0-Q_5) on the LOW-to-HIGH transition of the Clock Input (CP) if the Master Reset Input ($\overline{MR}$) is HIGH. When LOW, the Master Reset Input ($\overline{MR}$) resets all flip-flops (Q_0-Q_5 = LOW) independent of the Clock (CP) and Data Inputs (D_0-D_5).

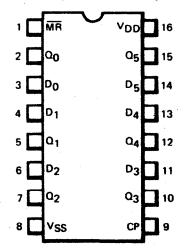
- **TYPICAL CLOCK FREQUENCY OF 16 MHz AT V_{DD} = 10 V**
- **COMMON CLOCK TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **COMMON ACTIVE LOW MASTER RESET**
- **FULLY EDGE-TRIGGERED CLOCK INPUT**

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

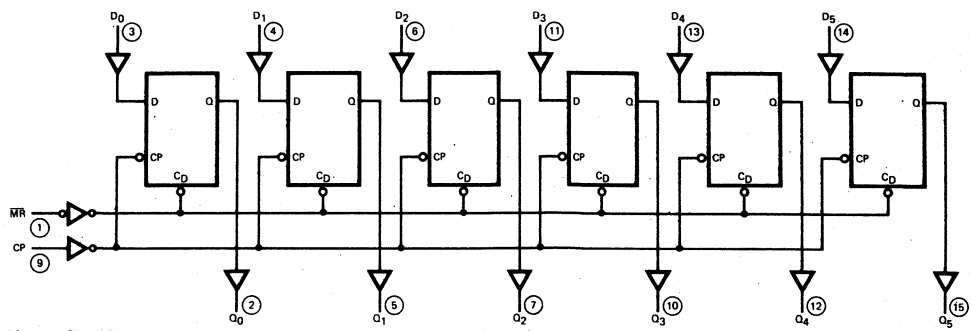


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

D_0-D_5	Data Inputs
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_5	Buffered Outputs from the Flip-Flops

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40		8		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					200			400		80			MAX	
		XM			2			4		0.8		µA	MIN, 25°C	
					100			200		40			MAX	

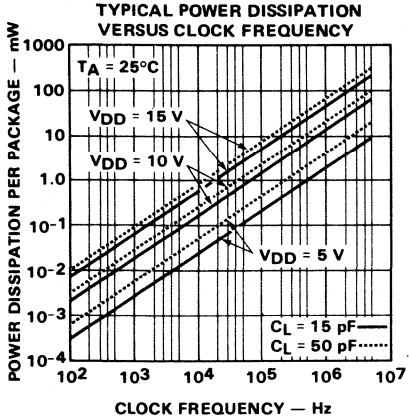
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		60	100		25	45		18		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			60	100		25	45		18		ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		65	105		30	50		20		ns	
t_{TLH}	Output Transition Time		35	75		20	40		10	25	ns	
t_{THL}			35	75		20	40		10	25	ns	
t_{PLH}	Propagation Delay, CP to Q_n		70	115		35	60		25		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			70	115		35	60		25		ns	
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		80	125		40	65		25		ns	
t_{TLH}	Output Transition Time		65	135		35	70		15	45	ns	
t_{THL}			65	135		35	70		15	45	ns	
t_wCP(L)	Minimum Clock Pulse Width	45	25		20	10			8		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
$t_w\overline{MR}$(L)	Minimum $\overline{MR}$ Pulse Width	55	35		35	20			15		ns	
t_{rec}	$\overline{MR}$ Recovery Time	25	6		13	5			2		ns	
t_s	Set-Up Time, D_n to CP	5	1		5	1			0		ns	
t_h	Hold Time, D_n to CP	20	10		10	2			1		ns	
f_{MAX}	Maximum Clock Frequency (Note 4)	5	9		8	16					MHz	

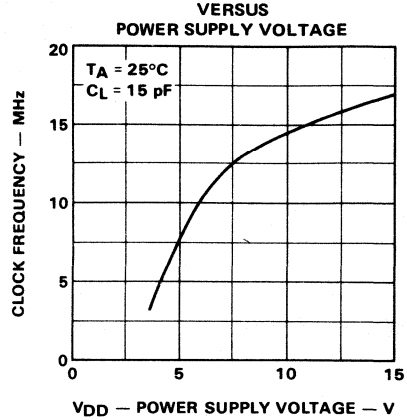
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L); Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 µs.

TYPICAL ELECTRICAL CHARACTERISTICS

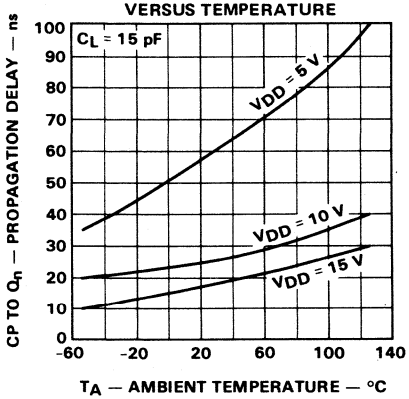
TYPICAL POWER DISSIPATION VERSUS CLOCK FREQUENCY



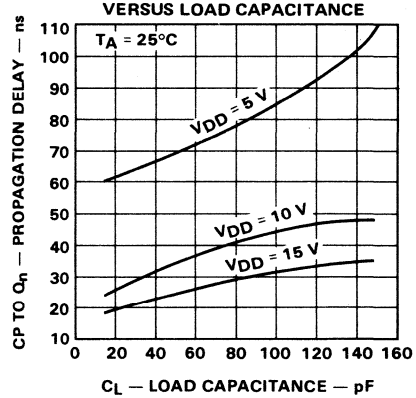
CLOCK FREQUENCY VERSUS POWER SUPPLY VOLTAGE



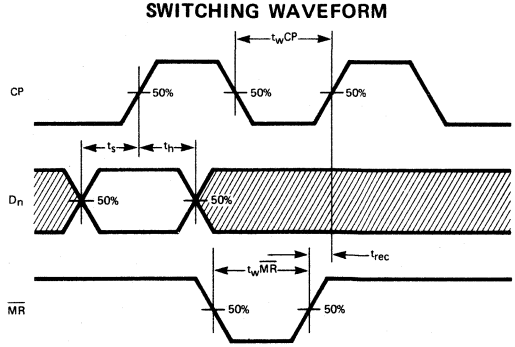
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE



SWITCHING WAVEFORM



MINIMUM PULSE WIDTHS FOR CP AND $\overline{MR}$, $\overline{MR}$
RECOVERY TIME, AND SET-UP AND HOLD TIMES, D_n TO CP

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values

F40175/340175
QUAD D FLIP-FLOP

DESCRIPTION – The F40175 is a Quad Edge-Triggered D Flip-Flop with four Data Inputs (D_0-D_3), a Clock Input (CP) an overriding asynchronous Master Reset ($\overline{MR}$), four Buffered Outputs (Q_0-Q_3) and four Complementary Buffered Outputs ($\overline{Q}_0$-$\overline{Q}_3$).

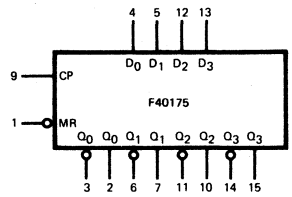
Information on the Data Inputs (D_0-D_3) is transferred to Outputs (Q_0-Q_3) on the LOW-to-HIGH Transition of the Clock Input (CP) if the Master Reset Input ($\overline{MR}$) is HIGH. When LOW, the Master Reset Input ($\overline{MR}$) resets all flip-flops (Q_0-Q_3 = LOW, $\overline{Q}_0$-$\overline{Q}_3$ = HIGH), independent of the Clock (CP) and Data (D_0-D_3) Inputs.

- **TYPICAL CLOCK FREQUENCY OF 16 MHz AT V_{DD} = 10 V**
- **COMMON CLOCK TRIGGERED ON LOW-TO-HIGH TRANSITION**
- **COMMON ACTIVE LOW MASTER RESET**
- **TRUE AND COMPLEMENTARY OUTPUTS AVAILABLE**
- **FULLY EDGE-TRIGGERED CLOCK INPUT**

PIN NAMES

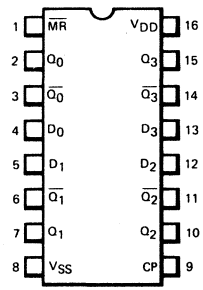
D_0-D_3	Data Inputs
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Buffered Outputs from the Flip-Flops
$\overline{Q}_0$-$\overline{Q}_3$	Complimentary Buffered Outputs from the Flip-Flops

LOGIC SYMBOL



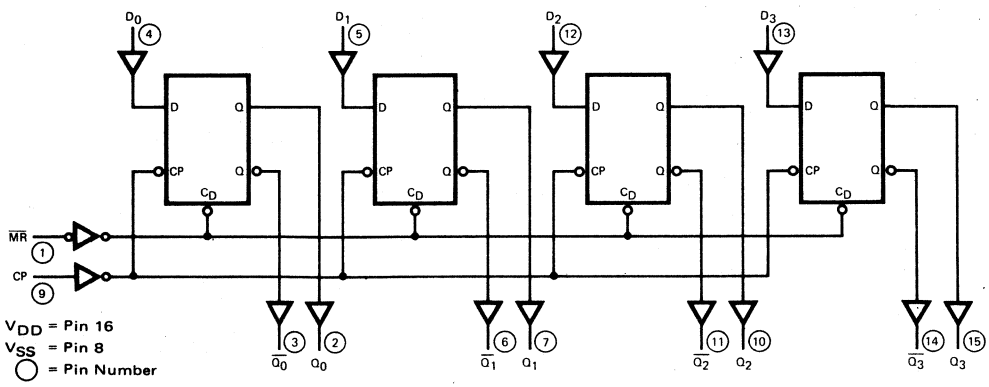
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

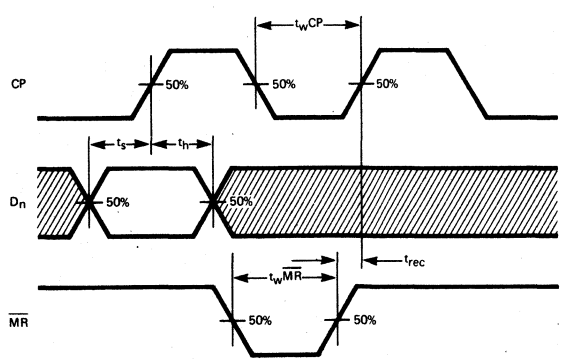
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40		8		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					200			400		80			MAX	
		XM			2			4		0.8		μA	MIN, 25°C	
					100			200		40			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n or $\overline{Q_n}$		60 60			25 25			18 18		ns ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n or $\overline{Q_n}$		65 65			30 30			20 20		ns ns	
t_{TLH} t_{THL}	Output Transition Time		35 35			20 20			10 10		ns ns	
t_{PLH} t_{PHL}	Propagation Delay, CP to Q_n or $\overline{Q_n}$		70 70			35 35			25 25		ns ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n or $\overline{Q_n}$		80 80			40 40			25 25		ns ns	
t_{TLH} t_{THL}	Output Transition Time		65 65			35 35			15 15		ns ns	
t_wCP(L)	Minimum Clock Pulse Width		25			10			8		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
$t_w\overline{MR}$(L)	Minimum $\overline{MR}$ Pulse Width		35			20			15		ns	
t_{rec}	$\overline{MR}$ Recovery Time		6			5			2		ns	
t_s t_h	Set-Up Time, D_n to CP Hold Time, D_n to CP		1 10			1 2			0 1		ns ns	
f_{MAX}	Maximum Clock Frequency (Note 4)		9			16					MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR CP AND $\overline{MR}$, $\overline{MR}$ RECOVERY TIME, AND SET-UP AND HOLD TIMES, D_n TO CP

Note: Set-up and Hold Times are shown as positive values but may be specified as negative values.

F40192/340192 • F40193/340193
4-BIT UP/DOWN DECADE AND BINARY COUNTER

DESCRIPTION – The F40192 is a 4-Bit Synchronous Up/Down BCD Decade Counter and the F40193 is a 4-Bit Synchronous Up/Down Binary Counter. Both operate the same except for the count sequence. Both counters have a Count Up Clock Input (CP_U), a Count Down Clock Input (CP_D), an asynchronous Parallel Load Input ($\overline{PL}$), four Parallel Data Inputs (P_0–P_3), an overriding asynchronous Master Reset (MR), four Counter Outputs (Q_0–Q_3), a Terminal Count Up (Carry) Output ($\overline{TC_U}$) and a Terminal Count Down (Borrow) Output ($\overline{TC_D}$).

When the Master Reset Input (MR) is LOW and the Parallel Load Input ($\overline{PL}$) is HIGH, the Counter Outputs change state on the LOW-to-HIGH transition of either Clock Input. However, for correct counting, both Clock Inputs cannot be LOW simultaneously. With the Master Reset Input (MR) LOW, information on the Parallel Data Inputs (P_0–P_3) is loaded into the counter when the Parallel Load Input ($\overline{PL}$) is LOW and stored in the counter when the Parallel Load Input ($\overline{PL}$) goes HIGH, independent of Clock Inputs (CP_U, CP_D). When HIGH, the Master Reset (MR) resets the counter independent of all other input conditions. See equations below for Terminal Count Outputs ($\overline{TC_U}$, $\overline{TC_D}$).

- **TYPICAL COUNT FREQUENCY OF 8 MHz AT V_{DD} = 10 V**
- **SYNCHRONOUS OPERATION**
- **INTERNAL CASCADING CIRCUITRY PROVIDED**
- **ACTIVE LOW PARALLEL LOAD**
- **ACTIVE HIGH ASYNCHRONOUS MASTER RESET**

PIN NAMES

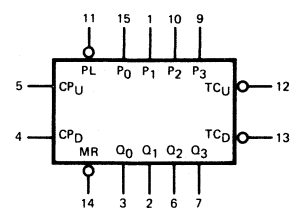
$\overline{PL}$	Parallel Load Input (Active LOW)
P_0–P_3	Parallel Data Inputs
CP_U	Count Up Clock Pulse Input (L→H Edge-Triggered)
CP_D	Count Down Clock Pulse Input (L→H Edge-Triggered)
MR	Master Reset Input (Asynchronous)
Q_0–Q_3	Buffered Counter Outputs
$\overline{TC_U}$	Buffered Terminal Count Up (Carry) Output (Active LOW)
$\overline{TC_D}$	Buffered Terminal Count Down (Borrow) Output (Active LOW)

MODE SELECTION
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐¬	H	Count Up
L	H	H	⌐¬	Count Down

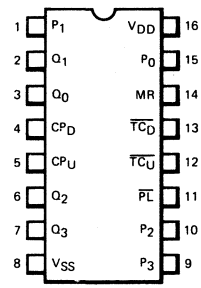
L = LOW Level
H = HIGH Level
X = Don't Care
⌐¬ = Positive-Going Clock Pulse Edge

LOGIC SYMBOL



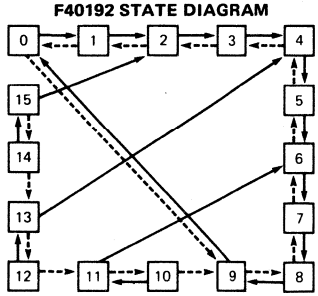
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



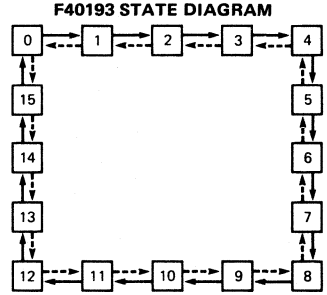
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

F40192 STATE DIAGRAM



Count Up ————
Count Down ----------

F40193 STATE DIAGRAM



F40192 LOGIC EQUATIONS FOR TERMINAL COUNT

$TC_U = Q_0 \bullet Q_3 \bullet \overline{CP_U}$

$TC_D = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$

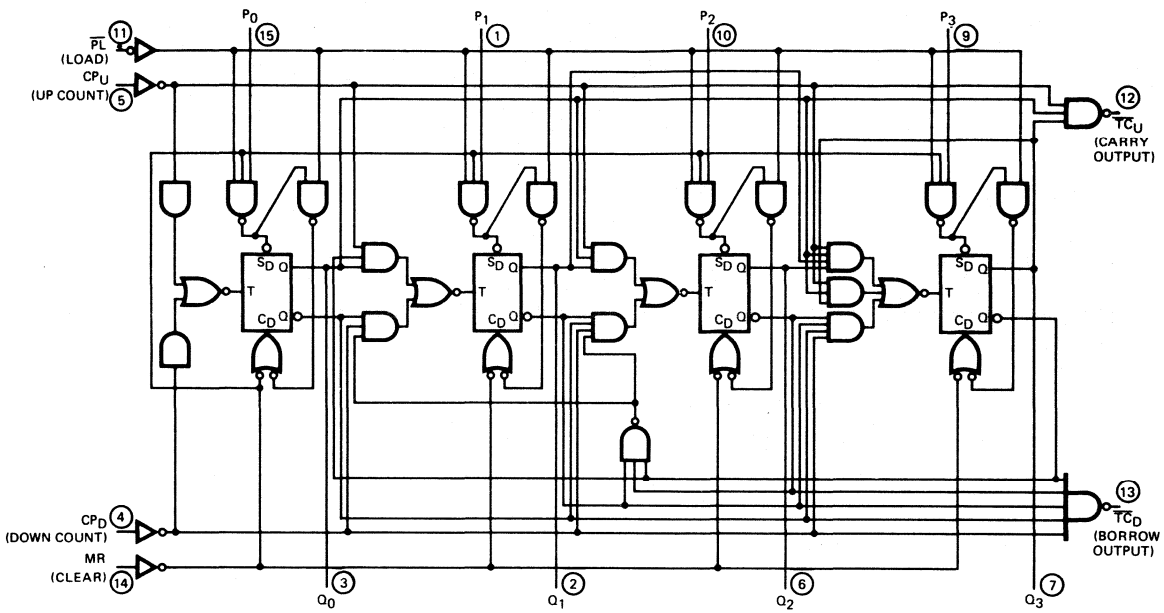
F40193 LOGIC EQUATIONS FOR TERMINAL COUNT

$TC_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP_U}$

$TC_D = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$

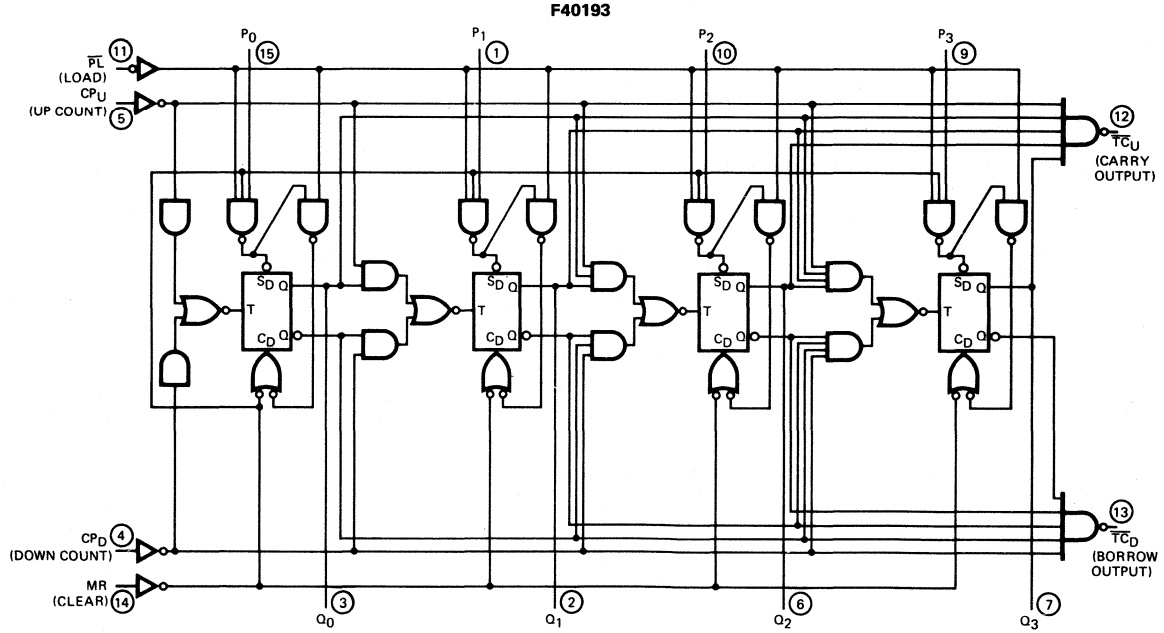
LOGIC DIAGRAMS

F40192



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

F40193



V_{DD} = Pin 16
V_{SS} = Pin 8
◯ = Pin Number

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		µA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			15			25		5		µA	MIN, 25°C	
					900			1500		3000			MAX	

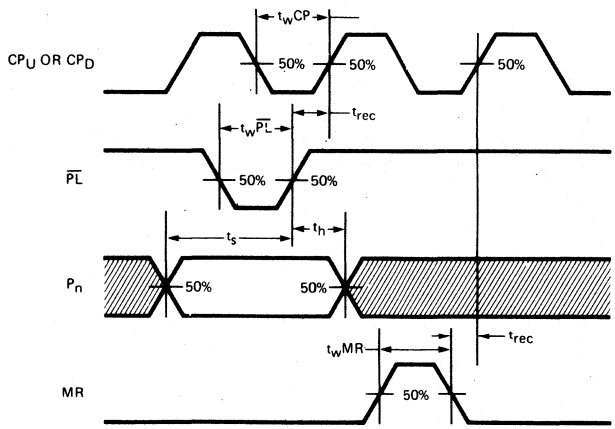
AC CHARACTERISTICS AND SWITCHING REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_U to Q_n		225			95			65		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			225			95			65		ns	
t_{PLH}	Propagation Delay, CP_D to Q_n		225			95			65		ns	
t_{PHL}			225			95			65		ns	
t_{PLH}	Propagation Delay, CP_U to $\overline{TC_U}$		110			50			35		ns	
t_{PHL}			110			50			35		ns	
t_{PLH}	Propagation Delay, CP_D to $\overline{TC_D}$		125			50			35		ns	
t_{PHL}			125			50			35		ns	
t_{PHL}	Propagation Delay, MR to Q_n		250			110			75		ns	
t_{PLH}	Propagation Delay, MR to $\overline{TC_U}$ or $\overline{TC_D}$		350			150			100		ns	
t_{PLH}	Propagation Delay, $\overline{PL}$ to Q_n		250			100			65		ns	
t_{PHL}			250			100			65		ns	
t_{TLH}	Output Transition Time		35			20			15		ns	
t_{THL}			35			20			15		ns	
t_{PLH}	Propagation Delay, CP_U to Q_n		245			105			70		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			245			105			70		ns	
t_{PLH}	Propagation Delay, CP_D to Q_n		245			105			70		ns	
t_{PHL}			245			105			70		ns	
t_{PLH}	Propagation Delay, CP_U to $\overline{TC_U}$		130			60			40		ns	
t_{PHL}			130			60			40		ns	
t_{PLH}	Propagation Delay, CP_D to $\overline{TC_D}$		145			60			40		ns	
t_{PHL}			145			60			40		ns	
t_{PHL}	Propagation Delay, MR to Q_n		270			120			80		ns	
t_{PLH}	Propagation Delay, MR to $\overline{TC_U}$ or $\overline{TC_D}$		370			170			105		ns	
t_{PLH}	Propagation Delay, $\overline{PL}$ to Q_n		270			110			70		ns	
t_{PHL}			270			110			70		ns	
t_{TLH}	Output Transition Time		55			30			20		ns	
t_{THL}			55			30			20		ns	
t_wCP	Min. CP_U or CP_D Pulse Width		85			30			20		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_wMR	Minimum MR Pulse Width		60			30			20		ns	
$t_w\overline{PL}$	Minimum $\overline{PL}$ Pulse Width		75			25			20		ns	
t_{rec}	MR Recovery Time		75			30			20		ns	
t_{rec}	$\overline{PL}$ Recovery Time		75			30			20		ns	
t_s	Set-Up Time, P_n to $\overline{PL}$		85			30			20		ns	
t_h	Hold Time, P_n to $\overline{PL}$		-83			-28			-19		ns	
f_{MAX}	Input Count Frequency (Note 4)		4			8					MHz	

Notes on following page.

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Inputs (CP_U or CP_D) be less than 15 μs.

SWITCHING WAVEFORMS



RECOVERY TIMES FOR $\overline{PL}$ AND MR, MINIMUM PULSE WIDTHS FOR CP_U, CP_D, $\overline{PL}$ AND MR AND SET-UP AND HOLD TIMES P_n TO $\overline{PL}$

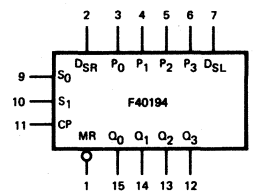
NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

F40194/340194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

DESCRIPTION – The F40194 is a 4-Bit Bidirectional Shift Register with two Mode Control Inputs (S_0, S_1), a Clock Input (CP), a Serial Data Shift Left Input (D_{SL}), a Serial Data Shift Right Input (D_{SR}), four Parallel Data Inputs (P_0-P_3), an overriding asynchronous Master Reset Input ($\overline{MR}$) and four Buffered Parallel Outputs (Q_0-Q_3).

When LOW, the Master Reset Input ($\overline{MR}$) resets all stages and forces all Outputs (Q_0-Q_3) LOW, overriding all other input conditions. When the Master Reset Input ($\overline{MR}$) is HIGH, the operating mode is controlled by the two Mode Control Inputs (S_0, S_1) as shown in the Truth Table. Serial and parallel operation is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). The inputs at which the data is to be entered and the Mode Control Inputs (S_0, S_1) must be stable for a set-up time before the LOW-to-HIGH transition of the Clock Input CP).

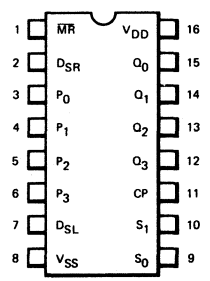
LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **POSITIVE EDGE-TRIGGERED CLOCK**

CONNECTION DIAGRAM
DIP (TOP VIEW)

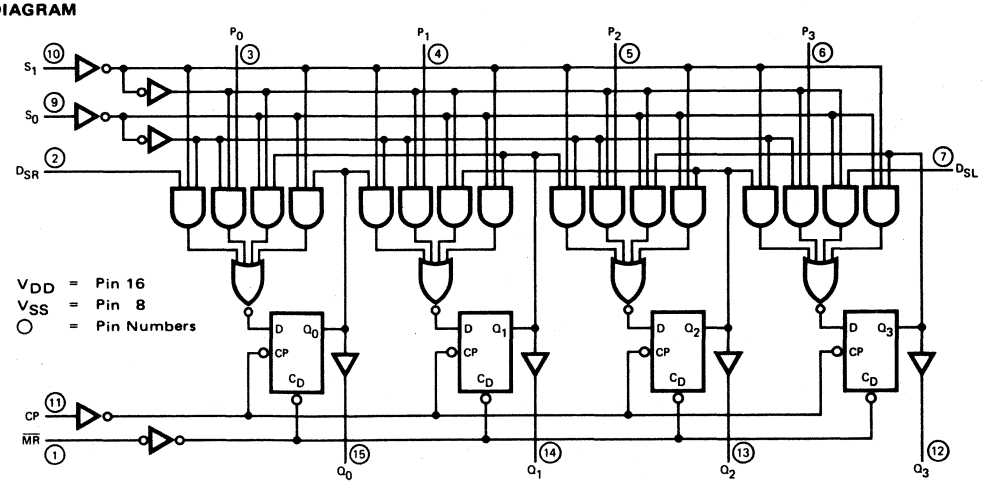


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

PIN NAMES

S_0, S_1	Mode Control Inputs
P_0-P_3	Parallel Data Inputs
D_{SR}	Serial (Shift Right) Data Input
D_{SL}	Serial (Shift Left) Data Input
CP	Clock Input (L→H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Parallel Outputs

LOGIC DIAGRAM



TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)					OUTPUTS AT t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	P_0,P_1,P_2,P_3	Q_0	Q_1	Q_2	Q_3
Hold	L	L	X	X	X	Q_0	Q_1	Q_2	Q_3
Shift Left	H	L	X	L	X	Q_1	Q_2	Q_3	L
	H	L	X	H	X	Q_1	Q_2	Q_3	H
Shift Right	L	H	L	X	X	L	Q_0	Q_1	Q_2
	L	H	H	X	X	H	Q_0	Q_1	Q_2
Parallel Load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(t_{n+1}) = Indicates state after next LOW-to-HIGH clock transition.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					500			1000		200			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					40			80		16			MAX	

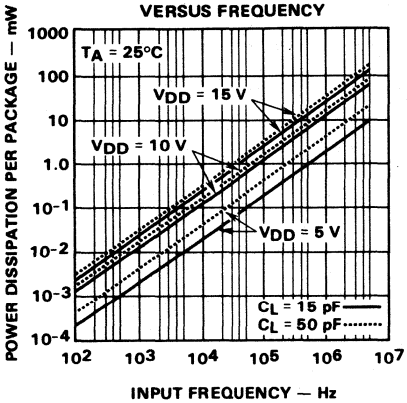
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q		80	150		35	65		25		ns	
t_{PHL}			80	150		35	65		25		ns	C_L = 15 pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		80	150		35	65		25		ns	Input Transition
t_{THL}	Output Transition Time		40	75		20	40		15	25	ns	Times < 20 ns
t_{TLH}			40	75		20	40		15	25	ns	
t_{PLH}	Propagation Delay, CP to Q		100	180		45	80		35		ns	
t_{PHL}			100	180		45	80		35		ns	C_L = 50 pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q		100	180		45	80		35		ns	Input Transition
t_{THL}	Output Transition Time		75	135		40	70		25	45	ns	Times < 20 ns
t_{TLH}			75	135		40	70		25	45	ns	
t_s	Set-Up Time, $P_0 - P_3$, D_{SL}, D_{SR} to CP	80	40		40	20			15		ns	
t_h	Hold Time, $P_0 - P_3$, D_{SL}, D_{SR} to CP	0	-10		0	-5			-5		ns	
t_s	Set-Up Time, S to CP	100	60		50	30			20		ns	
t_h	Hold Time, S to CP	0	-10		0	-5			-5		ns	C_L = 15 pF
t_wCP(L)	Minimum Clock Pulse Width	100	60		60	35			25		ns	Input Transition
$t_w\overline{MR}$(L)	Minimum $\overline{MR}$ Pulse Width	75	40		45	25			15		ns	Times < 20 ns
t_{rec}	Recovery Time for $\overline{MR}$	180	100		90	50			35		ns	
f_{MAX}	Maximum CP Frequency (Note 4)	4.5	9		9	14					MHz	

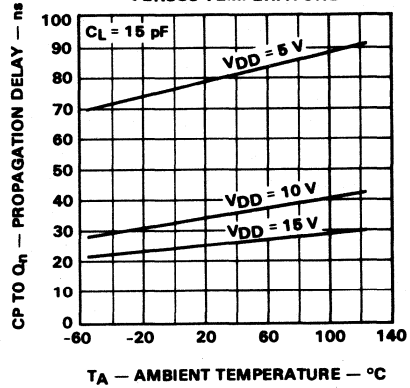
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w) do not vary with load capacitance.
4. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times to the Clock Input be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS

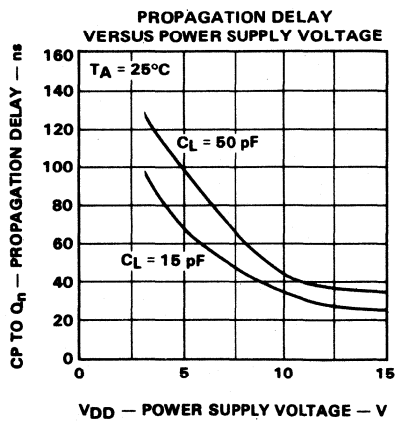
POWER DISSIPATION VERSUS FREQUENCY



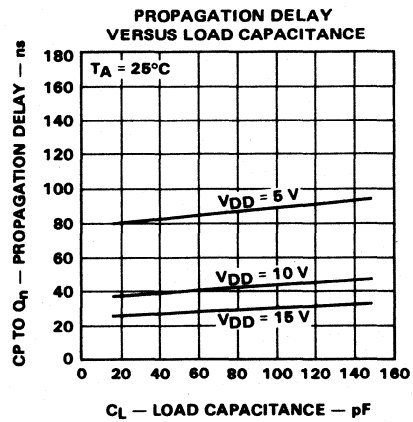
PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS POWER SUPPLY VOLTAGE

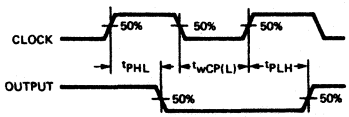


PROPAGATION DELAY VERSUS LOAD CAPACITANCE



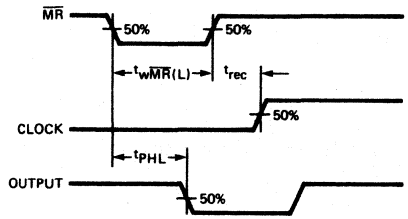
SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



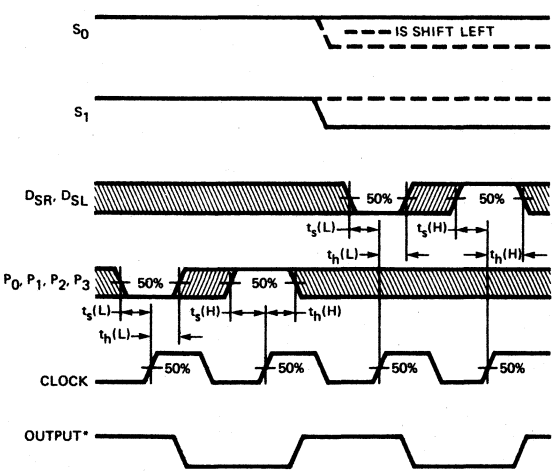
CLOCK TO OUTPUT DELAYS
CLOCK PULSE WIDTH

OTHER CONDITIONS: S_1 = L, $\overline{MR}$ = H, S_0 = H



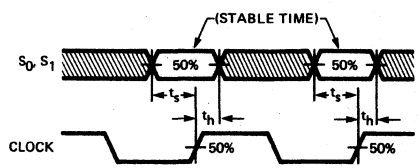
MASTER RESET PULSE WIDTH,
MASTER RESET TO OUTPUT DELAY AND
MASTER RESET TO CLOCK RECOVERY TIME

OTHER CONDITIONS: S_0, S_1 = H
$P_0 = P_1 = P_2 = P_3$ = H



SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (D_{SR}, D_{SL}) AND PARALLEL DATA (P_0, P_1, P_2, P_3)

OTHER CONDITIONS: $\overline{MR}$ = H
*D_{SR} Set-up Time Affects Q_0 Only
D_{SL} Set-up Time Affects Q_3 Only



SET-UP (t_s) AND HOLD (t_h) TIME FOR S INPUT

OTHER CONDITIONS: $\overline{MR}$ = H

F40195/340195
4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION – The F40195 is a fully synchronous edge-triggered 4-Bit Shift Register with a Clock Input (CP), four synchronous Parallel Data Inputs (P_0-P_3), two synchronous Serial Data Inputs (J, $\overline{K}$), a synchronous Mode Control Input ($\overline{PE}$), Buffered Outputs from all four bit positions (Q_0-Q_3), a Buffered Inverted Output from the last bit position ($\overline{Q}_3$) and an overriding asynchronous Master Reset Input ($\overline{MR}$).

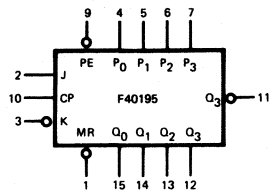
Operation is synchronous (except for Master Reset) and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Mode Control Input ($\overline{PE}$) is LOW, a LOW-to-HIGH clock transition loads data into the register from Parallel Data Inputs (P_0-P_3). When the Mode Control Input ($\overline{PE}$) is HIGH, a LOW-to-HIGH clock transition shifts data into the first register position from the Serial Data Inputs (J, $\overline{K}$), and shifts all the data in the register one position to the right. D-type entry is obtained by tying the two Serial Data Inputs (J, $\overline{K}$) together. A LOW on the Master Reset Input ($\overline{MR}$) resets all four bit positions (Q_0-Q_3 = LOW, $\overline{Q}_3$ = HIGH) independent of all other input conditions.

- **TYPICAL SHIFT FREQUENCY OF 14 MHz AT V_{DD} = 10 V**
- **ASYNCHRONOUS MASTER RESET**
- **J, $\overline{K}$ INPUTS TO THE FIRST STAGE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**
- **COMPLEMENTARY OUTPUT FROM THE LAST STAGE**
- **POSITIVE EDGE-TRIGGERED CLOCK**

PIN NAMES

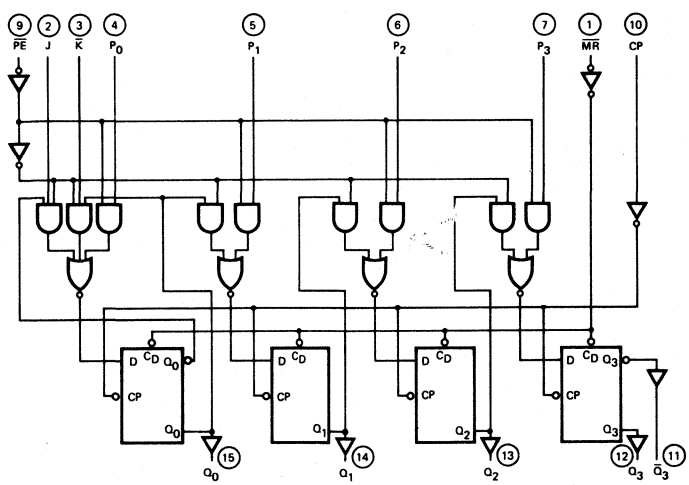
$\overline{PE}$	Parallel Enable Input (Active LOW)
P_0-P_3	Parallel Data Inputs
J	First Stage J Input (Active HIGH)
$\overline{K}$	First Stage K Input (Active LOW)
CP	Clock Input (L → H Edge-Triggered)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0-Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC SYMBOL



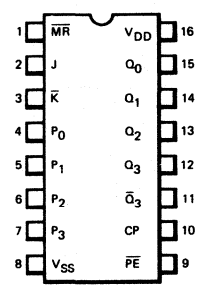
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = H)							OUTPUTS AT t_{n+1}				
	$\overline{PE}$	J	$\overline{K}$	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Shift Mode	H	L	L	X	X	X	X	L	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	L	H	X	X	X	X	Q_0	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	L	X	X	X	X	$\overline{Q}_0$	Q_0	Q_1	Q_2	$\overline{Q}_2$
	H	H	H	X	X	X	X	H	Q_0	Q_1	Q_2	$\overline{Q}_2$
Parallel Entry Mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
(t_{n+1}) = Indicates state after next LOW to HIGH clock transition.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

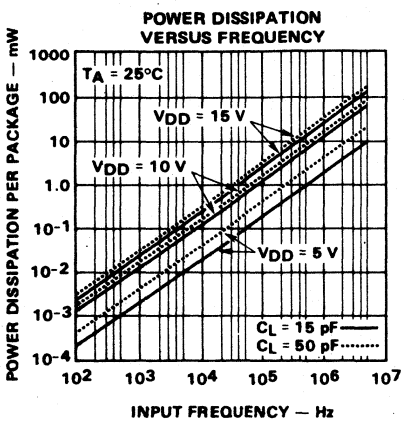
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			50			100		200		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					500			1000		200			MAX	
		XM			5			10		2		μA	MIN, 25°C	
					40			80		16			MAX	

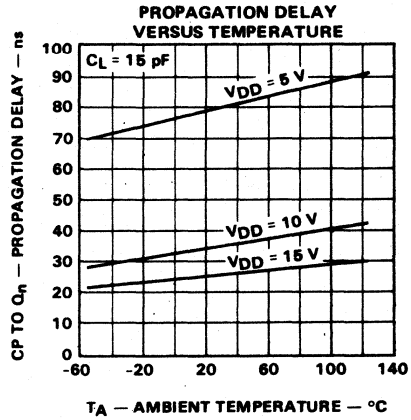
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

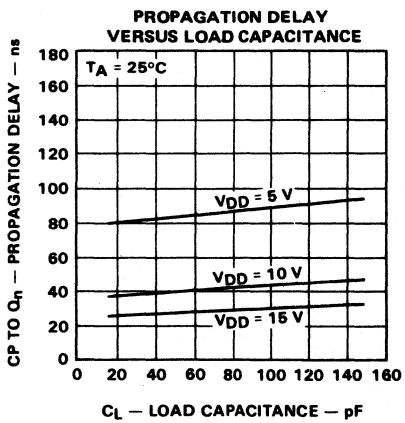
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to O_n or Q_3		80	150		35	65		25		ns	
t_{PHL}			80	150		35	65		25		ns	C_L = 15 pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to $\overline{Q_3}$		80	150		35	65		25		ns	Input Transition
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		80	150		35	65		25		ns	Times ≤ 20 ns
t_{THL}	Output Transition Time		40	75		20	40		15	25	ns	
t_{TLH}			40	75		20	40		15	25	ns	
t_{PLH}	Propagation Delay, CP to O_n or $\overline{Q_3}$		100	180		45	80		35		ns	
t_{PHL}			100	180		45	80		35		ns	C_L = 50 pF
t_{PHL}	Propagation Delay, $\overline{MR}$ to $\overline{Q_3}$		100	180		45	80		35		ns	Input Transition
t_{PHL}	Propagation Delay, $\overline{MR}$ to Q_n		100	180		45	80		35		ns	Times ≤ 20 ns
t_{THL}	Output Transition Time		75	135		40	70		25	45	ns	
t_{TLH}			75	135		40	70		25	45	ns	
t_s	Set-Up Time, J, $\overline{K}$, P_0-P_3 to CP	80	40		40	20			15		ns	
t_h	Hold Time, J, $\overline{K}$, P_0-P_3 to CP	0	−10		0	−5			−5		ns	
t_s	Set-Up Time, $\overline{PE}$ to CP	100	60		50	30			20		ns	
t_h	Hold Time, $\overline{PE}$ to CP	0	−10		0	−5			−5		ns	C_L = 15 pF
t_wCP(L)	Minimum Clock Pulse Width	100	60		60	35			25		ns	Input Transition
t_wMR(L)	Minimum $\overline{MR}$ Pulse Width	75	40		45	25			15		ns	Times ≤ 20 ns
t_{rec}	Recovery Time for $\overline{MR}$	180	100		90	50			35		ns	
f_{MAX}	Maximum CP Frequency (Note 4)	4.5	9		9	14					MHz	

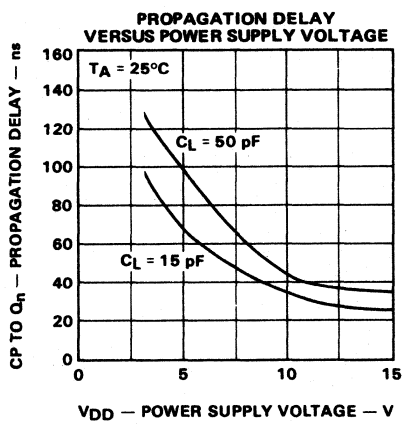
NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.
3. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transition Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-up Times (t_s), Hold Times (t_h), Recovery Times (t_{rec}), and Minimum Pulse Widths (t_w), do not vary with load capacitance.
4. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
5. It is recommended that input rise and fall times be less than 15 μs.

TYPICAL ELECTRICAL CHARACTERISTICS





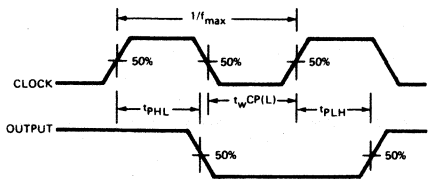




SWITCHING TIME WAVEFORMS

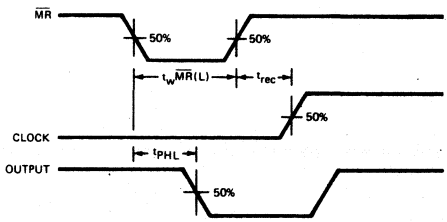
The shaded areas indicate when the input is permitted to change for predictable output performance.

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



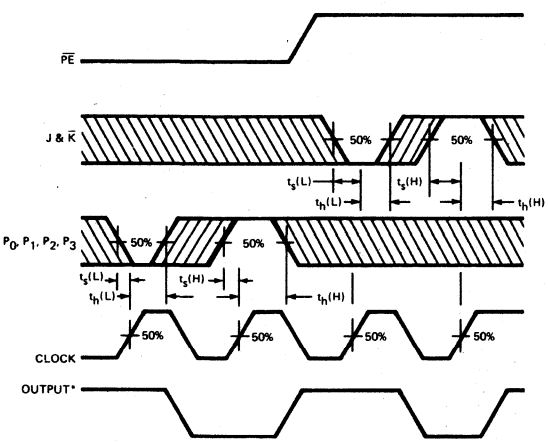
OTHER CONDITIONS: $J = \overline{PE} = \overline{MR}$ = HIGH
$\overline{K}$ = L & W

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



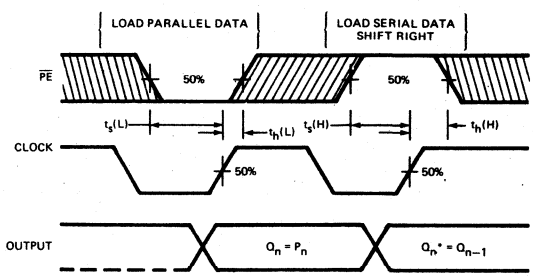
OTHER CONDITIONS: $\overline{PE}$ = LOW
$P_0 = P_1 = P_2 = P_3$ = HIGH

SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J & $\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



OTHER CONDITIONS: $\overline{MR}$ = HIGH
*J & $\overline{K}$ Set-up Time Affects Q_0 Only

SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT



OTHER CONDITIONS: $\overline{MR}$ = HIGH
*Q_0 State will be Determined by J & $\overline{K}$ Inputs

NOTE:
Set-up Times (t_s) and Hold Times (t_h) are shown as positive values but may be specified as negative values.

F40283/340283
4-BIT BINARY FULL ADDER

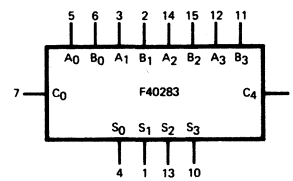
DESCRIPTION – The F40283 is a 4-Bit Binary Full Adder with two 4-bit Data Inputs (A_0–A_3, B_0–B_3), a Carry Input (C_0), four Sum Outputs (S_0–S_3) and a Carry Output (C_4).

The F40283 uses full lookahead across 4-bits to generate the Carry Output (C_4). This minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

- **FULL CARRY LOOKAHEAD ACROSS FOUR BITS**
- **EASILY CASCADED**

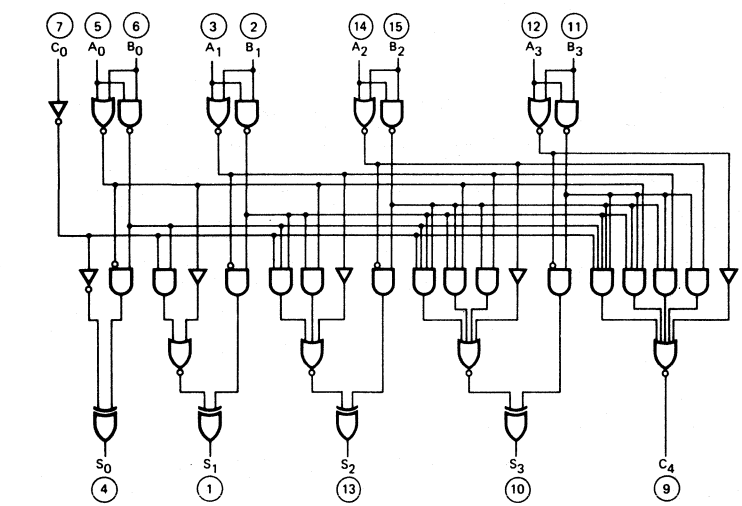
PIN NAMES	FUNCTION
A_0, B_0, A_1, B_1	Data Inputs
A_2, B_2, A_3, B_3	Data Inputs
C_0	Carry Input
S_0-S_3	Sum Outputs
C_4	Carry Output

LOGIC SYMBOL



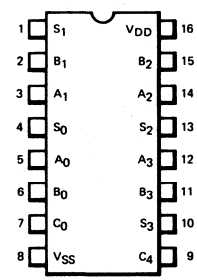
V_{DD} = Pin 16
V_{SS} = Pin 8

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			50			100		20		μA	MIN, 25°C	All inputs common and at 0 V or V_{DD}
					700			1400		280			MAX	
		XM			5			10		2.0		μA	MIN, 25°C	
					300			600		120			MAX	

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, A_n, B_n to S_n		160			62			47		ns	C_L = 15 pF Input Transition Times ≤ 20 ns
t_{PHL}			160			62			47		ns	
t_{PLH}	Propagation Delay, A_n, B_n to C_4		125			57			45		ns	
t_{PHL}			125			57			45		ns	
t_{PLH}	Propagation Delay, C_o to S_n		160			62			47		ns	
t_{PHL}			160			62			47		ns	
t_{PLH}	Propagation Delay, C_o to C_4		57			25			20		ns	
t_{PHL}			57			25			20		ns	
t_{TLH}	Output Transition Time		30			17			13		ns	
t_{THL}			30			17			13		ns	
t_{PLH}	Propagation Delay, A_n, B_n to S_n		178			69			52		ns	C_L = 50 pF Input Transition Times ≤ 20 ns
t_{PHL}			178			69			52		ns	
t_{PLH}	Propagation Delay, A_n, B_n to C_4		138			63			50		ns	
t_{PHL}			138			63			50		ns	
t_{PLH}	Propagation Delay, C_o to S_n		178			69			52		ns	
t_{PHL}			178			69			52		ns	
t_{PLH}	Propagation Delay, C_o to C_4		63			28			23		ns	
t_{PHL}			63			28			23		ns	
t_{TLH}	Output Transition Time		60			30			20		ns	
t_{THL}			60			30			20		ns	

NOTES:
1. Additional DC Characteristics are listed in this section under F4000 Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under F4000 Series CMOS Family Characteristics.

BIPOLAR INTERFACE CIRCUITS FOR CMOS

CMOS TO TTL DRIVER

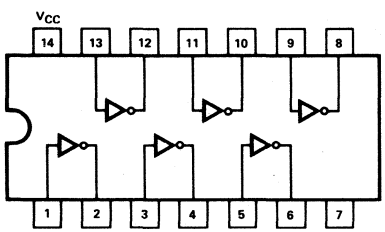
9LS04 • 54/74LS04 Hex Inverter

(Reference: Fairchild Low Power TTL Data Book)

When multi-TTL drive capability is required, the CMOS F4049 and F4050 Hex Buffers can be used to drive two standard TTL loads with typical delays of 45 ns (V_{DD} = 5 V). However, the 9LS04 drives five standard TTL loads with typical delays of 5 ns. The 9LS04 must be operated from a 5 V TTL supply, but it can accept input voltage to 11 V, allowing its use with CMOS operated up to 10 V.

- **F4000 COMPATIBLE INPUTS**
- **DRIVES FIVE TTL LOADS**
- **5 ns DELAY**
- **ACCEPTS 11 V INPUTS**
- **2 mW PER INVERTER**

9LS04 LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



MOS TO LED DIGIT DRIVER

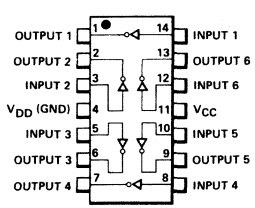
9664 MOS to LED Digit Driver

(Reference: Fairchild 9664 Data Sheet)

This driver is ideal for driving high current devices such as LEDs, relays and lamps. High input impedance allows direct drive from F4000 CMOS devices; however, there is some degradation in logic level at the CMOS output. The 9664 is specified to 10 V operation, the 9664A to 20 V.

- **150 mA SINK CAPABILITY**
- **CMOS COMPATIBLE INPUTS**
- **VERY LOW STANDBY POWER**
- **SIX HIGH GAIN DARLINGTON CIRCUITS**
- **10 AND 20 V OPERATION**

9664/9664A LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



CMOS TO 7-SEGMENT LED DISPLAY

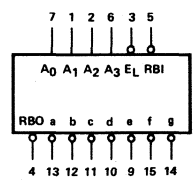
9374 7-Segment Decoder/Driver/Latch

(Reference: Fairchild 9374 Data Sheet)

This bipolar device contains latches for storage, a 7-segment decoder and 15 mA constant current drivers. The 9374 must operate at 5 V; its inputs are also limited to 5 V.

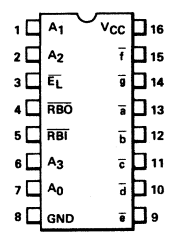
- **HIGH SPEED INPUT LATCHES FOR DATA STORAGE**
- **15 mA CONSTANT CURRENT SINK CAPABILITY TO DIRECTLY DRIVE COMMON ANODE LED DISPLAYS**
- **INCREASES INCANDESCENT DISPLAY LIFE**
- **DATA INPUT LOADING ESSENTIALLY ZERO WHEN LATCH DISABLED**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**

9374
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

9374
CONNECTION DIAGRAM
DIP (TOP VIEW)



BIPOLAR INTERFACE CIRCUITS FOR CMOS (Cont'd)

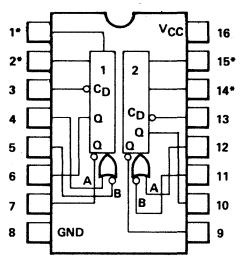
ONE-SHOT MULTIVIBRATOR

96L02 Low Power Dual
Retriggerable Resettable Monostable Multivibrator
(Reference: Fairchild Low Power TTL Book)

The 96L02 is pin and function compatible with the F4528 Dual Monostable and exhibits improved stability and speed. It is usable in 5 V CMOS systems.

- **TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT**
- **50 ns TYPICAL PROPAGATION DELAY**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **F4000 COMPATIBLE INPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

96L02 LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



* Leads for external timing

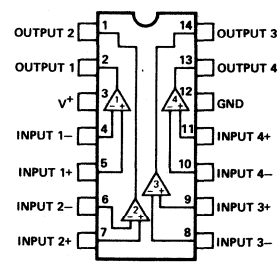
VOLTAGE COMPARATOR

μA775-Quad Comparator
(Reference: Fairchild μA775 Data Sheet)

In a CMOS system it may be necessary to detect differences between two voltage levels and convert to logic levels. The μA775 Quad Comparator is capable of operating over the CMOS power supply range. These comparators have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage. Applications include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators and wide range V_{CO}.

- **SINGLE SUPPLY OPERATION—+2.0 V TO +36 V**
- **COMPARES VOLTAGES NEAR GROUND POTENTIAL**
- **LOW CURRENT DRAIN—700 μA TYPICAL**
- **COMPATIBLE WITH ALL FORMS OF CMOS**
- **LOW INPUT BIAS CURRENT—25 nA TYPICAL**
- **LOW INPUT OFFSET CURRENT—25 nA**
- **LOW OFFSET VOLTAGE—5 mV MAX**

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



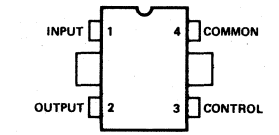
POWER SUPPLY REGULATOR

μA78MG 4-Terminal Regulator
(Reference: Fairchild μA78 MG • μA79 MG Data Sheet)

This single compact regulator with its 500 mA capability is sufficient for all but the very largest CMOS systems. The adjustable output voltage feature allows fine tuning of system speed product.

- **OUTPUT CURRENT IN EXCESS OF 0.5 A**
- **POSITIVE OUTPUT VOLTAGE 5 TO 30 V**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT PROTECTION**
- **OUTPUT SAFE AREA PROTECTION**
- **POWER MINI DUAL IN-LINE PACKAGE**

μA78 MGCONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: Heat sink tabs connected to common

CHARGE COUPLED DEVICE INTRODUCTION

Charge-coupled devices are a new class of monolithic integrated circuits based on the principle of discrete charge-packet transfer. They are characterized by high packing density, low power dissipation and low noise. Although they share the same technological base with transistors, they are functional devices that manipulate information in charge packets rather than devices that modulate electrical currents. Charge coupling is the collective transfer of all the mobile electric charge stored within a semiconductor storage element to a similar adjacent storage element. These storage elements are potential wells created in the silicon channel below closely spaced gate electrodes. External clocking of these electrodes transfers the electric charge from one potential well the the next. The clock frequency determines the shift rate. The quantity of stored charge in the "mobile packet" is determined by the input signal, the applied voltage and the capacitance of the storage cell. The amount of electric charge in each packet represents information. The basic CCD structure is a near ideal analog shift register where the number of stages in a line of the CCD structure determines the length of the register.

The input-charge information to a CCD comes from one of two sources, depending on the circuit application. A memory or analog shift register receives information from a charge injection port at the input; image-sensor information is supplied from hole-electron pairs created by incident light energy on one or more of the sensor cells. When a charge packet is transferred through the CCD register, it must neither gain nor lose significant charge or the information will change and no longer represent the input signal. The index of charge retention as the charge packet moves from one cell to the next is called *transfer efficiency*. All Fairchild CCD products utilize an ion-implanted buried-channel structure and closely spaced gate electrodes to provide high transfer efficiency, $\geqslant$ 99.99%, and reduce transfer transit time to assure high frequency performance.

CCD IMAGE SENSORS

CCD image sensors fall into two categories – linear and area. The inputs of both types are light photons which are converted to charge packets in closely spaced photosites. A linear array is composed of a row of photosites exposed to incident illumination and opaque transport registers for transferring the charge packets representing information to an output amplifier. Charge packets are transferred from the photosites to the registers after a period of integration determined by external clocking. The registers are then clocked and the light-generated charge packets are delivered to the output amplifier for conversion to proportional voltage levels. The CCD110, 101 and 121 are typical linear arrays with 256, 500 and 1728 elements respectively. The CCD131, to be announced in late 1975, has 1024 elements.

Area arrays are similar devices except that the photosites are arranged in a matrix format and the opaque transport registers are located between the photosite columns. The charge packets are transferred to the output amplifier in two separate fields, line by line. This is called the interline transfer approach. The CCD201 area image sensor has a matrix size of 100 x 100 and the CCD211, to be announced in late 1975, has a 244 x 190 matrix size.

CCD MEMORIES

Since its invention, the CCD concept has been recognized as having a great potential for digital memories. Although CCD memories can be configured in a number of ways, all are basically serial in nature and hence are block or line-access oriented rather than bit-access oriented. Their high density, low power dissipation and structural simplicity provide high performance at low cost in many cache, buffer and main-frame applications. Also, they will compete with high speed discs and other peripheral memories.

General Properties of CCD Memories

Speed – The movement of charge from one CCD electrode to the next is inherently fast, limited only by the carrier saturation velocity. A practical memory device requires several peripheral and interface circuits including read/write logic, level converters, sense amplifiers and I/O buffers. In the CCD memory, these circuits are implemented on chip by Isoplanar n-channel MOS technology and, for standard voltages, operate in the 100 kHz to 5 MHz range.

Power Dissipation – The dynamic non-equilibrium operating mode of the CCD element assures an almost ideal energy-transfer condition where on-chip power dissipation is associated primarily with the movement of signal charge (data). If, on the average, one-half the bit sites contain charge, the speed-power product is typically 0.2 pJ per bit transferred. For example, consider a simple series shift register block of N bits. The average power dissipated on-chip for a data frequency of f_c is given by the following.

$$P_D = 2N\,(0.2 \times 10^{-12})\,f_c$$

If $N = 1024$ and $f_c = 5$ MHz, then

$$P_D = 2 \text{ mW}$$

This is very low power for a memory of this size; moreover, in other configurations where most of the data is moving slowly or not at all, the power per bit is considerably lower.

Temperature Behavior – The CCD storage element is dynamic and therefore must be periodically refreshed similarly to a dynamic MOS RAM. Minimum required refresh rate is temperature dependent. At room temperature (25°C), the element storage time can be as high as one second. This value decreases by a factor of two for every 9°C increase in temperature up to approximately 70°C. Above this, it decreases even more rapidly, until at 125°C, it is falling by a factor of two every 4.5°C. For an ambient temperature of 70°C, a typical die temperature is approximately 90°C. Since the storage time is less than 5 ms under these conditions, the memory must be refreshed more frequently than at lower temperatures. The increase in refresh rate raises the power dissipation which, in turn, increases the difference between the ambient temperature and the die temperature thereby further increasing the required refresh rate. Conversely, at lowered temperatures (< 25°C), the power and time required for refresh rapidly becomes insignificant. For example, at −30°C ambient, the storage time of approximately one-third of a minute renders the memory close to non-volatile from a power dissipation standpoint. It may be advantageous, in many instances, to incorporate cooling to increase the performance of CCD memory systems.

CCD450 Dynamic Shift-Register Memory

The CCD450 is a 1-kilobyte serial storage memory consisting of 9216 bits, organized 1024 bytes by nine bits. It contains nine 1024-bit low power CCD shift registers which are shifted in parallel providing for storage and retrieval of 9-bit bytes in a byte-serial mode.

This CCD memory is a buried-channel gapless structure with ion-implanted barriers in the registers, combined with Isoplanar n-channel silicon-gate structures for on-chip timing, charge detection and level conversion. The registers are organized in a serpentine fashion with turn-around cells every 128 bits.

A byte-organized dynamic shift register complete with overhead functions, the CCD450 is particularly attractive for terminal applications where the byte organization and low power are highly important. In this application, it replaces more than nine packages, saves several square inches of board space and reduces power dissipation by more than an order of magnitude. The low power recirculate mode permits battery back-up for non-volatile and portable systems.

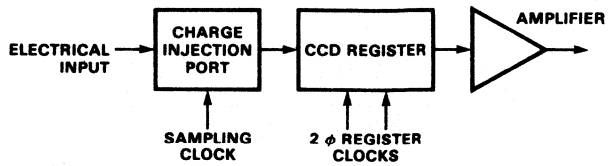
CCD460 LARAM (Line Addressable Random Access Memory)

Although the very nature of the CCD storage structure precludes a true random bit-access capability, an organization has been conceived that provides a pseudo-random access with access times in the tens of microseconds. This is the line-addressable random-access memory (LARAM), an integration of CCD and MOS memory concepts. Basically, the memory is composed of an MOS address selection matrix and a number of CCD sequential shift registers, each representing a line. When an address is selected, the driving waveforms are applied to the chosen line (register) to initiate readout, write in or refresh of information in that register.

This configuration allows an access time that is essentially dependent on the number of elements per line. In addition, since only one line is operative at any one time, clock capacitance and power dissipation are minimal. Depending on the stack configuration, a memory system using a line-addressable structure can be either word-organized where each line represents one or more words, or bit-organized, where each line contains one particular bit of a number of words. This organization is very flexible and can be used to advantage in cache buffers, swapping stores and mainframes.

CCD ANALOG SHIFT REGISTERS

The capability to manipulate information in the form of charge packets makes the CCD technology ideal for analog signal processing. In a CCD analog shift register (see block diagram), electrical inputs are applied to the charge injection port which samples the input signal at a rate determined by the input signal bandwidth.



ANALOG SHIFT REGISTER

This signal is then transformed into a charge packet and injected into the register. The 2-phase clocks shift the charge packet through the register to the output amplifier for conversion to output signal voltage. A filtering or sample-and-hold technique is usually required to recover the analog information. The time delay τ between the input and output signals is directly related to the number of elements in the CCD register, N, and the clock rate (frequency), $\tau = N/f$. Since N is fixed, varying the clock rate provides a variable delay which makes the CCD shift register a powerful device for applications that require highly precise delay of analog information such as video time-base correctors.

CCD311 Analog Shift Register

The CCD311 is a 130/260-bit analog shift register that can be operated as either a single 130-bit device, or as a 260-bit device using multiplexing techniques. It has a typical clock rate of 10 MHz and an operating frequency range of 10 kHz to 15 MHz. Delay time can be varied from 26 μs to 26 ms by simply varying the clock rate.

CCD101
500-ELEMENT SOLID STATE LINEAR IMAGE SENSOR

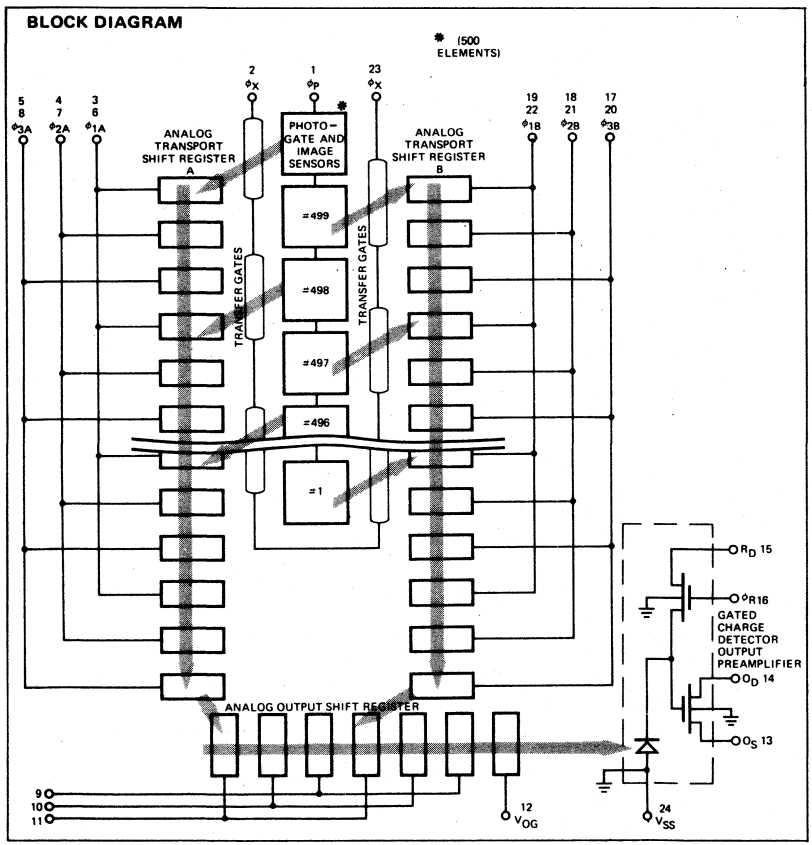
GENERAL DESCRIPTION – The CCD101 is a monolithic self-scanned 500-Element Image Sensor designed for slow scan TV, document reading, and other high sensitivity imaging applications. Buried channel and sealed silicon gate structure combined with advanced CCD processing achieve a large high-resolution optical array with high transfer efficiency and wide dynamic range.

In addition to the 500-element image sensing strip, the CCD101 includes a charge transfer gate, two 250-element analog shift registers, a 2-element analog output register, and an output detector/amplifier. The analog registers are 3-phase and provide the self scanning feature. The output signal is a sequential reading of the 500 imaging elements with a dynamic range of at least 200:1 at 1.0 MHz.

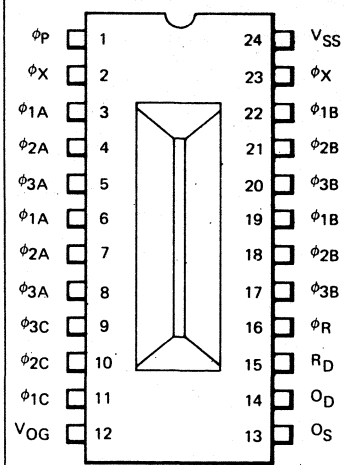
The device is packaged in a 24-Pin Dual In-line Package with a sealed glass optical window. The image sensing elements are on 0.030 mm centers.

- **DYNAMIC RANGE GUARANTEED 200:1 AT 1.0 MHz**
- **SENSITIVITY BETTER THAN 75 x 10^{-6} FT. CD. SEC.**
- **500 ELEMENTS ON A SINGLE CHIP**
- **BURIED CHANNEL AND SEALED SILICON GATE STRUCTURE**
- **ON-CHIP PREAMPLIFIER PROVIDES LOW OUTPUT IMPEDANCE**
- **LOW POWER REQUIREMENTS**
- **ALL OPERATING VOLTAGES UNDER 20 V**
- **PACKAGED IN 24-PIN DIP WITH GLASS WINDOW AND NON-REFLECTIVE INTERIOR**

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

ϕP	Photogate Clock
ϕX	Transfer Gate Clock
$\phi 1A$ and B $\phi 2A$ and B $\phi 3A$ and B	Clocks, Analog Transport Registers
$\phi 1C$ $\phi 2C$ $\phi 3C$	Clocks, Output Register
V_{OG}	Output Gate Bias Voltage
O_S	Output Transistor Source
O_D	Output Transistor Drain
ϕR	Reset Transistor Gate Clock
V_{SS}	Substrate Voltage (Ground)
R_D	Reset Transistor Drain

FUNCTIONAL DESCRIPTION – The CCD101 consists of five functional elements, illustrated in the Block Diagram:

1. A row of 500 Image Sensor Elements separated by diffused channel stops and covered by a sealed silicon photogate. This is shown in the center of the illustration.
2. Transfer Gate – a sealed silicon gate structure adjacent to both edges of the row of 500 Image Sensor Elements.
3. Two 250-Element Analog Transport Shift Registers – one on each side of the row of Image Sensor Elements and separated from it only by the Transfer Gate.
4. A 2-Element Analog Output Shift Register – shown at the bottom of the diagram. Charge coupled to both of the 250-element Transport Registers.
5. A Gated Charge Detector Output Preamplifier – shown at the right end of the Output Register. Detects the charges delivered and converts the signal to a video output voltage at terminal O_S.

Complete Device – Light energy falling on the Image Sensor Elements generates a proportional packet of electron-charge in each element. Electrical clocking of the Photogate, Transfer Gate, and the 3-Phase Transport and Output Registers delivers the charge packet from each element in a spatially related time sequence to the Gated Charge Detector Preamplifier which then delivers the resulting video signal to the output load resistor.

Image Sensor Elements and Photogate – Image photons pass through the transparent photogate and are absorbed in the single crystal silicon by hole-electron pair production. The resulting electrons are accumulated in the image sensor elements during the HIGH state of the photogate. The duration of the HIGH state is the integration period (T_{int}). The amount of charge accumulated is a linear function of the incident illumination intensity and the integration period. This charge packet can vary in an analog manner from a thermally generated minimum at zero illumination to saturation. The ratio of light level at saturation to the barely detectable light level (above the background noise) is a measure of the dynamic range of the device.

Transfer Gate – The charge packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers. Alternating charge packets are transferred out to the left register (A) and to the right (B) simultaneously. This parallel arrangement of the transport registers permits closer spacing of the image sensor elements and, thus, improves resolution. The HIGH state of the transfer gate must overlap the LOW state of both the photogate and the adjacent CCD electrode to transfer all the accumulated charge from the sensor element to the transport register. The transfer gate must then go LOW, and the photogate HIGH, to start the next light integration period.

Transport Shift Registers – The two 3-phase 250-element analog transport shift registers are used to move the image generated charge packets serially from the sensor elements to the output register, with both transport shift registers transferring charge packets to the output register simultaneously. The transport shift register clock rate is one half the output register clock rate, since the output register is handling data from both transport registers. (See Timing Diagram Figure 1.)

Output Shift Register – The output register is a 2-element 3-phase analog shift register, clocked at twice the transport register frequency. It receives inputs from both transport registers and arranges the elements in serial form in the same sequence as accumulated by the 500 image sensor elements. The clock rate of the output register is, therefore, the output data rate. The output signal is a sequential reading of the 500 image sensor elements.

The output gate is dc biased (and ac grounded). It interfaces the output register to the gated charge-detector diode, and provides shielding from clock transients.

Gated Charge Detector Output Preamplifier – The output signal (charge packet) is applied to a pre-charged diode and changes its potential linearly in response to the quantity of signal charge delivered. This potential is applied to the gate of the output n-channel MOST, producing a signal output in the external load connected to lead 13 or 14. The output impedance is 500 Ω when connected as a source follower with a 1000 Ω load. The g_m of the output transistor is approximately 1000 μmhos.

The reset transistor is clocked by a reset signal (ϕ_R) and recharges the charge-detector diode capacitance during the interval between delivery of signal charge packets from the output register.

All relationships of the above functions are illustrated in the Timing Diagram, Figure 1.

DEFINITION OF TERMS

Charge Coupling – A method of moving finite charge-packets of electrons from one position in the semiconductor to an adjacent position by the use of sequential gate induced depletion regions (potential wells) and electric fields. The packets of charge are minority carriers and no junctions are required, thus, providing low noise level operation.

Dynamic Range – The ratio of the saturation light signal level and the minimum light signal detectable above the background electronic noise level.

Charge Transfer Efficiency – The degree to which the entire charge packet of electrons is moved from one potential well to the next without loss.

Photogate Clock ϕ_P – The positive swinging voltage clock applied to the photogate to enable the sensor areas to accumulate light generated charge and to move that charge at a finite time through the transfer gate to the transport register.

Transfer Clock ϕ_X – The positive swinging voltage clock applied to the transfer gate to move the accumulated charge from the image sensor elements to the analog transport registers.

Analog Transport Register Clocks ϕ_{1A} and B, ϕ_{2A} and B, ϕ_{3A} and B – The 3-phase clock voltages applied to the gates of the transport registers to move the charge packets received from the image sensor elements to the output register.

Analog Output Register Clocks ϕ_{1C}, ϕ_{2C}, ϕ_{3C} – The 3-phase clock voltages applied to the gates of the output register to move the charge packets received from the two transport registers to the gated charge detector output preamplifier.

Gated Charge Detector Preamplifier – The output circuit portion of the CCD101 linear image sensor which receives the charge packets from the output register and converts them to video voltage output signals.

Dark Signal Non-Uniformity – The peak-to-peak variation in background signal level in the absence of light as a percentage of saturation signal level.

Photoresponse Non-Uniformity – The percentage difference in signal levels from different sensing elements exposed to the same light source, measured at the output of the CCD image sensor.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to +150°C
Operating Temperature	0°C to +75°C
Clock Inputs	
Pins 1 through 12, 16 through 23	+20V to −20V*
Pins 13, 14, 15	+20V to −0.6V*

*with respect to V_{SS}, Pin 24.

CAUTION:

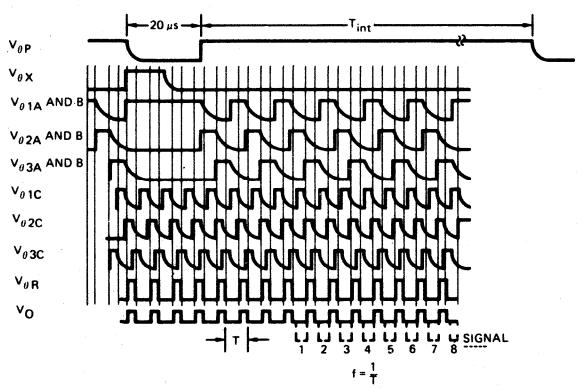
Static discharge to any pin may cause permanent damage. Use shorting clip provided during insertion and removal. Store in shorting clip or conductive foam. Use grounded soldering irons and tools. Personnel should wear grounding bracelets and avoid synthetic smocks and gloves when handling devices.

OPERATING CHARACTERISTICS: Over guaranteed operating range with R_L = 2.0 kΩ to ground, unless otherwise noted.

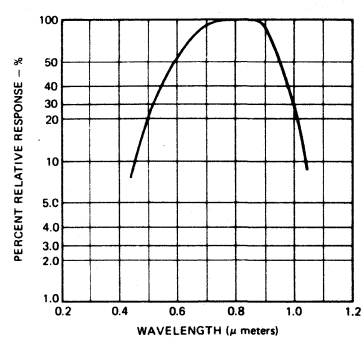
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP	MAX.		
	Dynamic Range	$2x10^2$	$5x10^2$	$3x10^3$		F_ϕ Max, 25°C
	Sensitivity			$75x10^{-6}$	Ft cd s	
	Spectral Response Range	500		1,000	n m	
	Saturation Exposure		$15x10^{-3}$		Ft cd s	2800°C Tungsten
	Photoresponse Non-Uniformity			±15	%	F_ϕ Max.
	Average Dark Signal		1.0		mV	F_ϕ Max, 25°C
	Dark Signal Non-Uniformity		1.0	2.0	% (Note 1)	F_ϕ Max.
F_ϕ	Output Register Clock Frequency	0.01		1.0	MHz	25°C
$V_{\phi L}$	Register and Transfer Gate, Clock LOW Voltage		−4.0		V	
$V_{\phi H}$	Register and Transfer Gate, Clock HIGH Voltage		+6.0		V	
$V_{\phi RL}$	Reset Clock LOW Voltage		0		V	
$V_{\phi RH}$	Reset Clock HIGH Voltage		+7.0		V	
$V_{\phi PL}$	Photogate Clock LOW Voltage		−2.0		V	
$V_{\phi PH}$	Photogate Clock HIGH Voltage		+5.0		V	
V_{RD}	Reset Transistor Drain Bias Voltage	+12	+13	+14	V	DC Voltage
V_{OD}	Output Transistor Drain Bias Voltage	+15	+17	+20	V	DC Voltage
V_{OG}	Output Gate Bias Voltage		0		V	DC Voltage
V_O	Saturation Output Voltage		500		mV	
PC	Power Consumption		50		mW	F_ϕ Max.

NOTE:
1. Dark signal non-uniformity is specified as a percentage of the saturation output signal at F_ϕ = 1.0 MHz and at the prescribed clock voltage levels.

TIMING DIAGRAM



SMOOTHED RELATIVE SPECTRAL RESPONSE



CCD110/110F
256-ELEMENT LINEAR IMAGE SENSOR

GENERAL DESCRIPTION — The CCD110/110F are monolithic self-scanned 256-Element Image Sensors designed for optical character recognition and other high sensitivity, high speed imaging applications.

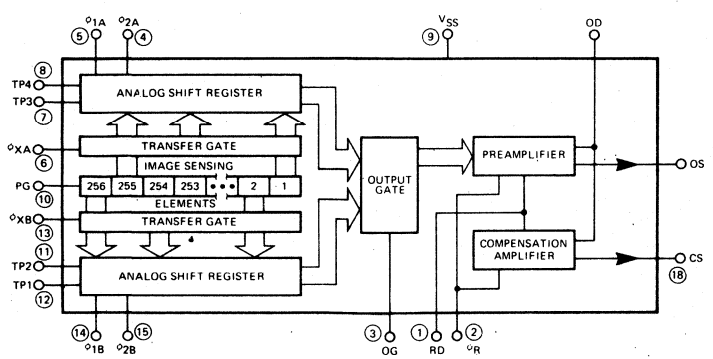
The device contains a row of 256 sensing elements that accept light photons and converts them to electrical charge packets.

In addition to a row of 256 sensing elements, the CCD110/110F chips include: two charge transfer gates, two 2-phase analog shift registers, an output charge detector/preamplifier, and a compensation output amplifier. The 2-phase analog shift registers both feed the input of the charge detector resulting in sequential reading of the 256 imaging elements.

The cell size is 13μ (0.51 mils) by 17μ (0.67 mils) on 13μ (0.51 mils) centers. The device is manufactured using Fairchild charge coupled device buried channel technology.

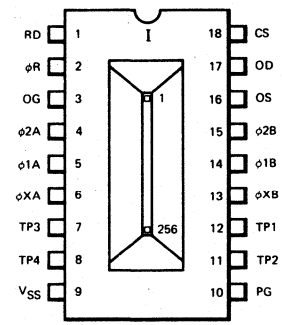
- **DYNAMIC RANGE TYPICAL: 500 TO 1 (PEAK TO PEAK), 2500 TO 1 (RMS)**
- **256 ELEMENTS ON A SINGLE CHIP**
- **ON-CHIP PREAMPLIFIER AND COMPENSATION AMPLIFIER**
- **LOW POWER REQUIREMENTS**
- **ALL OPERATING VOLTAGES UNDER 15 V**
- **PACKAGED IN 18-PIN DUAL IN-LINE PACKAGE**
- **LOW NOISE EQUIVALENT EXPOSURE**
- **WIDE RANGE OF VIDEO DATA RATE**
- **DIMENSIONALLY PRECISE PHOTOSITE SPACING**

BLOCK DIAGRAM

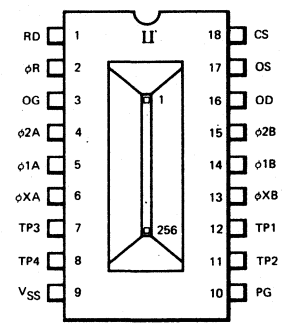


CONNECTION DIAGRAM
DIP (TOP VIEW)

CCD110



CCD110F



PIN NAMES

PG	Photogate
ϕXA, ϕXB	Transfer Gate Clock
ϕ1A, ϕ2A ϕ1B, ϕ2B	Analog Shift Register Transport Clocks
OG	Output Gate
OS	Output Transistor Source
OD	Output Transistor Drain
CS	Compensation Transistor Source
ϕR	Reset Transistor Gate Clock
RD	Reset Transistor Drain
TP	Test Point
V_{SS}	Substrate (Ground)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
Clock Inputs, Pins 2, 3, 4, 5, 6, 7, 10, 12, 13, 14, 15	−0.3 V to 12 V
Pins 1, 8, 11, 16, 17, 18	−0.3 V to 18 V

Caution: The device has limited built-in gate protection. It is recommended to control and minimize static charge build-up. Care should be taken to avoid shorting pins OS and CS to ground during operation of the device.

FUNCTIONAL DESCRIPTION – The CCD110/110F consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements – A row of 256 Image sensor elements separated by diffused channel stops and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon by hole-electron pair production. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated is a linear function of the incident illumination intensity and the integration period. The output signal will vary in this analog manner from a thermally generated noise background at zero illumination to a maximum at saturation.

Two Transfer Gates – Gate structures adjacent to the row of Image Sensor Elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers. Alternating charge packets are transferred to the right and left (A and B) analog transport shift registers. The HIGH states of the transfer-gates must be contained by the HIGH state of the transport shift register clocks. The next light integration period is started when transfer gates go LOW.

Two 130-Bit Analog Shift Registers – One on each side of the row of Image Sensor Elements and separated from it by a Transfer Gate. The two registers are used to move the image generated charge packets serially from the sensor elements to the charge detector/preamplifier. The phase relationship of the last elements of the two shift registers provide for alternate delivery of charge packets to re-establish the serial sequence of the photosites.

A Gated Charge Detector/Preamplifier – Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal output at OS. The reset transistor is driven by a reset clock (ϕR) so as to recharge the charge-detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

Generation of the necessary waveforms to operate the device is explained in detail in the CCD110/110F Board Brochure that includes a typical drive circuit diagram, a printed copy of the layout of a two-sided PC board, a parts list of components that are needed to build the board and oscilloscope photographs of the driving waveforms.

DEFINITION OF TERMS

Charge Coupled Device – A charge coupled device is a semiconductor device in which isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Gate Clock ϕ_{XA}, ϕ_{XB} – The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD shift registers.

Analog Shift Register Transport Clocks, ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} – The two sets of 2-phase clock applied to the gates of the CCD shift registers to move the charge packets received from the image sensor elements to the gated charge-detecting preamplifier.

Gated Charge Detector Preamplifier – The output circuit of the CCD110/110F which receives the charge packets from the CCD shift registers and provides a signal voltage proportional to the size of each charge packet. Before each new charge packet is sensed, a reset clock returns the output voltage to a base level.

Reset Clock ϕ_R – The voltage waveform required to drive the gated charge detector preamplifier.

Dynamic Range – The saturation exposure divided by the peak to peak noise equivalent exposure.

This does not take into account dark signal non-uniformities or average dark signal.
Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of 4 to 6 is generally appropriate. (Peak to peak noise is approximately equal to 4 to 6 times rms noise.)

DEFINITION OF TERMS (Cont'd)

Peak to Peak Noise Equivalent Exposure – The exposure level which gives an output signal equal to the peak to peak noise level at the output in the dark.

Saturation Exposure – The minimum exposure level that will produce a saturated output signal. Saturation exposure is equal to the light intensity times the photosite integration time.

Spectral Response Range – The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity – The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Photoresponse Non-uniformity – The difference of the response levels of the most and the least sensitive element under uniform illumination. This is commonly expressed as a percentage of the saturation output voltage.

Average Dark Signal – The output signal level in the dark averaged over all elements and measured relative to the base line output voltage established by the reset clock. This is a linear function of the integration time. It is also strongly dependent on temperature. This is commonly expressed as a percentage of the saturation output voltage.

Dark Signal Non-uniformity – Maximum deviation of the output voltage of any element from the background level in the dark. This is commonly expressed as a percentage of the saturation voltage.

Saturation Output Voltage – The maximum signal output voltage.

Integration Time – The time interval between the falling edges of any transfer pulse ϕXA and ϕXB as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Output Signal Range – The output signal range is defined as OSR = V_{sat} $-(t_{INT} + t_{Transfer})$ x Rate of Average Dark Signal where: t_{INT} = Integration Time; $t_{Transfer}$ = time necessary to transfer the charge packets from the analog shift registers and is equal to $\frac{260}{f_{\phi R}}$. Integration time (t_{INT}) does not necessarily equal transfer time ($t_{Transfer}$). If long integration times are required, $t_{Transfer}$ should be minimized (increase $f_{\phi R}$) to maximize OSR.

TEST LOAD CONFIGURATION

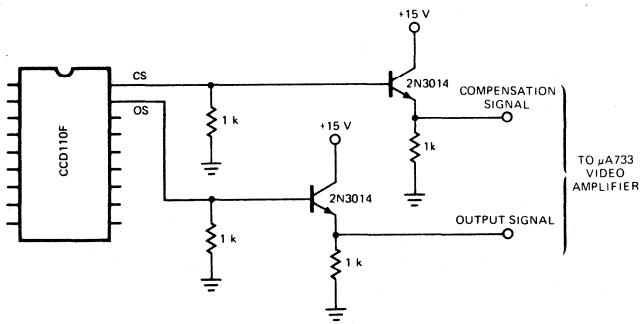


Fig. 1

DC CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{OG}	Output Gate Voltage		6.0			Note 1
V_{PG}	Photogate Voltage		9.0		V	Note 2
TP1, TP3	Test Points		0.0		V	
TP2, TP4	Test Points	14.5	15.0	15.5	V	

CLOCK CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi 1AL}$, $V_{\phi 1BL}$ $V_{\phi 2AL}$, $V_{\phi 2BL}$	Analog Shift Register Transport Clocks LOW	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi 1AH}$, $V_{\phi 1BH}$ $V_{\phi 2AH}$ $\phi 2BH$	Analog Shift Register Transport Clocks HIGH		8.0			Notes 3, 4, 12
$V_{\phi XAL}$	Transfer Gate Clock LOW	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi XAH}$	Transfer Gate Clock HIGH		8.0		V	Notes 3, 4, 12
$V_{\phi RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi RH}$	Reset Clock HIGH		10.0		V	
$f_{\phi 1A}$, $f_{\phi 1B}$ $f_{\phi 2A}$, $f_{\phi 2B}$	Analog Shift Register Transport Clock Frequency		5.0		MHz	Notes 5, 6
$f_{\phi R}$	Reset Clock Frequency (Output Bit Rate)		10		MHz	Notes 5, 6

AC CHARACTERISTICS: $T_A = 25°C$, $f_{\phi 1} = f_{\phi 2} = 2.5$ MHz, $f_{\phi R} = 5$ MHz, $t_{INT} \cong 275\ \mu s$, $t_{TRANSFER} \cong 260\ \mu s$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range	250	500			Notes, 7, 8, 9
NEE	Peak-to-Peak Noise Equivalent Exposure		1×10^{-3}		$\mu J/cm^2$	Notes 8, 9
SE	Saturation Exposure		0.5		$\mu J/cm^2$	Notes 8, 9
SR	Spectral Response Range Limits		0.45-1.05		μm	
R	Responsivity		0.4		V per $\mu J/cm^2$	Note 13
PRNU	Photoresponse Non-uniformity		±4	±6	% of V_{sat}	Note 10
ADS	Average Dark Signal		0.25	1.25	% of V_{sat}	
DSNU	Dark Signal Non-uniformity		0.5	2.5	% of V_{sat}	
V_{sat}	Saturation Output Voltage	100	200		mV	Note 11
P	Power Dissipation		100		mW	$V_{OD} = 15$ V
Z	Output Impedance		1000		Ω	
N	Peak-to-Peak Noise		400		μV	
RDS	Rate of Average Dark Signal		2		mV/ms	

NOTES:
1. Adjustment in the range of 4 V to 8 V may be required for optimum operation.
2. Adjustment in the range of 5 V to 12 V may be required for optimum operation.
3. Negative transients on the clocks below 0.0 V may cause an increase in apparent dark signal.
4. $C_{\phi XA} = C_{\phi XB} = C_{\phi 1A} = C_{\phi 1B} = C_{\phi 2A} = C_{\phi 2B} \cong 50$ pF, $C_{\phi R} \cong 1.5$ pF
5. The resulting data output frequency $f_{\phi R}$ is twice that of each analog shift register clock, $f_{\phi 1A}$, $f_{\phi 2A}$, $f_{\phi 1B}$, $f_{\phi 2B}$.
6. Clock rates shown are typical rates at which the device operates. Operation of the devices at lower or higher frequencies will not damage the device.
7. T_{int} = integration time ≃ 275 μs.
8. The dynamic range is measured by taking the ratio of the saturation output voltage to the peak-to-peak noise of the device in the dark. Because of the high degree of linearity of the device the dynamic range measurement is also approximately equal to the ratio of the saturation exposure to the peak-to-peak noise equivalent exposure.
9. 1 $\mu J/cm^2$ = 0.02 fcs at 2854° K. 1 fcs = 50 $\mu J/cm^2$ at 2854° K.
10. Measurement is done at 50% of saturation output level. Measurement excludes first and last elements.
11. See Fig. 1 for test load configuration.
12. Adjustment in the range of 6 V to 10 V may be required for optimum operation.
13. See definition of terms.

OUTPUT SIGNAL LEVEL VS. INTEGRATION TIME 2854°K TUNGSTEN SOURCE

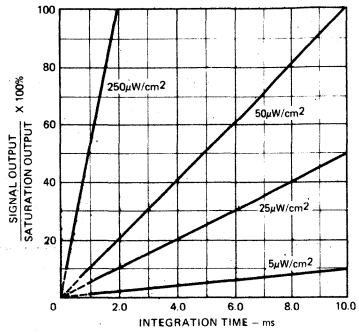
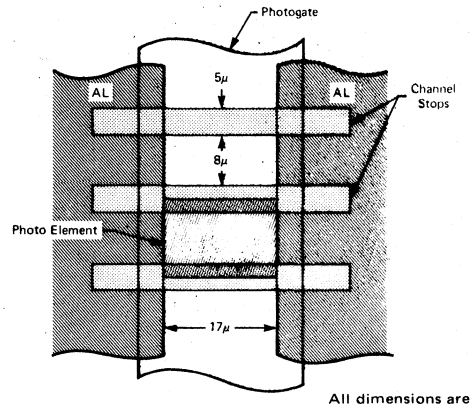


Fig. 2

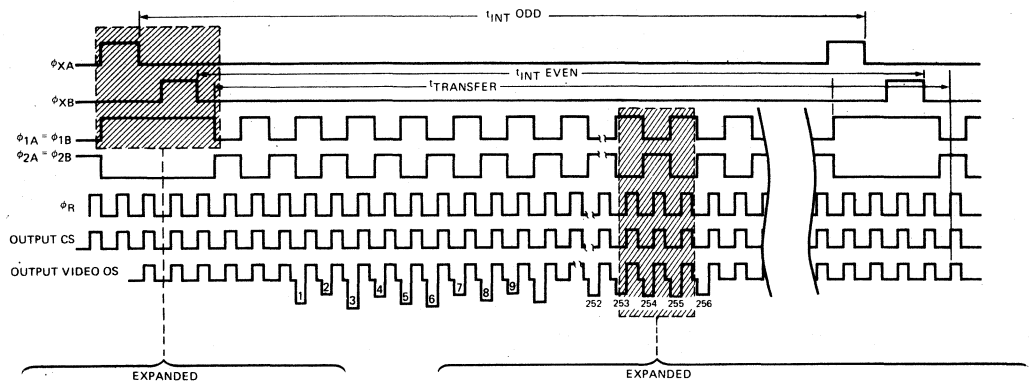
PHOTOELEMENT DIMENSIONS

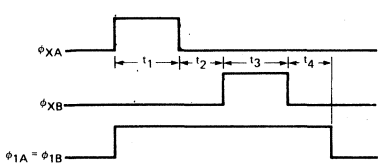


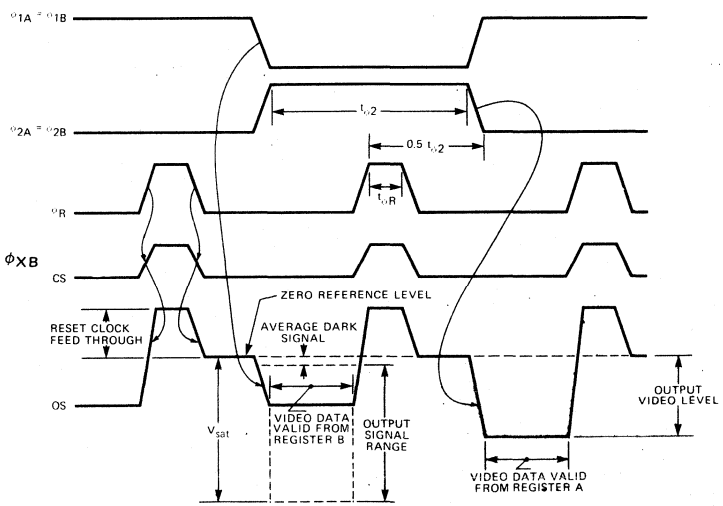
All dimensions are typical values

Fig. 3

TIMING DIAGRAM DRIVE SIGNALS







Timing requirements for Transfer Gate Pulses ϕ_{XA}, ϕ_{XB}

$t_1 = t_3 > 0.8\ \mu s$

$t_2 = t_4 > 0.1\ \mu s$

$20\ ns < (t_r \approx t_f) < 80\ ns$

Timing requirements for Reset Pulse ϕ_R

$t_r \simeq t_f \leqslant 20\ ns$

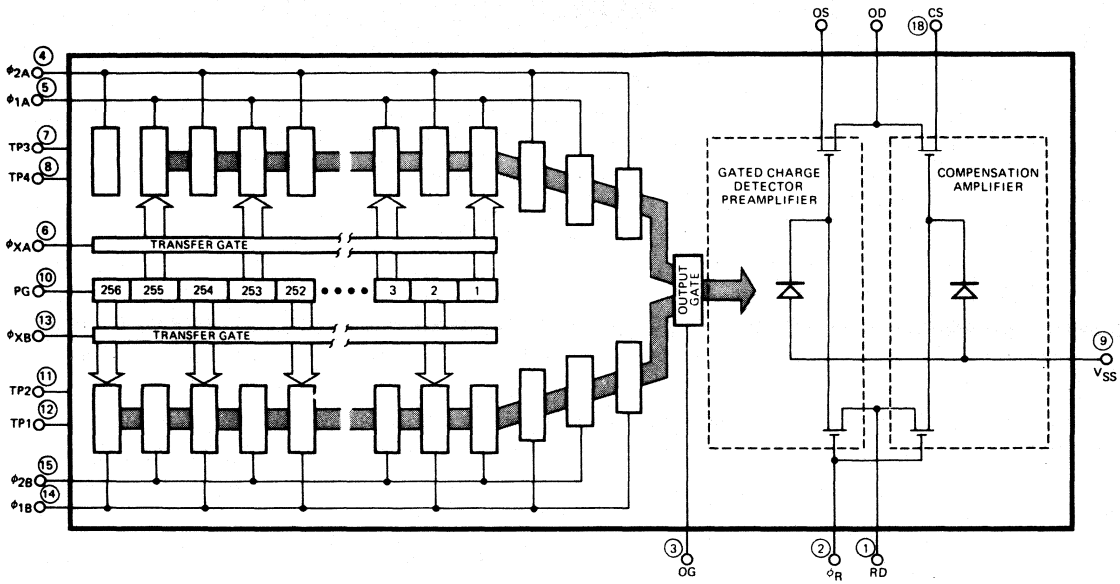
$0.2\ (t_{\phi 2}) < t_{\phi R} < 0.3\ (t_{\phi 2})$

Timing requirements for $\phi_{1A} = \phi_{1B}$

$20\ ns < (t_r \approx t_f) < 100\ ns$

Fig. 4

CIRCUIT DIAGRAM



◯ = Lead Numbers

Fig. 5

CCD121
1728-ELEMENT LINEAR IMAGE SENSOR

GENERAL DESCRIPTION – The CCD121 is a monolithic self-scanned 1728 Element Image Sensor designed for page scanning applications. The device provides a 200 line per inch resolution across an 8-1/2 inch page.

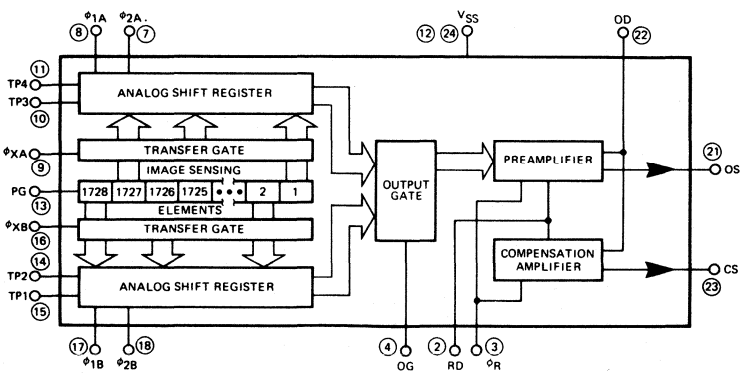
The device is also intended to be used for facsimile readers, optical character recognition, as well as imaging applications that require high resolution, high sensitivity and high speed.

In addition to a row of 1728 sensing elements, the CCD121 chip includes: two charge transfer gates, two 2-phase analog shift registers, an output charge detector/preamplifier, and a compensation output amplifier. The 2-phase analog shift registers both feed the input of the charge detector resulting in sequential reading of the 1728 imaging elements.

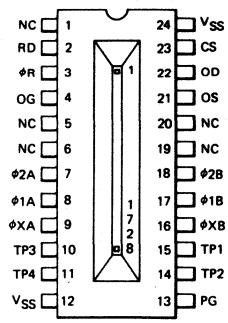
The cell size is 13μ (0.51 mils) by 17μ (0.67 mils) on 13μ (0.51 mils) centers. The device is manufactured using Fairchild charge coupled device buried channel technology.

- **DYNAMIC RANGE 500:1 TYPICAL AT 1 MHz**
- **1728 ELEMENTS ON A SINGLE CHIP**
- **ON-CHIP PREAMPLIFIER AND COMPENSATION AMPLIFIER**
- **LOW POWER REQUIREMENTS**
- **ALL OPERATING VOLTAGES UNDER 15 V**
- **PACKAGED IN 24-PIN DUAL IN-LINE PACKAGE**
- **LOW NOISE EQUIVALENT EXPOSURE**
- **WIDE RANGE OF VIDEO DATA RATE**
- **DIMENSIONALLY PRECISE PHOTOSITE SPACING**

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

PG	Photogate
ϕXA, ϕXB	Transfer Gate Clock
ϕ1A, ϕ2A ϕ1B, ϕ2B	Analog Shift Register Transport Clocks
OG	Output Gate
OS	Output Transistor Source
OD	Output Transistor Drain
CS	Compensation Transistor Source
ϕR	Reset Transistor Gate Clock
RD	Reset Transistor Drain
TP	Test Point
V_{SS}	Substrate (Ground)
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to 100°C
Operating Temperature	−25°C to 55°C
Clock Inputs, Pins 3, 7, 8, 9, 10, 13, 15, 16, 17, 18	−0.3 V to 12 V
Pins 2, 4, 11, 14, 21, 22, 23	−0.3 V to 18 V

Caution: The device has limited built-in gate protection. It is recommended to control and minimize static charge build-up. Care should be taken to avoid shorting pins OS and CS to ground during operation of the device.

FUNCTIONAL DESCRIPTION — The CCD121 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — A row of 1728 Image sensor elements separated by diffused channel stops and covered by a silicon photogate. Image photons pass through the transparent polycrystalline silicon photogate and are absorbed in the single crystal silicon by hole-electron pair production. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated is a linear function of the incident illumination intensity and the integration period. The output signal will vary in this analog manner from a thermally generated noise background at zero illumination to a maximum at saturation.

Two Transfer Gates — Gate structures adjacent to the row of Image Sensor Elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gates to the transport registers. Alternating charge packets are transferred to the right and left (A and B) analog transport shift registers. The HIGH states of the transfer-gates must be contained by the HIGH state of the transport shift register clocks. The next light integration period is started when transfer gates go LOW.

Two 866-Bit Analog Shift Registers — One on each side of the row of Image Sensor Elements and separated from it by a Transfer Gate. The two registers are used to move the image generated charge packets serially from the sensor elements to the charge detector/preamplifier. The phase relationship of the last elements of the two shift registers provide for alternate delivery of charge packets to re-establish the serial sequence of the photosites.

A Gated Charge Detector/Preamplifier — Charge packets are transported to a precharged diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor producing a signal output at OS. The reset transistor is driven by a reset clock (ϕR) so as to recharge the charge-detector diode capacitance before the arrival of each new signal charge packet from the transport registers.

Generation of the necessary waveforms to operate the device is explained in detail in the CCD121 Board Brochure that includes a typical drive circuit diagram, a printed copy of the layout of a two-sided PC board, a parts list of components that are needed to build the board and oscilloscope photographs of the driving waveforms.

DEFINITION OF TERMS

Charge Coupled Device — A charge coupled device is a semiconductor device in which isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Gate Clock ϕ_{XA}, ϕ_{XB} — The voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD shift registers.

Analog Shift Register Transport Clocks, ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B} — The two sets of 2-phase clock applied to the gates of the CCD shift registers to move the charge packets received from the image sensor elements to the gated charge-detecting preamplifier.

Gated Charge Detector Preamplifier — The output circuit of the CCD121 which receives the charge packets from the CCD shift registers and provides a signal voltage proportional to the size of each charge packet. Before each new charge packet is sensed, a reset clock returns the output voltage to a base level.

Reset Clock ϕ_R — The voltage waveform required to drive the gated charge detector preamplifier.

Dynamic Range — The saturation exposure divided by the peak to peak noise equivalent exposure.

This does not take into account dark signal non-uniformities or average dark signal.
Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of 4 to 6 is generally appropriate. (Peak to peak noise is approximately equal to 4 to 6 times rms noise.)

DEFINITION OF TERMS (Cont'd)

Peak to Peak Noise Equivalent Exposure – The exposure level which gives an output signal equal to the peak to peak noise level at the output in the dark.

Saturation Exposure – The minimum exposure level that will produce a saturated output signal. Saturation exposure is equal to the light intensity times the photosite integration time.

Spectral Response Range – The spectral band in which the response per unit of radiant power is more than 10% of the peak response.

Responsivity – The output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Photoresponse Non-uniformity – The difference of the response levels of the most and the least sensitive element under uniform illumination. This is commonly expressed as a percentage of the saturation output voltage.

Average Dark Signal – The output signal level in the dark averaged over all elements and measured relative to the base line output voltage established by the reset clock. This is a linear function of the integration time. It is also strongly dependent on temperature. This is commonly expressed as a percentage of the saturation output voltage.

Dark Signal Non-uniformity – Maximum deviation of the output voltage of any element from the background level in the dark. This is commonly expressed as a percentage of the saturation voltage.

Saturation Output Voltage – The maximum signal output voltage.

Integration Time – The time interval between the falling edges of any transfer pulse ϕ_{XA} and ϕ_{XB} as shown in the timing diagram. The integration time is the time allowed for the photosites to collect charge.

Output Signal Range – The output signal range is defined as OSR = V_{sat} $-(t_{INT} + t_{Transfer})$ x Rate of Average Signal Offset where: t_{INT} = Integration Time; $t_{Transfer}$ = time necessary to transfer the charge packets from the analog shift registers and is equal to $\frac{1728}{f_{\phi R}}$. Integration time (t_{INT}) does not necessarily equal transfer time ($t_{Transfer}$). If long integration times are required, $t_{Transfer}$ should be minimized (increase $f_{\phi R}$) to maximize OSR.

Average Signal Offset – Average signal offset is a dc offset of the output voltage (due to the average leakage current in the CCD registers) which increases linearly with the transfer time.

TEST LOAD CONFIGURATION

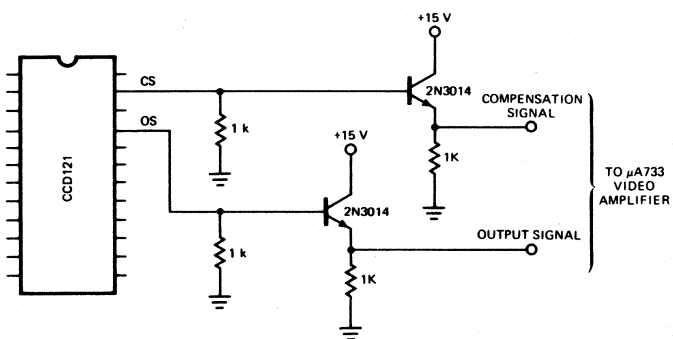


Fig. 1

DC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{OG}	Output Gate Voltage		6.0			Note 1
V_{PG}	Photogate Voltage		9.0		V	Note 2
TP1, TP3	Test Points		0.0		V	
TP2, TP4	Test Points	14.5	15.0	15.5	V	

CLOCK CHARACTERISTICS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi 1AL}$, $V_{\phi 1BL}$ $V_{\phi 2AL}$, $V_{\phi 2BL}$	Analog Shift Register Transport Clocks LOW	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi 1AH}$, $V_{\phi 1BH}$ $V_{\phi 2AH}$ $\phi 2BH$	Analog Shift Register Transport Clocks HIGH		8.0			Notes 3, 4, 12
$V_{\phi XAL}$	Transfer Gate Clock LOW	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi XAH}$	Transfer Gate Clock HIGH		8.0		V	Notes 3, 4, 12
$V_{\phi RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Notes 3, 4
$V_{\phi RH}$	Reset Clock HIGH		10.0		V	
$f_{\phi 1A}$, $f_{\phi 1B}$ $f_{\phi 2A}$, $f_{\phi 2B}$	Analog Shift Register Transport Clock Frequency		0.5		MHz	Notes 5, 6
$f_{\phi R}$	Reset Clock Frequency (Output Bit Rate)		1.0		MHz	Notes 5, 6

AC CHARACTERISTICS: $T_A = 25°C$, $f_{\phi 1} = f_{\phi 2} = 0.5$ MHz, $f_{\phi R} = 1$ MHz, $t_{INT} \cong 1.94$ ms, $t_{TRANSFER} = 1.73$ ms

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range		500			Notes, 7, 8, 9
NEE	Peak-to-Peak Noise Equivalent Exposure		1×10^{-3}		$\mu J/cm^2$	Notes 8, 9
SE	Saturation Exposure		0.5		$\mu J/cm^2$	Notes 8, 9
SR	Spectral Response Range Limits	0.45		1.05	μm	
R	Responsivity		0.4		V per $\mu J/cm^2$	Note 13
PRNU	Photoresponse Non-uniformity		±6	±10	% of V_{sat}	Note 10
ADS	Average Dark Signal		2		% of V_{sat}	
DSNU	Dark Signal Non-uniformity		3		% of V_{sat}	
V_{sat}	Saturation Output Voltage	100	200		mV	Note 11
P	Power Dissipation		100		mW	$V_{OD} = 15$ V
Z	Output Impedance		1000		Ω	
N	Peak-to-Peak Noise		400		μV	
RSO	Rate of Average Signal Offset		1		mV/ms	

NOTES:
1. Adjustment in the range of 4 V to 8 V may be required for optimum operation.
2. Adjustment in the range of 5 V to 12 V may be required for optimum operation.
3. Negative transients on the clocks below 0.0 V may cause an increase in apparent dark signal.
4. $C_{\phi XA} = C_{\phi XB} = C_{\phi 1A} = C_{\phi 1B} = C_{\phi 2A} = C_{\phi 2B} \cong 400$ pF. $C_{\phi R} \cong 1.5$ pF.
5. The resulting data output frequency $f_{\phi R}$ is twice that of each analog shift register clock, $f_{\phi 1A}$, $f_{\phi 2A}$, $f_{\phi 1B}$, $f_{\phi 2B}$.
6. Clock rates shown are typical rates at which the device operates. Operation of the devices at lower or higher frequencies will not damage the device.
7. T_{int} = integration time ≅ 1.94 ms.
8. The dynamic range is measured by taking the ratio of the saturation output voltage to the peak-to-peak noise of the device in the dark. Because of the high degree of linearity of the device the dynamic range measurement is also approximately equal to the ratio of the saturation exposure to the peak-to-peak noise equivalent exposure.
9. 1 μ J/cm^2 = 0.02 fcs at 2854°K. 1 fcs = 50 μ J/cm^2 at 2854°K.
10. Measurement is done at 50% of saturation output level. Measurement excludes first and last elements.
11. See Fig. 1 for test load configuration.
12. Adjustment in the range of 6 V to 10 V may be required for optimum operation.
13. See definition of terms.

OUTPUT SIGNAL LEVEL VS. INTEGRATION TIME
2854°K TUNGSTEN SOURCE

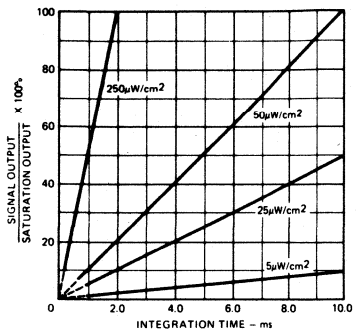


Fig. 2

PHOTOELEMENT DIMENSIONS

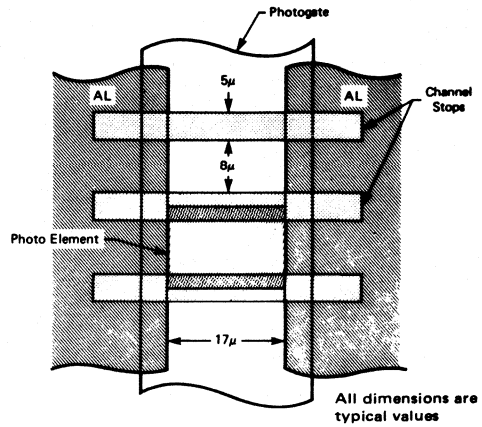
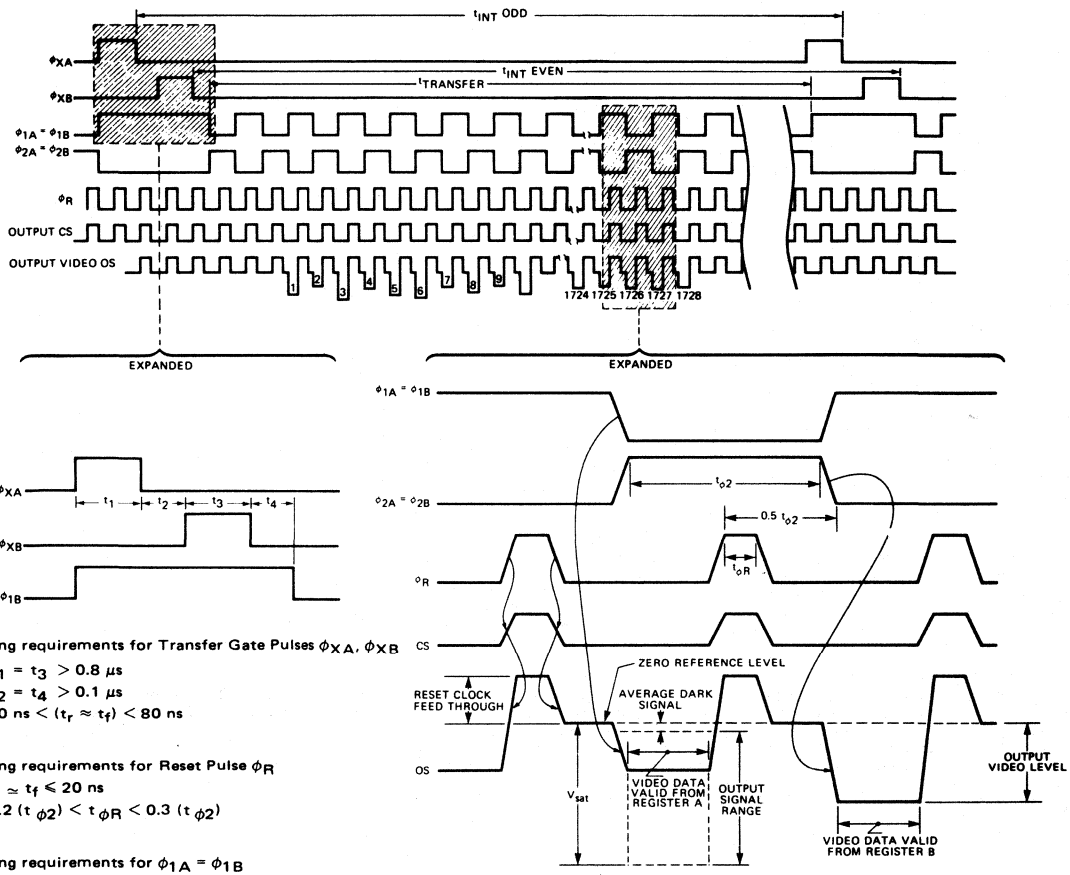


Fig. 3

TIMING DIAGRAM DRIVE SIGNALS



Timing requirements for Transfer Gate Pulses ϕ_{XA}, ϕ_{XB}

$t_1 = t_3 > 0.8\ \mu s$

$t_2 = t_4 > 0.1\ \mu s$

$20\ ns < (t_r \approx t_f) < 80\ ns$

Timing requirements for Reset Pulse ϕ_R

$t_r \simeq t_f \leq 20\ ns$

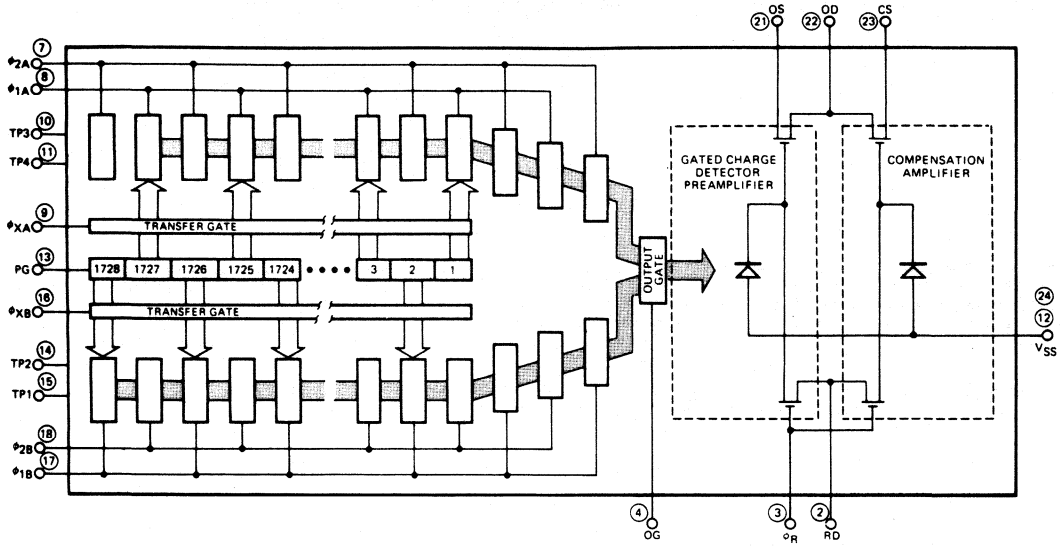
$0.2\ (t_{\phi 2}) < t_{\phi R} < 0.3\ (t_{\phi 2})$

Timing requirements for $\phi_{1A} = \phi_{1B}$

$20\ ns < (t_r \approx t_f) < 100\ ns$

Fig. 4

CIRCUIT DIAGRAM



○ = Lead Numbers

Fig. 5

CCD201
100 × 100-ELEMENT SELF-SCANNING IMAGE SENSOR

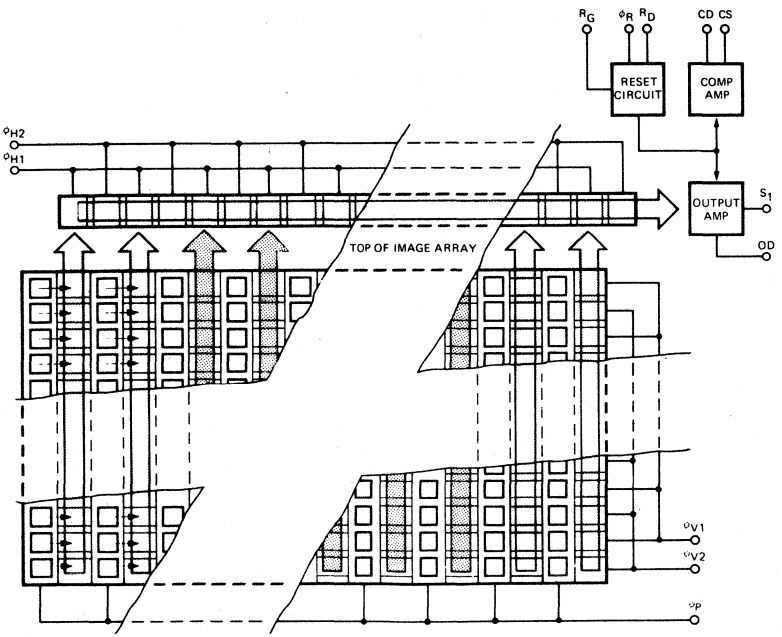
GENERAL DESCRIPTION — The CCD201 is a 2-Phase 10,000-Element Self-Scanning Image Sensor. It uses charge coupled technology with buried channels and ion-implanted barriers. The light sensitive area is a 100 x 100 array of photo elements which provide an image aspect ratio of 4 x 3. The image sensing elements are 1.2 mils x 0.8 mils located on 1.2 mil vertical centers and 1.6 mil horizontal centers.

In addition to the image sensing array, the CCD201 chip includes: 100 columns of 2-phase analog shift registers interdigitated in the photosensor array, a 102-element 2-phase analog output shift register, an output detector/preamplifier and a compensation output amplifier.

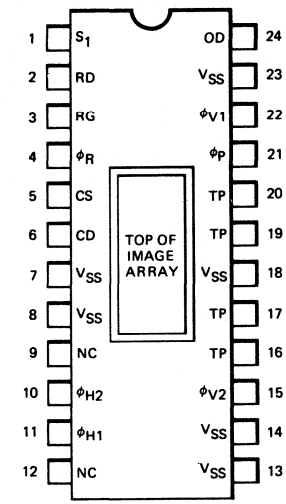
The device is packaged in a 24-Pin Dual In-line Package with an optical glass window.

- **2-PHASE CLOCK OPERATION**
- **100 x 100-ELEMENT ARRAY ON A SINGLE CHIP**
- **INTERLACED SELF SCANNING**
- **ALL OPERATING VOLTAGES UNDER 20 V**
- **ON-CHIP VIDEO PREAMPLIFIER AND COMPENSATION CIRCUIT**
- **LOW POWER 50 mW TYP**
- **PACKAGED IN 24-PIN DIP WITH OPTICAL GLASS WINDOW**

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



PIN NAMES

S_1	Output Amplifier Source
RD	Reset Drain
RG	Reset Gate
ϕ_R	Reset Clock
CS	Compensation Amplifier Source
CD	Compensation Amplifier Drain
ϕ_{H1}, ϕ_{H2}	Horizontal Register Clocks
ϕ_{V1}, ϕ_{V2},	Vertical Clocks
ϕ_P	Photogate Clock
OD	Output Amplifier Drain
TP	Production Test Points

FUNCTIONAL DESCRIPTION – The CCD201 consists of the following functional subsections as illustrated in the Block Diagram:

1. 10,000 image sensors in a 100 x 100 array
2. 100 Columns of 2-phase vertical analog shift registers interdigitated with the photosensor array.
3. A 102-element 2-phase horizontal analog output shift register charge coupled to the output of each of the 100 column shift registers.
4. A gated charge detector output preamplifier which detects and converts the charges delivered to a video output voltage at terminal S_1.
5. A compensation output amplifier that provides the capability for differential amplification and suppression of reset clock noise in the video output.

Light energy incident on the image sensor elements generates a packet of electrons in each element. Electrical clocking of the photogate, 2-phase vertical transport registers, and 2-phase horizontal output register delivers the charge packet from each photoelement to the gated charge detector preamplifier which provides a video signal output. The reset clock pulse is proportionately amplified by the compensation amplifier and is provided for suppression purposes. Detailed descriptions of the functional subsections follow.

Image Sensor Elements – Image photons pass through the transparent polycrystaline silicon photogate and are absorbed in the single crystal silicon by hole-electron pair production. The resulting photo electrons are accumulated in the photosites during the HIGH state of the photogates. The duration of this HIGH state is the integration period. The amount of charge accumulated is a linear function of the incident illumination intensity and the integration period. The output signal will vary in this analog manner from a thermally generated noise background at zero illumination to a maximum at saturation.

2-Phase Vertical Shift Registers – At the end of the integration period, the photogate voltage (ϕP) is lowered and alternate vertical site charge packets (corresponding to one field, i.e., the odd-numbered photoelements) are transferred to their associated vertical shift register. They are then transported to the output register, a row at a time, by the vertical clocks (ϕ_{V1} & ϕ_{V2}). Fifty vertical transfers are required to remove one field of information from the vertical register. Subsequent to removal of one field of information, a second frame cycle is instituted to gather the information from photosites corresponding to the other field (i.e., the even numbered photoelements).

Output Shift Register – The output register is a 102-element 2-phase analog shift register clocked at over 102 times the vertical shift register frequency. As each row of information is transferred from the column registers to the output register, it is serially moved to the output amplifier by the horizontal clocks (ϕ_{H1} & ϕ_{H2}). A minimum of 102 horizontal clock pulse sets are required to complete one row of information transfer to the gated charge detector.

Gated Charge Detector and Output Preamplifier – The output shift register data (in the form of charge packets) are applied to a precharged diode where the potential is changed linearly in response to the quantity of signal charge delivered. This potential is applied to the gate of the output n-channel MOS transistor which produces a signal output at S_1. The dual gate reset circuit is clocked by reset signal (ϕ_R) and recharges the charge-detector diode capacitance during the interval between transfer of signal charge packets from the output register.

Compensation Amplifier – An additional output amplifier is driven with only the reset signal (ϕ_R) to provide an output at CS which is similar in wave shape to the reset transient contained in the video signal output. This can be used to suppress the reset clock noise by use of a differential amplifier in the external video circuitry.

DRIVE CIRCUITRY – Figure 6 gives the basic timing and drive voltages required to operate the CCD201. Outputs are also available for X–Y oscilloscope deflection to form a raster which displays the area sensor's video output. The amplified output of the CCD201 is applied to the Z axis input of the oscilloscope.

One-half of a 9016 Hex Inverter is the master oscillator which runs at twice the horizontal clocking frequency (a crystal oscillator could be used for better stability). The oscillator frequency should be between 200 kHz and 8 MHz. This master clock drives the horizontal counter which consists of a pair of 9316s counting modulo 224 (14 x 16). This is equivalent to 112 horizontal drive pulses (ϕ_H) which are at half the clock frequency. The divide by 224 is accomplished by preloading the first counter to 2 when it reaches a full count, making it effectively a count by 14. The output of the first stage acts as a divide by 2 counter to provide the horizontal drive pulses (ϕ_H). IC 8 provides both the reset clock ($\overline{\phi_R}$) and the delay necessary to compensate for the delay through the first stage of the counter. The reset clock ($\overline{\phi_R}$) is a 25% duty cycle signal used to precharge the detector diode of the CCD device. The sample and hold clock ($\overline{\phi_S}$), also generated by IC 12, is to be used in a sample and hold amplifier to smooth the CCD201 video output.

The terminal count of IC 3 is true for 7 horizontal clock (ϕ_H) pulses and is used as the CRT horizontal retrace period. The ϕ_{H1} and ϕ_{H2} outputs consist of strings of 105 pulses used to shift out the horizontal information before the vertical shift pulse refills the register with the next line of information.

The Q_3 output of the second 9316 counter (IC 3) is inverted and used to clock the vertical counters. IC 4 and 5 count the vertical lines and keep track of the odd and even fields. The first seven stages of the counter are counting modulo 51. This is accomplished by preloading the 2s complement of the modulo into the first six stages of this counter when the Q_2 output of IC 5 has gone LOW. When the Q_2 output went LOW, the last stage of the counter was incremented. Q_2 activates the Parallel Enable input which on the next clock pulse loads a binary 13 into the first six stages, presents Q_2 back to a HIGH state, but retains the information in Q_3, since it is reloaded from its own output.

Q_3 effectively is a toggle flip-flop driven by the Q_2 output and acts as odd/even field identifier. IC 7 (a 9309 Dual 4-Input Multiplexer) is used as a combinatorial logic element to derive from the outputs of the various counters, the drive signals for the discrete drivers and the sweep circuits.

Horizontal sweep output for the oscilloscope is generated by a μA748 fast operational amplifier acting as an integrator. The values shown in Figure 6 are selected to be compatible with a 2 MHz oscillator and a 1 MHz horizontal drive frequency. The integration capacitor must be increased if the oscillator frequency is lowered and decreased if the frequency is raised significantly. The transistor driving the input to the operational amplifier force a discharge of the integration capacitor. The vertical integrator is similar in function but is much slower and a μA741 is sufficient. Since the output voltage increases positively with time, the inverted polarity should be used on the oscilloscope to form a normal raster. The capacitor on this sweep generator must be changed with a frequency change as outlined above. On the odd fields, the sweep is allowed to start early, this forms the line interlacing on the monitoring oscilloscope.

Composite blanking is available to blank the video signal on horizontal and vertical retrace in a video amplifier.

The transistor devices and the SH0013 provide the necessary complementary signals with the proper capacitive drive capability.

This circuit is intended to provide a starting point for circuit development and as such does not necessarily provide the optimum drive voltage to the CCD201. Note that all drive voltages are of the same level, controlled by the setting of the –8.5 V supply. Individual adjustment of $V_{\phi PL}$, $V_{\phi VL}$, $V_{\phi HL}$ and $V_{\phi RL}$ will optimize the CCD201's performance.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−25°C to +100°C
Operating Temperature	−25°C to +65°C
Clock Inputs	
Pins 7, 8, 13, 14, 18, 23	V_{SS} = 0V
Pins 1, 2, 5, 6, 24	+15V to −.6V
Pins 3, 4, 10, 11, 15, 21, 22	+15V to −10V

CAUTION:

Static discharge to any pin may cause permanent damage. Store in shorting clip or conductive foam. Use grounded soldering irons and tools. Personnel should wear grounding bracelets and avoid synthetic smocks and gloves.

FORCING FUNCTIONS: See Note 6

SYMBOL	PARAMETER	LIMITS			UNITS	COMMENTS
		MIN	TYP	MAX		
$f_{\phi H}$	Output (horizontal) Register Clock Frequency	0.1		4.0	MHz	
$V_{\phi HL}$	Horizontal Register Clock LOW Voltage	−10	−8.0		V	$C_{\phi H1} = C_{\phi H2} \approx 20$ pF
$V_{\phi HH}$	Horizontal Register Clock HIGH Voltage		+2.0	+10	V	
$V_{\phi VL}$	Vertical Register Clock LOW Voltage	−10	−8.0		V	$C_{\phi V1} = C_{\phi V2} \approx 1500$ pF
$V_{\phi VH}$	Vertical Register Clock HIGH Voltage		+2.0	+10	V	
$V_{\phi RL}$	Reset Clock LOW Voltage	−10	−8.0		V	$C_{\phi R} \approx 5$ pF
$V_{\phi RH}$	Reset Clock HIGH Voltage		+2.0	+10	V	
$V_{\phi PL}$	Photogate Clock LOW Voltage	−10	−8.0		V	$C_{\phi P} \approx 1500$ pF
$V_{\phi PH}$	Photogate Clock HIGH Voltage		+2.0	+10	V	
V_{RD}	Reset Transistor Drain Bias Voltage		+12	+15	V	
V_{OD}	Output Transistor Drain Bias Voltage		+12	+15	V	
V_{RG}	Reset Gate Bias Voltage		+12	+15	V	
V_{CD}	Compensation Amplifier Drain Voltage		+12	+15	V	

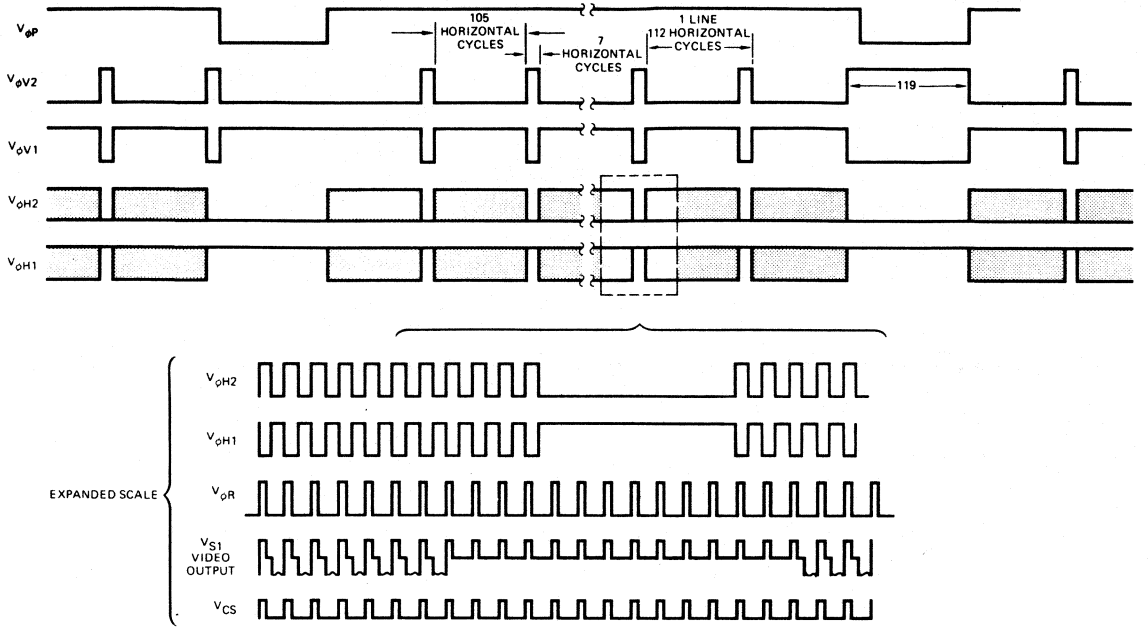
OPERATING CHARACTERISTICS: V_{SS} = 0 V, T_A = 25°C, R_L = 1 k from S_1 to Ground, See Note 5.

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
	Dynamic Range	100	200			Note 1
	Responsivity	400	600		mV/ftc	Notes 1 & 2
	Spectral Response Range	480		1100	nm	
	Saturation Exposure		3.125×10^{-3}		ftcds	Notes 1 & 2
	Photo Response Non-Uniformity			±15	%	Notes 1 & 4
	Average Dark Signal		5.0		mV	Notes 1 & 4
	Modulation Transfer Function		0.6			Notes 1 & 3
V_O	Saturation Output Voltage	50	75		mV	Note 1
P_D	Power Dissipation		50		mW	

NOTES:

1. $f_{\phi H}$ = 500kHz, $f_{\phi V}$ = 4.5 kHz, $f_{\phi P}$ = 40 Hz.
2. Tungsten Light source at 2854°K color temperature.
3. Measured with 100% contrast test pattern at 70 lines resolution.
4. Elements in the outer columns (1 and 100), due to edge effects, may exceed these parameters.
5. 16, 17, 19 and 20 are test points used during production. During normal operation they must be connected as follows:
   Pin 16 to 6 or equivalent voltage.
   Pins 13, 19 and 20 to V_{SS}.
6. Optimum performance will be realized by adjustment of clock voltage levels. Adjustment of $V_{\phi PL}$, $V_{\phi VL}$, $V_{\phi HL}$ and $V_{\phi RL}$ will have the most significant effect on performance.

TIMING DIAGRAM | DRIVE SIGNALS



TYPICAL PERFORMANCE CURVES

VIDEO SIGNAL FROM A SINGLE LINE

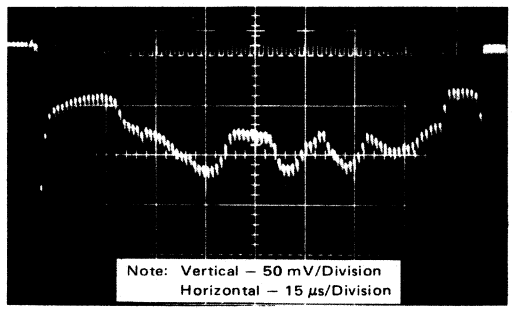


Fig. 2

SPECTRAL RESPONSE

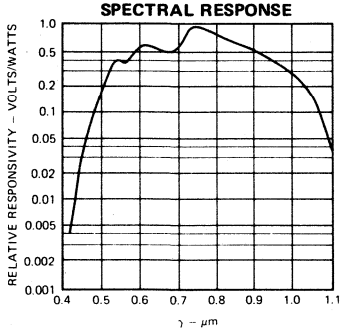


Fig. 3

MODULATION TRANSFER FUNCTION

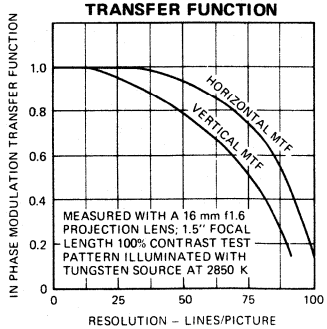


Fig. 4

NOISE EQUIVALENT POWER

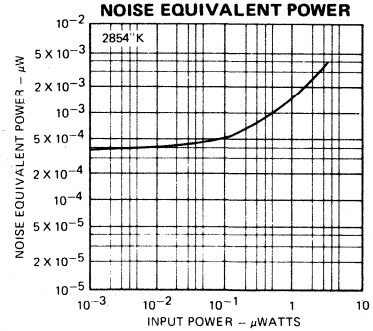


Fig. 5

FREQUENCY AND PULSE GENERATING CIRCUITS

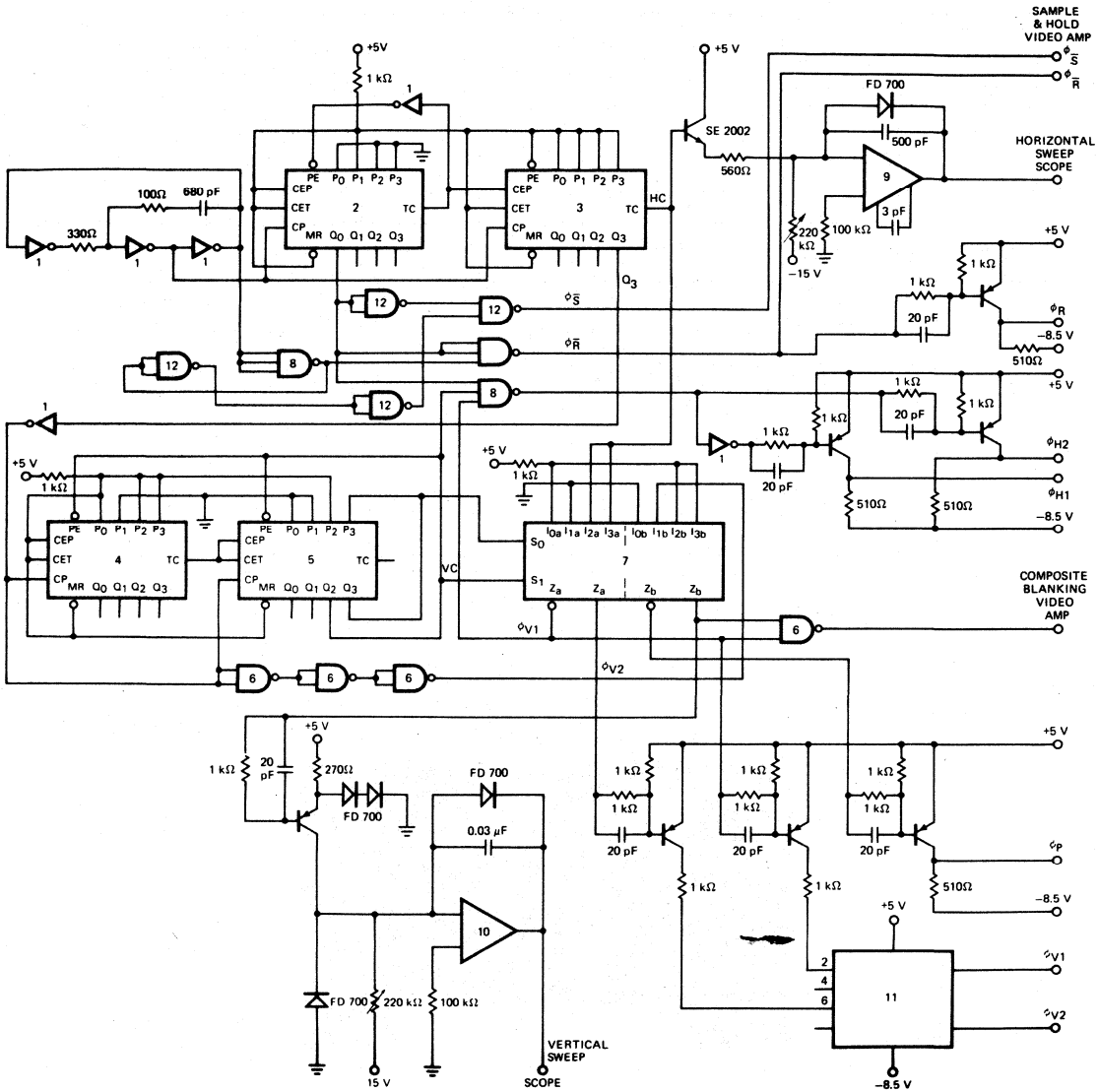


Fig. 6

Parts List

IC 1	9016
IC 2, 3, 4, 5	9316
IC 6, 12	9002
IC 7	9309
IC 8	9003
IC 9	μA748
IC 10	μA741
IC 11	SH0013
All PNPs	2N5910

CLASSIFICATIONS – Image Sensors are classified in terms of the maximum number of defective photosites allowed and their position in the array. The array is divided into three zones (see Fig. G), since defects near the periphery of the array are usually less objectionable than those near the center.

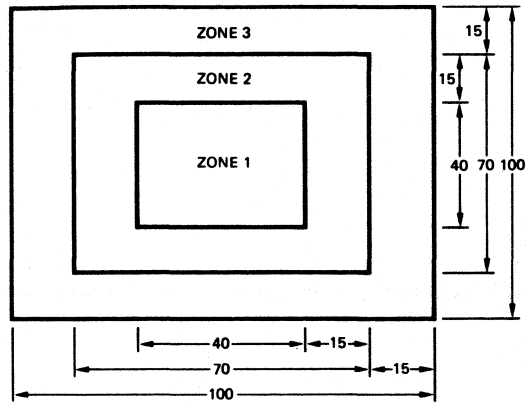
The following classification tables specify the maximum number of defects by size and position in the array.

CCD201ADC – CLASS A

Maximum Number of Elements in Cluster	Maximum No. of Clusters per Zone		
	Zone 1 16% of Area	Zone 2 33% of Area	Zone 3 51% of Area
4	0	0	1
2	0	1	2
1	0	3	5

CCD201BDC – CLASS B

Maximum Number of Elements in Cluster	Maximum No. of Clusters per Zone		
	Zone 1	Zone 2	Zone 3
9	0	0	1
6	0	0	2
4	0	1	2
2	0	2	3
1	2	5	9



All dimensions in Elements

Fig. 7

CCD311

130/260 BIT ANALOG SHIFT REGISTER

GENERAL DESCRIPTION – The CCD311 is a buried channel charge coupled device intended to be used in analog signal processing systems that include delay and temporary storage of analog information.

The CCD311 consists of two 130 bit analog shift registers each with its own charge injection port and sampling control enabling manipulation of a total of 260 bits of analog data. The chip includes a single preamplifier and a compensation output amplifier and is packaged in an 18-pin Dual In-line Package.

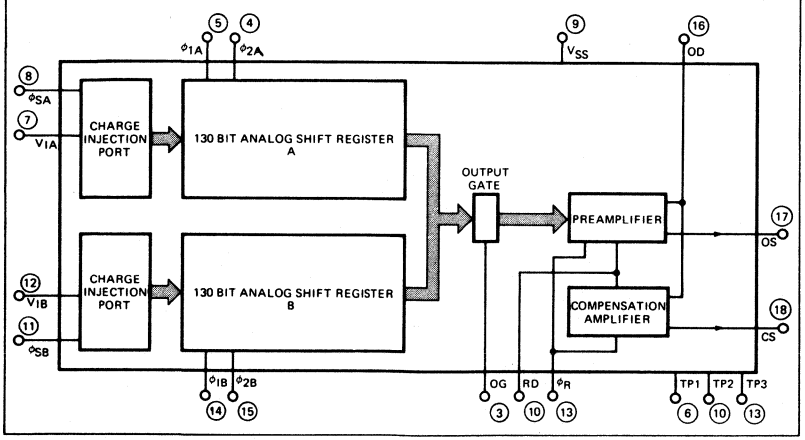
- **130 OR 260 BITS OF ANALOG DELAY ON A SINGLE CHIP**
- **TWO SEPARATE CHARGE INJECTION PORTS**
- **GREATER THAN 10 MHz SAMPLING RATE**
- **SIGNAL-TO-NOISE RATIO OF GREATER THAN 50 dB**
- **ON-CHIP OUTPUT BUFFER AMPLIFIER**

ABSOLUTE MAXIMUM RATINGS

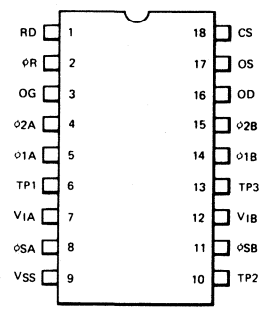
Storage temperature	−25°C to 100°C
Pins 2, 3, 4, 5, 7, 12, 14 and 15	−0.3 V to 12 V*
Pins 1, 8, 11, 16, 17 and 18	−0.3 V to 18 V*
Pins 6, 9, 10 and 13	Ground

*Note: with respect to ground.

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



V_{SS} = Pin 9

PIN NAMES

ϕ1A, ϕ2A ϕ1B, ϕ2B	Analog Shift Register Transport Clocks
OG	Output Gate
OS	Output Transistor Source
OD	Output Transistor Drain
CS	Compensation Transistor Source
ϕR	Reset Transistor Gate Clock
RD	Reset Transistor Drain
V_{SS}	Substrate (Ground)
V_{IA}, V_{IB}	Analog Input Gates
ϕSA, ϕSB	Analog Sample Clocks
TP1, TP2, TP3	Test Points

Caution: The device has limited built-in gate protection. It is recommended to control and minimize static charge build-up. Care should be taken to avoid shorting pins OS and CS to ground during operation of the device. Pins 6, 9, 10 and 13 should be externally grounded during operation.

FUNCTIONAL DESCRIPTION – The CCD311 consists of the following functional elements illustrated in the Block Diagram:

Two Charge Injection Ports – The analog information in voltage form is applied to two input ports at V_{IA} and V_{IB} Upon the activation of the analog sample clocks ϕ_{SA} and ϕ_{SB} a charge packet linearly dependent on the voltage applied at the port input is injected into its corresponding 130 bit analog shift register.

Two 130 Bit Analog Shift Registers – These registers transport the charge packets from the charge injection ports to a gated charge detector. Transport of charge packets is accomplished by external clocking of the registers. Analog shift register A is clocked by ϕ_{1A} and ϕ_{2A}. Similarly register B is clocked by ϕ_{1B} and ϕ_{2B}.

A Differential Gated Charge Detector/Preamplifier – Charge packets from the analog shift registers are delivered to the gated charge detector. A reset transistor in the gated charge detector is driven by the external reset clock (ϕ_R).

MODES OF OPERATION

130-Bit Analog Delay – Either 130 bit Analog Shift Register (A or B) can be operated as an analog delay line. The driving waveforms to operate shift register A is shown in Fig. 3. The input voltage signal is applied directly to V_{IA}. The Analog Sample Clock ϕ_{SA} samples this input voltage and injects a proportional amount of charge packet into the first bit of Register A. The input voltage A1 which is sampled between t = 0 and t = tc, appears (inverted) at the output terminal OS at t = 260 tc. A2 appears at t = 262 tc, and so on. A reset clock ϕ_R is applied in order to recharge the charge detector diode of the gated charge detector before the arrival of each charge packet from the transport register. This reset clock is capacitively coupled on chip into the output waveform OS. Terminal CS provides the reset clock so that off chip differential amplification can be used to remove reset clock coupling from the video waveform. When only the A register is used, ϕ_{1B}, ϕ_{2B} and V_{IB}, should be grounded, and ϕ_{SB} = 15 Vdc.

Shift register B can be operated in the analogous fashion as shown in Fig. 4. When only the B register is used, ϕ_{1A}, ϕ_{2A} and V_{IA} should be grounded and ϕ_{SA} = 15 Vdc.

260-Bit Analog Delay – The two registers can be multiplexed to double the sampling rate of an input voltage signal. Fig. 5 in the timing diagram shows the relationship of the timing waveforms for this mode of operation. Here $\phi_{1A} = \phi_{1B}$, $\phi_{2A} = \phi_{2B}$, ϕ_{SA} and ϕ_{SB} are clocked as before. The same input signal voltage is applied to both V_{IA} and V_{IB}. Between t = 0 and t = tc, the input signal voltage A_1 is sampled by register A. Between t = tc and t = 2tc, the input signal voltage B_1 is sampled by register B. The charge packet corresponding to A_1 appears at the output at t = 260tc and the charge packet corresponding to B_1 appears at a t = 261tc. The gated charge integrator has to be recharged twice as often, ϕ_R has to be clocked at twice the original frequency.

When the device is operated in the multiplexed mode, it is recommended to provide at least one dc level control on the two inputs (V_{IA} or V_{IB}) to balance the two input ports.

TEST LOAD CONFIGURATION

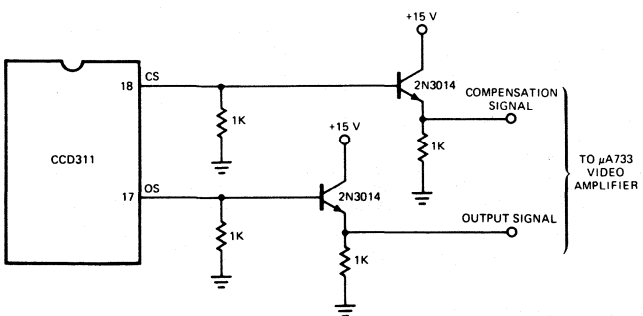


Fig. 1

OUTPUT SIGNAL RANGE VS. RESET CLOCK FREQUENCY $f_{\phi R}$

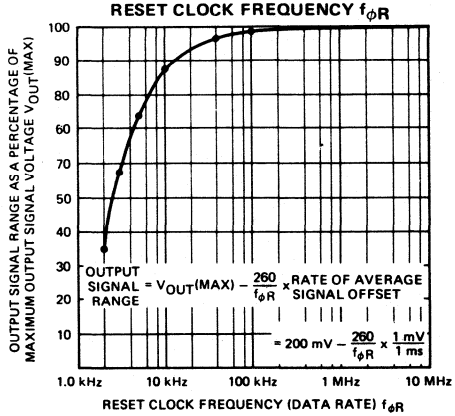


Fig. 2

DC CHARACTERISTICS $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{OD}	Output Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{RD}	Reset Transistor Drain Voltage	14.5	15.0	15.5	V	
V_{OG}	Output Gate Voltage		5.0		V	Note 3
R_{IN}	Input Resistance (Injection Port)		1		MΩ	Resistance from Pins 7 or 12 to Ground, Note 10
C_{IN}	Input Capacitance (Injection Port)		3		pF	Capacitance from Pin 7 or 12 to Ground, Note 10
TP1, TP2, TP3	Test Points		0.0		V	

CLOCK CHARACTERISTICS $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi 1AL}$, $V_{\phi 1BL}$ $V_{\phi 2AL}$, $V_{\phi 2BL}$	Analog Shift Register Transport Clocks LOW	0.0	0.5	0.8	V	Note 1
$V_{\phi 1AH}$, $V_{\phi 1BH}$ $V_{\phi 2AH}$, $V_{\phi 2BH}$	Analog Shift Register Transport Clocks HIGH	9.5	10.0	10.5	V	Note 1
$V_{\phi RL}$	Reset Clock LOW	0.0	0.5	0.8	V	Note 2
$V_{\phi RH}$	Reset Clock HIGH	10.0	11.0	12.0	V	Notes 2, 9
$V_{\phi SAL}$, $V_{\phi SBL}$	Analog Sample Clock LOW	4.5	5.0	5.5	V	
$V_{\phi SAH}$, $V_{\phi SBH}$	Analog Sample Clock HIGH	9.5	10.0	10.5	V	
V_{IA}, V_{IB}	Analog Input Gate Range		0.3–1.3		V	Note 4

AC CHARACTERISTICS $T_A = 25°C$, $R_L = 1$ k All parameters measured in a multiplex mode with balanced inputs and $F_{\phi R} = 10$ MHz

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
$f_{\phi 1A}$, $f_{\phi 1B}$ $f_{\phi 2A}$, $f_{\phi 2B}$	Analog Shift Register Transport Clock Frequency		5		MHz	See Fig. 2
$f_{\phi R}$	Reset Clock Frequency		10		MHz	Note 5
$f_{\phi SA}$, $f_{\phi SB}$	Analog Sample Clock Frequency		5		MHz	Note 6
BW	Input Signal Bandwidth (3 dB down)		4		MHz	Note 7
IL	Insertion Loss		15		dB	
NL	Non-Linearity		5		%	
S/N	Signal to Noise Ratio		50		dB	
RSO	Rate of Average Signal Offset		1		mV/ms	
V_{OUT} (max)	Maximum Output Signal Voltage		200		mV	Note 8

NOTES:
1. $C_{\phi 1A} = C_{\phi 1B} = C_{\phi 2A} = C_{\phi 2B} \cong 50$ pF = capacitance with respect to ground.
2. $C_{\phi R} \cong 1.5$ pF = capacitance with respect to ground.
3. Adjustment in the range of 4 V –6 V is required for optimum performance.
4. dc bias adjustment in the range of 0 V –2.5 V may be necessary for a 1 V Analog Input Gate Range in order to optimize non-linearity.
5. If the device is operated using either the A or B register only, then the $f_{\phi R}$ should be the same as $f_{\phi 1A}$, $f_{\phi 1B}$, $f_{\phi 2A}$, $f_{\phi 2B}$.
6. In a multiplex mode of operation $f_{\phi SA} = f_{\phi SB} = 5$ MHz typically (refer to timing diagram for phase relationships). In that case the total sampling rate on the input signal is 10 MHz.
7. For proper reconstruction of the input signal information, the sampling rate should be more than twice the input bandwidth. In a multiplex mode of operation and with a 4 MHz input bandwidth, $f_{\phi SA} = f_{\phi SB} = 5$ MHz, $f_{\phi R} = 10$ MHz and $f_{\phi 1A} = f_{\phi 1B} = f_{\phi 2A} = f_{\phi 2B} = 5$ MHz.
8. See test load configuration, Fig. 1.
9. $V_{\phi RH} \geq V_{RD} - 5.0$ V.
10. The signal acquisition time is not dependent upon the RC time constant of the input port.

TIMING DIAGRAMS

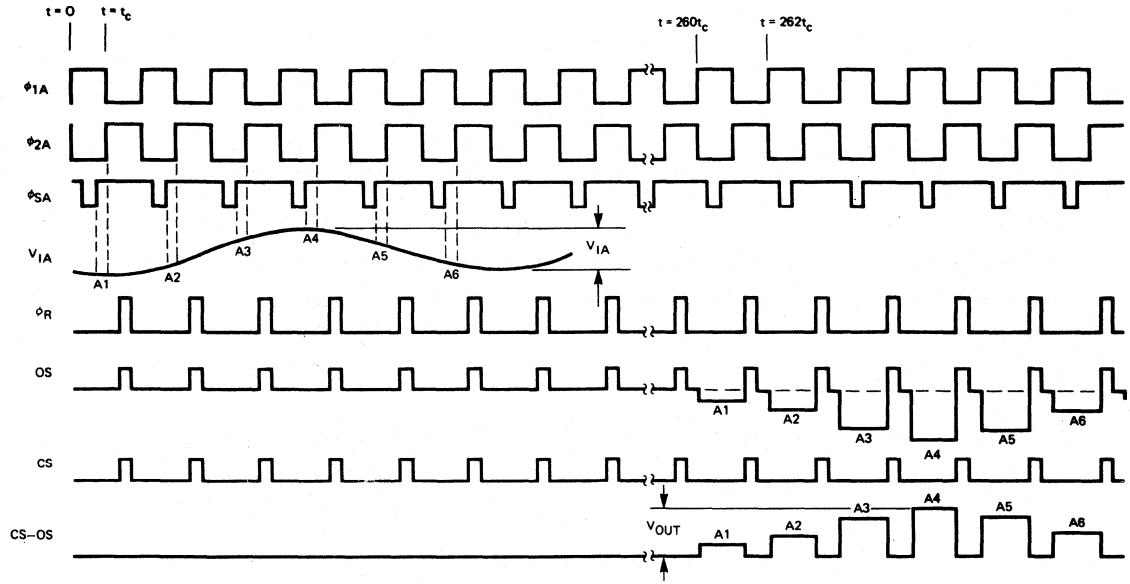


Fig. 3
ANALOG SHIFT REGISTER A OPERATION

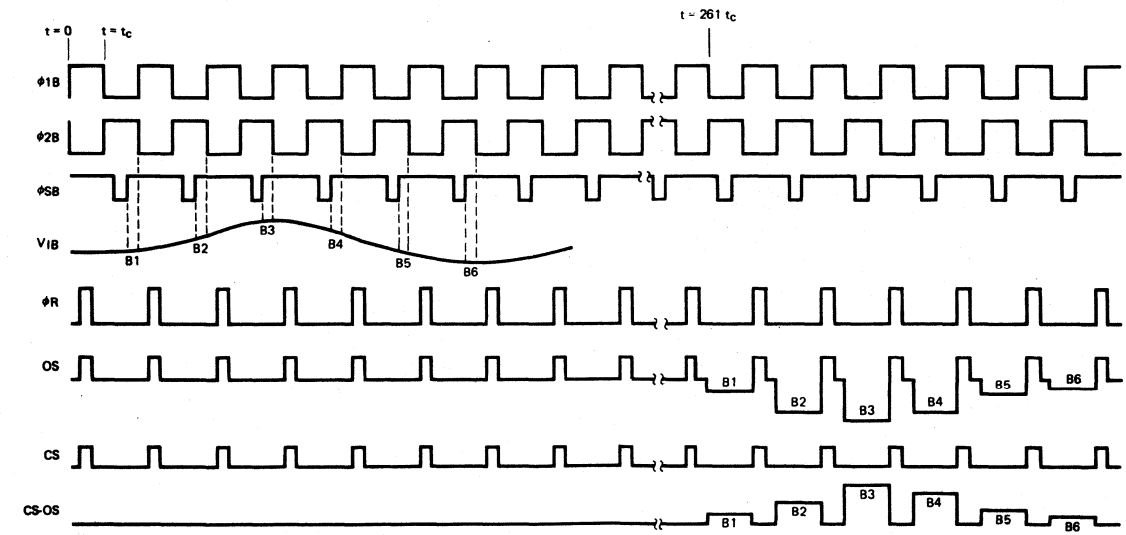
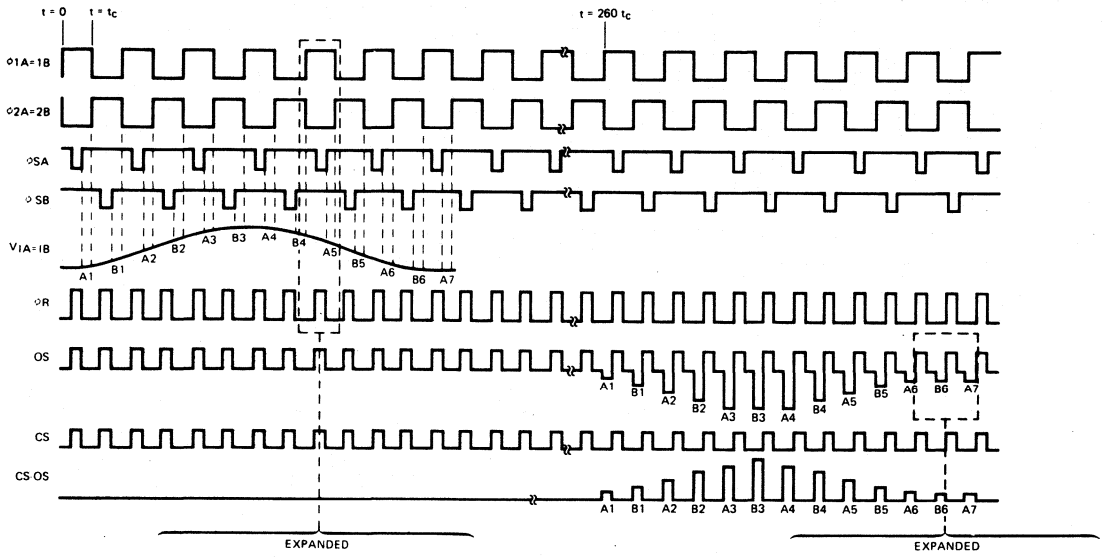
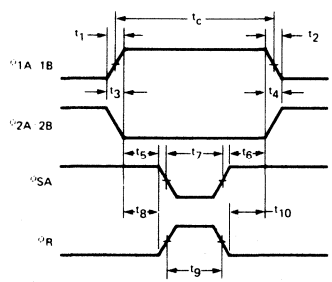


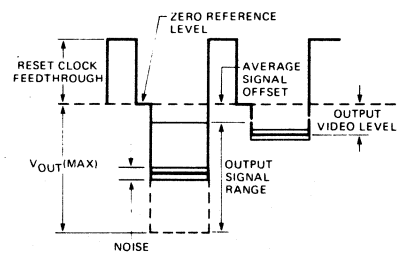
Fig. 4
ANALOG SHIFT REGISTER B OPERATION

TIMING DIAGRAMS (Cont'd)





t_1, t_2, t_3 and $t_4 \leq 1/3\ t_c$
t_5, t_6 and $t_{10} \geq 1$ ns
t_7 and $t_9 \geq 35$ ns

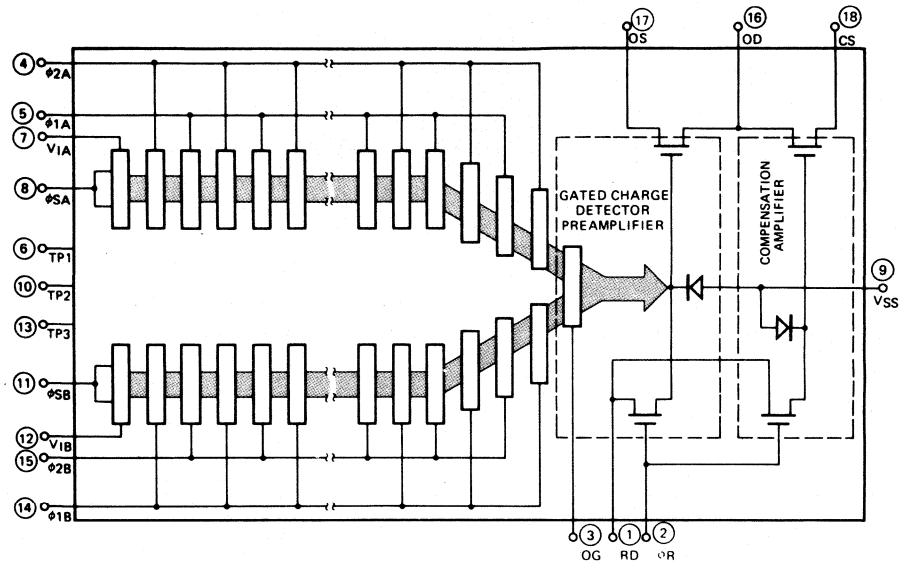


NOTE:

For multiplexed operation, the output signal appears during t_8. Therefore, it is recommended to maximize t_8.

Fig. 5
ANALOG SHIFT REGISTERS A & B MULTIPLEX OPERATION

CIRCUIT DIAGRAM



CCD311 DRIVE CIRCUITRY

Due to the flexibility of the CCD311 timing and clocking requirements various schemes can be used to clock the device. In particular the timing diagrams shown in *Figures 3, 4* and *5* are the most general timing relationships to operate the device. The typical drive circuitry shown in *Figure 6* generates a timing relationship as shown in *Figure 7*. This scheme is the simplest timing diagram for the device. The drive circuitry is intended for device operation (ϕ_R clock) of 10 kHz to 12 MHz (video rate). An external clock of twice the desired ϕ_R frequency is applied to IC1A and IC1B which are interconnected in a synchronous mode of counting. The clock is divided by 2 in IC1A. Pin 9 of IC1A is $\overline{\phi}_R$ which is connected to IC2 pin 11. IC2 is a quad TTL to MOS driver. The $\overline{\phi}_R$ pulse is inverted and level shifted which results in a ϕ_R pulse of approximately 0 to 10 V. The 68 pF capacitor on the ϕ_R line speeds up the rise time of ϕ_R. The output of IC1B is 1/2 of the ϕ_R frequency. IC1B pins 6 and 7 are $\overline{\phi}_1$ and $\overline{\phi}_2$ respectively. They are applied to pins 3 and 6 of IC2 where they are level shifted and inverted. This results in ϕ_1 and ϕ_2 clocks of 0 to 10 V amplitude.

ϕ_{SA} and ϕ_{SB} are generated by IC3. ϕ_{SA} is equal to $\overline{\phi_R \bullet \overline{\phi}_2}$. ϕ_{SB} is equal to $\overline{\phi_R \bullet \overline{\phi}_1}$. IC3 has the ground connection tied to +5 V. The V_{CC} connection is tied to +10 V. The pull-up resistors on the output insure a full 5 V swing. The ϕ_{SA} and ϕ_{SB} pulses out of IC3 swing from +5 V to +10 V. The sync pulse is buffered by IC3. The timing relation of the sync pulse is the same as ϕ_2. The inputs to IC3 are all capacitively coupled because of the level shift function. The 1 k resistors supply a zero signal reference. ϕ_1, ϕ_2 and ϕ_R have diode clamps to eliminate any clock excursions that may go below V_{SS}. The 22 Ω series resistors in the ϕ_1 and ϕ_2 lines smooth the rise and fall transitions. The input signal is capacitively coupled and routed through two dc bias circuits. This gives separate dc balance control for V_{IA} and V_{IB}.

The OS and CS outputs are terminated with 1 k load resistor. The 1 k pot at IC4 pin 1 adjusts the amount of CS fed to IC4 to balance the ϕ_R feedthrough in the OS signal. The 5 k pot between pin 4 and 11 of IC4 is a gain adjust. The output of the transistor buffer lowers the output impedance to drive a 50 Ω cable. The output should be terminated into 50 Ω.

In order to get the circuitry to operate properly, apply an external clock at a rate of 2X at the desired output video frequency. Observe the ϕ_R, ϕ_1 and ϕ_2 output waveforms and adjust the A power supply so that ϕ_1 and ϕ_2 will have a 10 V swing, ϕ_R should be about 1 V higher than ϕ_1 and ϕ_2. While observing the ϕ_{SA} and ϕ_{SB} pulses, adjust the B power supply for a swing of +5 V to +10 V on ϕ_{SA} and ϕ_{SB}. (Note: the potential between V_{CC} and the ground pin on IC3 should not exceed 5.5 V.) Next, adjust the V_{OG} adjust pot for +5 V on pin 3 of the CCD311 and adjust IC4 for minimum gain (≅ x 10). Ground the input port and adjust dc balance pots to 0 V. Observing the video output adjust the 1 k pot on IC4 pin 1 for minimum video output then adjust dc balance pots for 0.7 V. Apply a 0.5 V peak-to-peak sine wave at the signal input. The output video signal should be approximately 1 V peak-to-peak.

TYPICAL DRIVE CIRCUITRY

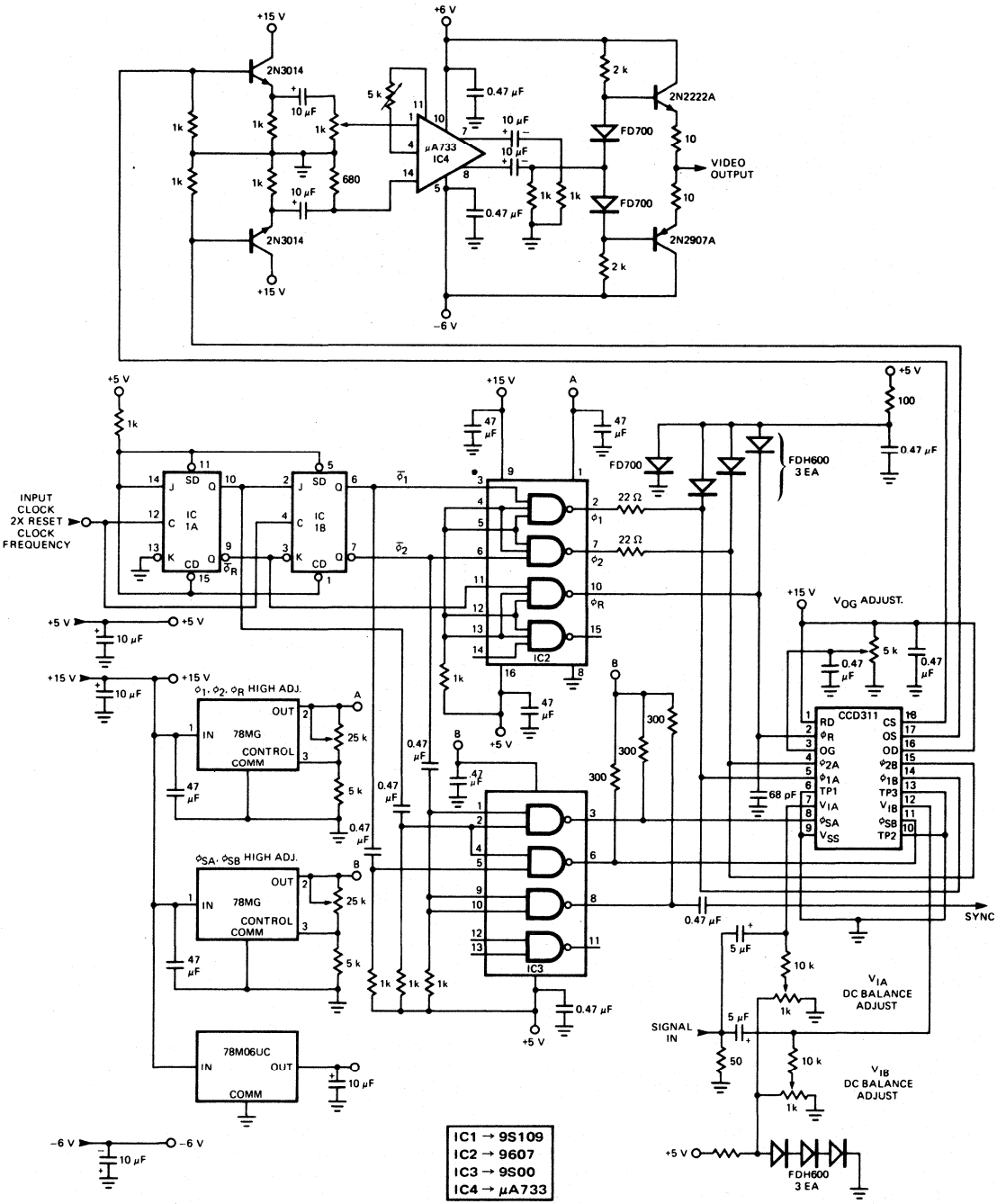
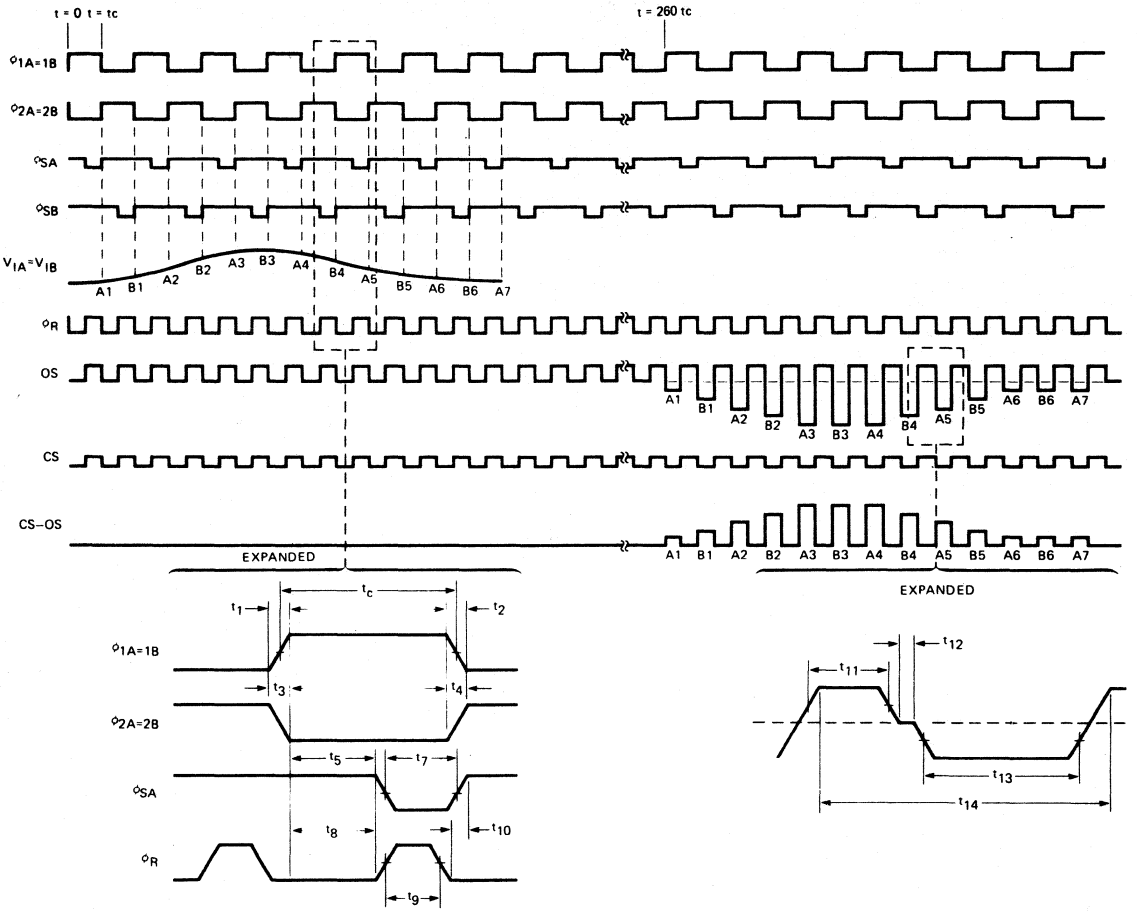


Fig. 6

TIMING DIAGRAM GENERATED BY THE TYPICAL DRIVE CIRCUITRY



For $f_{\phi R}$ = 10 MHz, $f_{\phi 1A} = f_{\phi 1B} = f_{\phi 2A} = f_{\phi 2B}$ = 5 MHz we have t_1 = 12 ns, t_2 = 10 ns, t_3 = 10 ns, t_4 = 12 ns, t_5 = 30 ns, t_6 = 0 ns, t_7 = 50 ns, t_9 = 44 ns, t_{10} = 5 ns, t_{11} = 40ns, t_{12} = 2 ns, t_{13} = 50 ns, t_{14} = 100 ns and t_c = 95 ns. All t_r and t_f are at 10 and 90% points.

Fig. 7

DEFINITION OF TERMS

Insertion Loss – Insertion loss is defined as: $20 \log \frac{\text{input signal}}{\text{output signal}}$

Non-Linearity – Non-linearity is defined as the maximum deviation (ΔV) of the output voltage expressed as a percentage of the maximum output signal voltage using a 5-step standard NTSC input signal.

Signal-to-Noise Ratio – $S/N = 20 \log \frac{V_{out}(max)}{\text{rms noise}}$. The rms noise is measured at $V_{out} = \frac{1}{2} V_{out}(max)$.

Average Signal Offset – The average signal offset is a DC offset of the output voltage (due to the average leakage current in the CCD register) which increases linearly with delay time and is temperature dependent. It has the effect of reducing the output signal range as the delay time is increased.

Output Signal Range – The output signal range is the difference between $V_{OUT}(max)$ (the maximum voltage at the output OS of the device) and the average signal offset.

CCD450/450A
9216-BIT DYNAMIC SHIFT REGISTER MEMORY

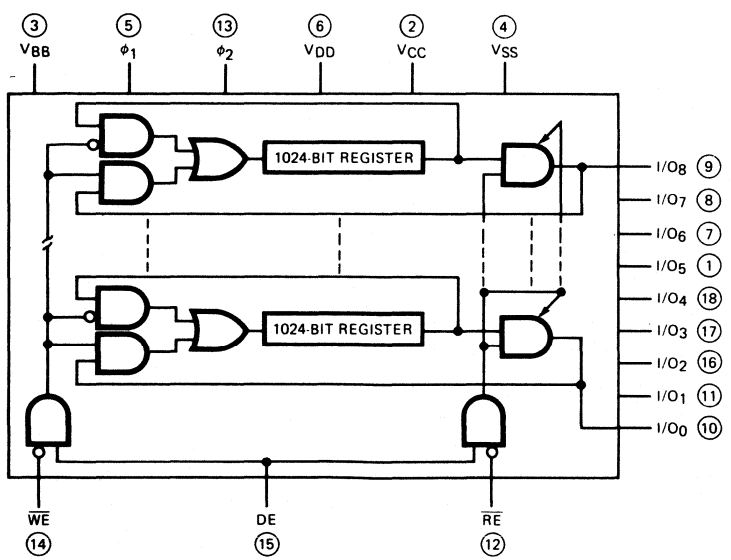
GENERAL DESCRIPTION – The CCD450/450A are 1-kilobyte serial storage devices organized 1024 words by nine bits. They contain nine 1024-bit low power CCD shift registers which are shifted in parallel providing for storage and retrieval of 9-bit words in a word-serial mode. The nine bi-directional TTL compatible data lines have 3-state output buffers. Operating frequency is 100 kHz to 2 MHz. Common to all nine registers are two clock lines, a Data Enable line, a $\overline{RE}$ line and a $\overline{WE}$ line. The devices operate in four modes: read, write, read/modify/write, and recirculate.

The CCD450/450A utilize a buried channel ion-implanted barrier structure for the CCD registers and an n-channel, silicon gate, Isoplanar structure for the on-chip MOS circuitry.

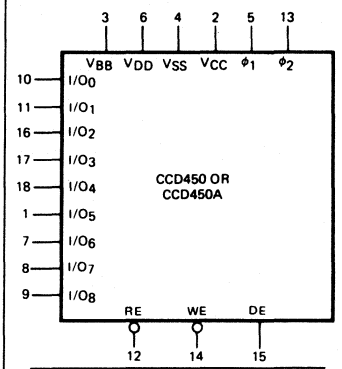
- **LOW POWER DISSIPATION: 250 mW IN THE READ MODE, 40 mW IN THE LOW SPEED STANDBY MODE**
- **CLOCK RATE: 2 MHz GUARANTEED (CCD450A)**
- **STANDARD 18-PIN DUAL IN-LINE PACKAGE**
- **3-STATE OUTPUTS**
- **NINE PARALLEL REGISTERS FOR BYTE-PLUS-PARITY OPERATION**
- **TTL COMPATIBLE**

PIN NAMES		LEVEL	CAPACITANCE	CURRENT
$I/O_0 - I/O_8$	Data Lines	TTL	8 pF	10 μA
ϕ_1	Clock	0 – 12 V	400 pF	2 mA
ϕ_2	Clock	0 – 12 V	400 pF	
$\overline{RE}$	Read Enable (Active LOW)	TTL	8 pF	10 μA
$\overline{WE}$	Write Enable (Active LOW)	TTL	8 pF	10 μA
DE	Data Enable	0 – 12 V	8 pF	6 mA
V_{SS}	Power Supply	Ground		
V_{CC}	Power Supply	+5.0 V		
V_{DD}	Power Supply	+12 V		
V_{BB}	Power Supply	−2.5 V		

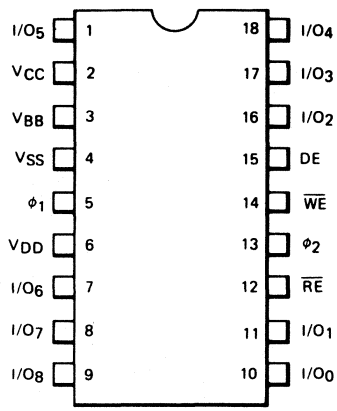
BLOCK DIAGRAM



LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE

DE	$\overline{RE}$	$\overline{WE}$	I/O LINES	MODE
L	X	X	Z_H	Recirculate (Low Power)
H	H	H	Z_H	Recirculate
H	H	L	I	Write
H	L	H	O	Read
H	L→H	X→L	0→Z_H→I	Read/ Modify/ Write

I = Input
O = Output
Z_H = High Impedance State

H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)

FUNCTIONAL DESCRIPTION – The CCD450/450A are serial storage memories consisting of 9216 bits which are organized in a format of 1024 words by 9 bits. This architecture is realized by the use of nine shift registers each containing 1024 bits. Since these registers are shifted in parallel, 9-bit words are stored or retrieved in a word-serial mode.

The basic timing is established by two clocks (ϕ_1 and ϕ_2) as shown in the timing diagram. During ϕ_2 HIGH time the logic is reset, data is shifted by one-half bit and the mode control level conversion from TTL to MOS levels is accomplished. During ϕ_1 HIGH time the data is shifted by one-half bit, the output charge state is sensed and presented to the output. The charge level written into the first CCD cell during ϕ_1 HIGH time is controlled by:

a. the output charge level during the Read or Recirculate mode, or
b. the data line during the Write mode.

The read and write operations are controlled by the state of Read Enable (pin 12), Write Enable (pin 14) and Data Enable (pin 15). The modes of operation are shown in the Truth Table.

MODES OF OPERATION (Refer to timing diagram)

Read Mode. In the read mode the Data Enable line (DE) is raised, and $\overline{RE}$ is lowered, as shown in the timing diagram, during ϕ_2 HIGH time. Both lines are held stable during ϕ_1 HIGH time. The data appears at the Input/Output ($I/O_0 - I/O_8$) pins t_{RA} after the leading edge of ϕ_1 HIGH time. Automatic recirculation of the data is provided in this mode.

Write Mode. In the write mode the Data Enable line (DE) is raised, and $\overline{WE}$ is lowered as shown in the timing diagram. Data must be valid at the I/O pins t_{SWD} prior to the trailing edge of ϕ_1. This data replaces any previous data in the current memory location.

Recirculate Mode 1. In the low power recirculate mode the Data Enable line (DE) is held LOW and all other inputs are ignored. Power is removed from on-chip and buffer circuits. Power consumption can be further reduced by lowering the clock frequency to the minimum allowable rate. **2.** Data can also be recirculated with I/O lines at high impedance by holding DE, $\overline{RE}$, and $\overline{WE}$ all HIGH. Power consumption will be higher than in the recirculate mode, example 1 but less than in the read mode.

Read/Modify/Write. In the read/modify/write mode the first part of ϕ_1 HIGH time provides the read function which is followed immediately by the write function during the second part of ϕ_1 HIGH time. The read data becomes available after t_{RA} and is present until $\overline{RE}$ goes HIGH. The new data inputs must be present on the I/O lines t_{SWD} prior to the trailing edge of ϕ_1.

Clear Memory. To clear memory upon start-up requires 4000 clock cycles minimum with DE and $\overline{RE}$ held HIGH and $\overline{WE}$ and I/Os held LOW.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to 55°C
Pins with Respect to V_{SS}	
I/O, $\overline{RE}$, $\overline{WE}$, V_{CC}	−0.5 V to +8.0 V
DE, ϕ_1, ϕ_2, V_{DD}	−0.5 V to +18 V
V_{BB}	+0.5 V to −5.0 V (current limited to less than 10 mA)

CAUTION: Static discharge to any gate pin may cause permanent damage. Store with shorting clip or on conductive foam. Use grounded soldering irons, tools and personnel when handling devices. Avoid synthetic fabric smocks and gloves. It is recommended that the device be inserted into socket before turning power on.

DC REQUIREMENTS: V_{DD} = 12 V +10%, −5%, V_{CC} = 5.0 V ±5%, V_{BB} = −2.5 V ±20%, T_A = 0°C to 55°C

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input LOW Voltage (I/O_0 thru I/O_8, $\overline{RE}$ and $\overline{WE}$)	−0.3		+0.8	V	
V_{IH}	Input HIGH Voltage (I/O_0 thru I/O_8, $\overline{RE}$ and $\overline{WE}$)	+2.2			V	
$V_{\phi L}$	Clock LOW Voltage (ϕ_1, ϕ_2)	−0.3		+0.4	V	
$V_{\phi H}$	Clock HIGH Voltage (ϕ_1, ϕ_2)	+11.0		Note 1	V	See Note 1, Fig. 2
V_{DEL}	Data Enable LOW Voltage	-0.3		+0.8	V	
V_{DEH}	Data Enable HIGH Voltage	10.8		13.2	V	

DC CHARACTERISTICS: V_{DD} = 12 V +10%, −5%, V_{CC} = 5.0 V ±5%, V_{BB} = −2.5 V ±20%, T_A = 0°C to 55°C

SYMBOL		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OL}		Output LOW Voltage (I/O_0 thru I/O_8)			+0.4	V	I_{OL} = 2.0 mA
V_{OH}		Output HIGH Voltage (I/O_0 thru I/O_8)	+2.4			V	I_{OH} = 0.2 mA
I_{IN}		Input Leakage Current $\overline{RE}$ & $\overline{WE}$			10	μA	$V_{IH} = V_{CC}$
		ϕ_2			10	μA	$V_{\phi 2H}$ = 12 V
		ϕ_1			2	mA	$V_{\phi 1H}$ = 12 V
		I/O Leakage Current (I/O_0 thru I/O_8)			±10	μA	$\overline{RE} = V_{IH}$
		Data Enable			6	mA	V_{DEH} = 13.2 V
I_{DD}	V_{DD} Current	Read Mode			18	mA	at f_{Max}
		Standby Mode			2	mA	at f_{Min}
I_{CC}	V_{CC} Current	Read Mode			5	mA	at f_{Max}
		Standby Mode			0.1	mA	at f_{Min}
I_{BB}	V_{BB} Current				10	μA	at f_{Max}

NOTE 1:
$V_{\phi H}$ max is dependent on value of V_{DD} as shown: operation is guaranteed within enclosed region shown in Fig. 2.

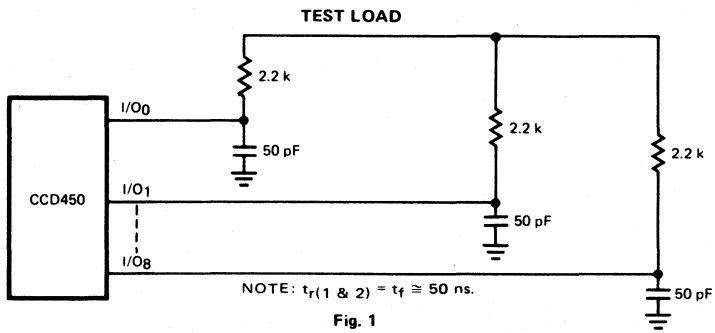


Fig. 1

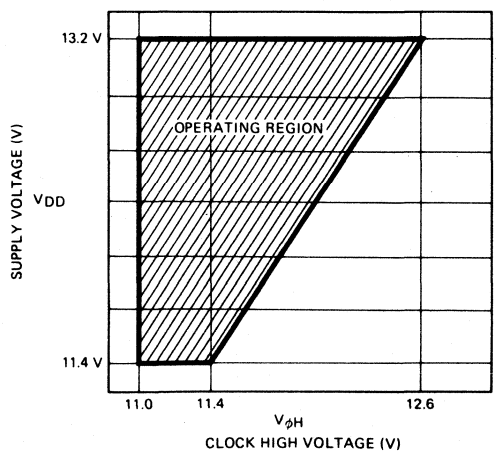


Fig. 2
V_{DD} SUPPLY VOLTAGE VERSUS CLOCK HIGH VOLTAGE

AC CHARACTERISTICS: V_{DD} = 12 V +10%, −5%, V_{CC} = 5.0 V ±5%, V_{BB} = −2.5 V ±20%, T_A = 0°C to 55°C

SYMBOL	PARAMETER	CCD450A		CCD450		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
t_{RA}	Read Access		140		180	ns	Note 1
t_{RP}	Read Persistence Time		0		0	ns	Note 2
C_ϕ	Clock Capacitance		400		400	pF	
C_R, C_W	$\overline{RE}$ and $\overline{WE}$ Capacitance		8		8	pF	
C_{DE}	Data Enable Capacitance		8		8	pF	

AC REQUIREMENTS: V_{DD} * 12 V +10%, −5%, V_{CC} = 5.0 V ±5%, V_{BB} = −2.5 V ±20%, T_A = 0°C to 55°C

SYMBOL	PARAMETER	CCD450A		CCD450		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX		
$t_{\phi 1RWC}$	ϕ_1 Clock HIGH Time in the Read, Write & Recirculate Modes	150	500	200	500	ns	
$t_{\phi 1RMW}$	ϕ_1 Clock HIGH Time in the Read/Modify/Write Mode	300	500	350	500	ns	
$t_{\phi 2}$	ϕ_2 Clock HIGH	70	500	100	500	ns	
t_{UL1}	Underlap 1	20	200	20	200	ns	
t_{UL2}	Underlap 2	20	9560	20	9480	ns	Note 3
t_{SW}	Write Set-Up	100		100		ns	
t_{HW}	Write Hold	0		0		ns	
t_{SWDE}	Write Mode Data Enable Set-Up	100		100		ns	
t_{HWDE}	Write Mode Data Enable Hold	0		0		ns	
t_{SWD}	Write Data Set-Up	50		50		ns	
t_{HWD}	Write Data Hold	0		0		ns	
t_{SRDE}	Recirculate Mode Data Enable Set-Up	0		0		ns	
t_{HRDE}	Recirculate Mode Data Enable Hold	0		0		ns	
t_{r1}	ϕ_1 Rise Time	50	200	50	200	ns	
t_{r2}	ϕ_2 Rise Time	50		50		ns	
t_f	ϕ_1 & ϕ_2 Fall Time	50		50		ns	
t_{RMW}	Read Enable High Time in Read/Modify/Write Mode	50		50		ns	
f	Clock Rate	0.1	2.0	0.1	1.0	MHz	

NOTES:
1. Propagation delay depends on the occurrence of the last one of the three events: $\overline{RE}$ going LOW, ϕ_1 going HIGH, or DE going HIGH.
2. Read persistence time (valid data period) terminates with first one of three events to occur: ϕ_2 going HIGH, DE going LOW, or $\overline{RE}$ going HIGH.
3. $t_{UL2(MAX)} = 10\ \mu s - (t_{\phi 1} + t_{\phi 2} + t_{UL1} + 2t_r + 2t_f)$

READ/MODIFY/WRITE
(Reference levels for timing 10% and 90%)

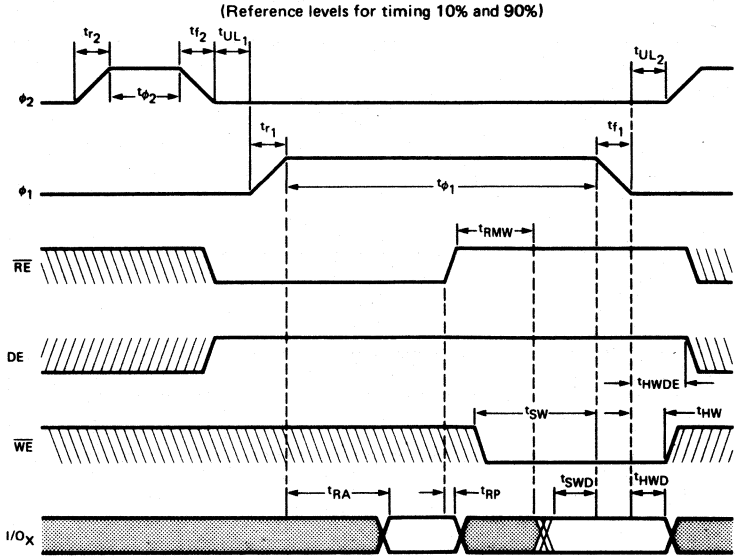


Fig. 3

READ, WRITE OR RECIRCULATE MODE TIMING
(Reference levels for timing 10% and 90%)

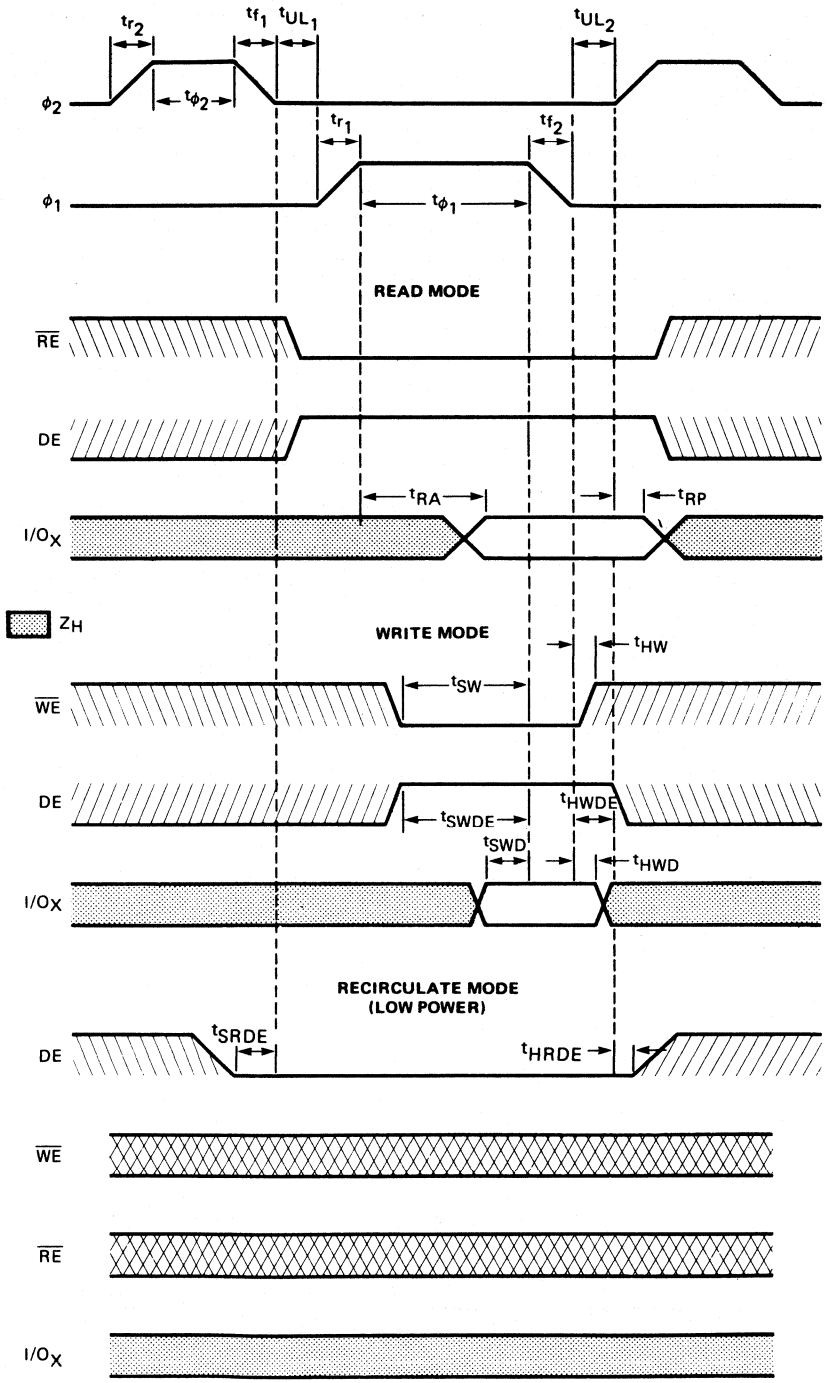


Fig. 4

CCD460
16,384-BIT DYNAMIC LINE ADDRESABLE RAM, LARAM

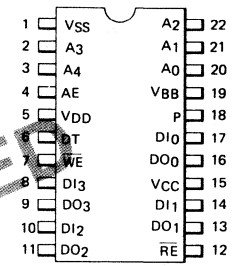
GENERAL DESCRIPTION – The Fairchild CCD460 is a fast 16,384 bit dynamic CCD memory designed for fast access cache, swapping store, mainframe, and other memory applications where its LARAM performance features are required. The Line Addressable Random Access Memory organization provides a data rate of 20 megabits per second with an average random access time of 12.8 μs at an operating frequency of 5 MHz, and with typically less than 200 mW of power. It also provides very low clock drive capacitance loading. The 5-bit address selects one of 32 128-bit registers in each section and those registers deliver or receive data through their input and output pins. Data is not inverted and is available 4 bits parallel. Recirculation is automatic in accessed registers.

Operation is straightforward and support circuitry kept simple by the TTL compatibility of data in and out lines and address lines, 3-state outputs, and very low drive capacitance loading on the 0-12 V inputs to Address Enable, Data Transfer, and Precharge pins. Readout is non-destructive and data out lines can be wired-OR for flexibility and ease of expansion. The device operates in four modes: read, write, read/modify/write, and low power standby recirculate.

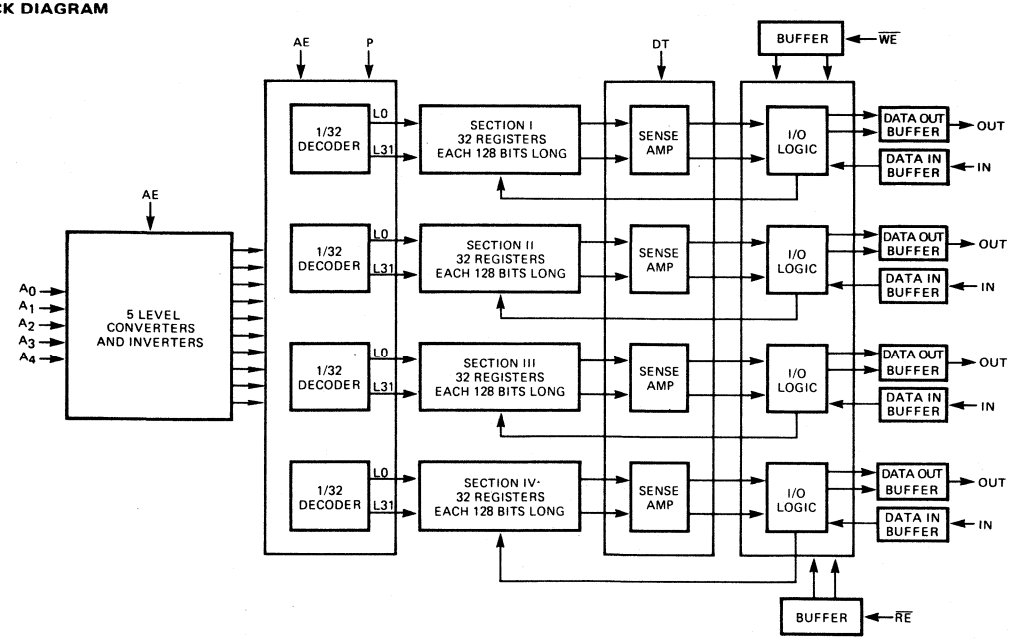
The CCD460 features Isoplanar, NMOS, buried channel, and silicon gate structure for high density and reliable performance.

- **HIGH DATA RATE – 20 MEGABITS PER SECOND**
- **FAST READ ACCESS TIME – < 100 ns**
- **FAST AVERAGE RANDOM ACCESS TIME – 12.8 μs**
- **LOW POWER – 200 mW MAX @ 5 MHz, 50 mW STANDBY RECIRCULATE @ 400 kHz**
- **LOW CLOCK CAPACITANCES – 120 pF AND 15 pF**
- **TWO PHASE OPERATION – 0 TO +12 V CLOCKS**
- **TTL COMPATIBLE**
- **3-STATE OUTPUTS**
- **FOUR MODE OPERATION; READ, WRITE, READ/MODIFY/WRITE, RECIRCULATE**
- **FOUR INPUTS AND FOUR OUTPUTS**
- **STANDARD 22-PIN DIP**
- **ISOPLANAR, NMOS, BURIED CHANNEL, SILICON GATE STRUCTURE**

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



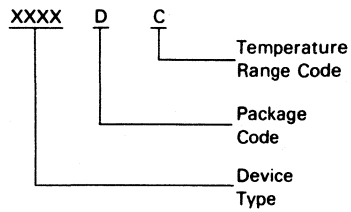
5

ORDER AND PACKAGE INFORMATION

Fairchild integrated circuits may be ordered using a simplified purchasing code where the package style and temperature range are defined as follows:

PACKAGE STYLE

D = Dual In-line – Ceramic (hermetic)
P = Dual In-line – Plastic
F = Flatpak



In order to accommodate varying die sizes and numbers of pins (14, 16, 24, etc.), a number of different package forms are required. The Package Information list on the following pages indicates the specific package codes currently used for each device type. The detailed package outline corresponding to each package code is shown at the end of this section.

Temperature Range

Three basic temperature grades are in common use: C = Commercial-Industrial (MOS), 0°C to +70°C; C = Commercial-Industrial (CMOS), −40°C to +85°C; L = Limited Military (MOS), −55°C to +85°C; M = Military, −55°C to +125°C. Exact values and conditions are indicated on the data sheets. For CCD temperature range, check the individual data sheets.

Examples

(a) 4014FM
This number code indicates a 4014 Register in a Flatpak with military temperature rating.

(b) 4720DC
This number code indicates a 4720 256 x 1 RAM in a ceramic Dual In-line Package with commercial temperature rating.

(d) 2102DM
This number code indicates a 2102 RAM in a ceramic package with a military temperature rating.

Device Identification/Marking

All Fairchild standard catalog integrated circuits will be marked as follows:

Device Type XX
Date Code

MOS PACKAGE INFORMATION

DEVICE	PACKAGE CODE			TEMPERATURE RANGE		
	D	P	F	C	L	M
1103	7D			X		
1103F	7D			X		
1103S	7D			X		
11031	7D			X		
21L02	6D			X		
21L02A	6D			X		
21L02B	6D			X		
2102	6D			X	X	X
2102F	6D			X	X	X
21021	6D			X	X	X
21022	6D			X	X	X
2533	6C			X	X	X
3257	6K			X		
3258	7J			X		
3260	7M			X		
3262A	7J			X		
3262B	7J			X		
3341	6D	9R		X	X	X
3341A	6D	9R		X		
3342	7J	9B		X		
3347	7J	9B		X		
3348	7M			X		
3349	7J	9B		X		
33511	7Y			X	X	X
33512	7Y			X	X	X
3355	6C	9L		X		
33571	7J			X		
33752	7J			X		
3515	7M			X		
35L38	7I			X		
35L38A	7I			X		
35L38B	7I			X		
3538	7I			X	X	X
3538F	7I			X	X	X
35381	7I			X	X	X
3539*	7I			X		
3705	7J		4A	X	X	X
3708	7J		4A	X	X	X
3814	7M			X		
3815	7M			X		
3816	7J	9B		X		
3817A		8P		X		
3817D		8P		X		
3843*	7Y			X		
3850	6I			X	X	X
3851	6I			X	X	X
3852	6I			X	X	X
3853	6I			X	X	X
3854	6I			X	X	X
40962	6D		4D	X	X	
40963	6D		4D	X	X	
40964	6D		4D	X	X	
40965	6D		4D	X	X	

*To Be Announced

CMOS PACKAGE INFORMATION

DEVICE	MILITARY (M) -55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL -40°C to +85°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
4001	6A	3I	6A	9A	3I
4002	6A	3I	6A	9A	3I
4006	6A	3I	6A	9A	3I
4007	6A	3I	6A	9A	3I
4008	6B	4L	6B	9B	4L
4011	6A	3I	6A	9A	3I
4012	6A	3I	6A	9A	3I
4013	6A	3I	6A	9A	3I
4014	6B	4L	6B	9B	4L
4015	6B	4L	6B	9B	4L
4016	6A	3I	6A	9A	3I
4017	6B	4L	6B	9B	4L
4018	6B	4L	6B	9B	4L
4019	6B	4L	6B	9B	4L
4020	6B	4L	6B	9B	4L
4021	6B	4L	6B	9B	4L
4022	6B	4L	6B	9B	4L
4023	6A	3I	6A	9A	3I
4024	6A	3I	6A	9A	3I
4025	6A	3I	6A	9A	3I
4027	6B	4L	6B	9B	4L
4028	6B	4L	6B	9B	4L
4029	6B	4L	6B	9B	4L
4030	6A	3I	6A	9A	3I
4031	6B	4L	6B	9B	4L
4035	6B	4L	6B	9B	4L
4040	6B	4L	6B	9B	4L
4041	6A	3I	6A	9A	3I
4042	6B	4L	6B	9B	4L
4043	6B	4L	6B	9B	4L
4044	6B	4L	6B	9B	4L
4046	6B	4L	6B	9B	4L
4047	6A	3I	6A	9A	3I
4049	6B	4L	6B	9B	4L
4050	6B	4L	6B	9B	4L
4051	6B	4L	6B	9B	4L
4052	6B	4L	6B	9B	4L
4053	6B	4L	6B	9B	4L
4066	6A	3I	6A	9A	3I
4067	6N,6Q	4M	6N,6Q	9N,9U	4M
4068	6A	3I	6A	9A	3I
4069	6A	3I	6A	9A	3I
4070	6A	3I	6A	9A	3I
4071	6A	3I	6A	9A	3I
4072	6A	3I	6A	9A	3I
4073	6A	3I	6A	9A	3I
4075	6A	3I	6A	9A	3I
4076	6B	4L	6B	9B	4L
4077	6A	3I	6A	9A	3I
4078	6A	3I	6A	9A	3I
4081	6A	3I	6A	9A	3I
4082	6A	3I	6A	9A	3I
4085	6A	3I	6A	9A	3I
4086	6A	3I	6A	9A	3I

CMOS PACKAGE INFORMATION (Cont'd)

DEVICE	MILITARY (M) -55°C to +125°C		COMMERCIAL (C)/INDUSTRIAL -40°C to +85°C		
	CERAMIC DIP (D)	FLATPAK (F)	CERAMIC DIP (D)	PLASTIC DIP (P)	FLATPAK (F)
4104	6B	4L	6B	9B	4L
4510	6B	4L	6B	9B	4L
4511	6B	4L	6B	9B	4L
4512	6B	4L	6B	9B	4L
4514	6N,6Q	4M	6N,6Q	9N,9U	4M
4515	6N,6Q	4M	6N,6Q	9N,9U	4M
4516	6B	4L	6B	9B	4L
4518	6B	4L	6B	9B	4L
4519	6B	4L	6B	9B	4L
4520	6B	4L	6B	9B	4L
4522	6B	4L	6B	9B	4L
4526	6B	4L	6B	9B	4L
4528	6B	4L	6B	9B	4L
4531	6B	4L	6B	9B	4L
4532	6B	4L	6B	9B	4L
4539	6B	4L	6B	9B	4L
4555	6B	4L	6B	9B	4L
4556	6B	4L	6B	9B	4L
4582	6B	4L	6B	9B	4L
4702	6B	4L	6B	9B	4L
4703	6Q	4M	6Q	9U	4M
4704	6Q	4M	6Q	9U	4M
4705	6Q	4M	6Q	9U	4M
4706	6Q	4M	6Q	9U	4M
4707	6Q	4M	6Q	9U	4M
4710	7D		7D	9M	
4720	6B	4L	6B	9B	4L
4723	6B	4L	6B	9B	4L
4724	6B	4L	6B	9B	4L
4725	6B	4L	6B	9B	4L
4731	6A	3I	6A	9A	3I
4734	7D		7D	9M	
40085	6B	4L	6B	9B	4L
40097	6B	4L	6B	9B	4L
40098	6B	4L	6B	9B	4L
40160	6B	4L	6B	9B	4L
40161	6B	4L	6B	9B	4L
40162	6B	4L	6B	9B	4L
40163	6B	4L	6B	9B	4L
40174	6B	4L	6B	9B	4L
40175	6B	4L	6B	9B	4L
40192	6B	4L	6B	9B	4L
40193	6B	4L	6B	9B	4L
40194	6B	4L	6B	9B	4L
40195	6B	4L	6B	9B	4L
40283	6B	4L	6B	9B	4L

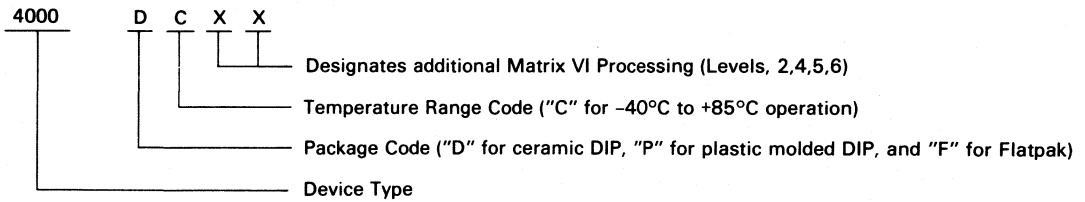
CCD PACKAGE INFORMATION

DEVICE	PACKAGE CODE – D	TEMPERATURE RANGE
CCD101	7E1	C
CCD110	7E2	C
CC110F	7E7	C
CCD121	7E4	C
CCD201	7E3	C
CCD311	7E6	C
CC450A	7E5	C
CC450B	7E5	C
CCD460	7E8	C

MATRIX VI PROGRAM ORDERING INFORMATION

Matrix VI is a full spectrum/cost effective reliability and quality program for commercial/industrial ICs only. It features six levels of screening/package flows, each tailored to a user's field application/environment and his incoming quality/equipment reliability requirements.

A Matrix VI part number consists of the device type followed by the package code letter, the temperature range code letter, and the Matrix VI code letter (as applicable, see flow chart).



EXAMPLES

(a) 4001PC — Device type 4001, packaged in plastic Dual In-line (P), in commercial temperature range (C) and processed to Matrix VI Level 1.

(b) 4001PCQM — Device type 4001, packaged in plastic Dual In-line (P), in commercial temperature range (C) with supplemental Matrix VI Level 2 testing including 100% thermal shock, "hot rail" test and 0.15% AQL functional testing.

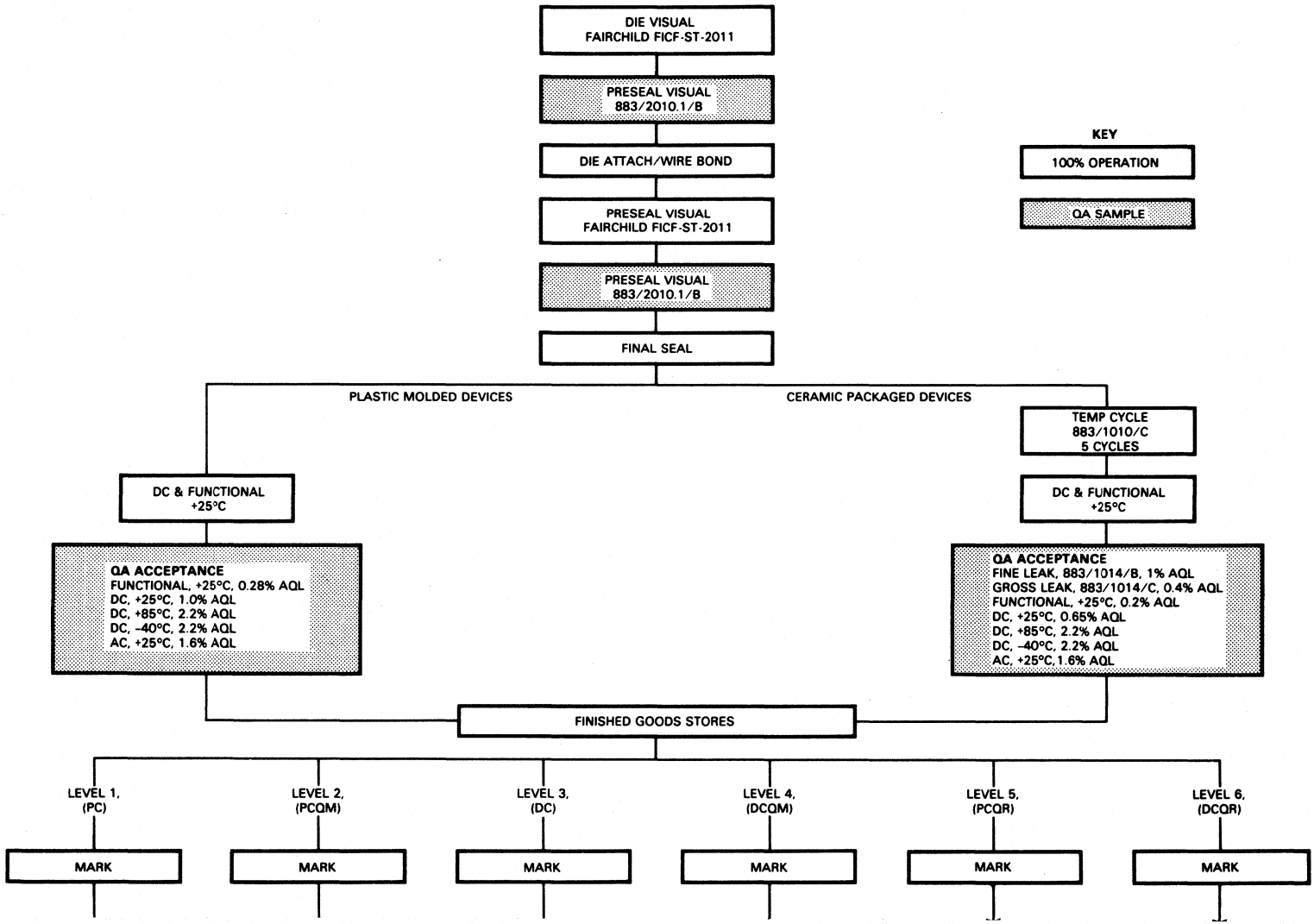
(c) 4001DC — Device type 4001, packaged in ceramic Dual In-line (D), in commercial temperature range and processed to Matrix VI Level 3.

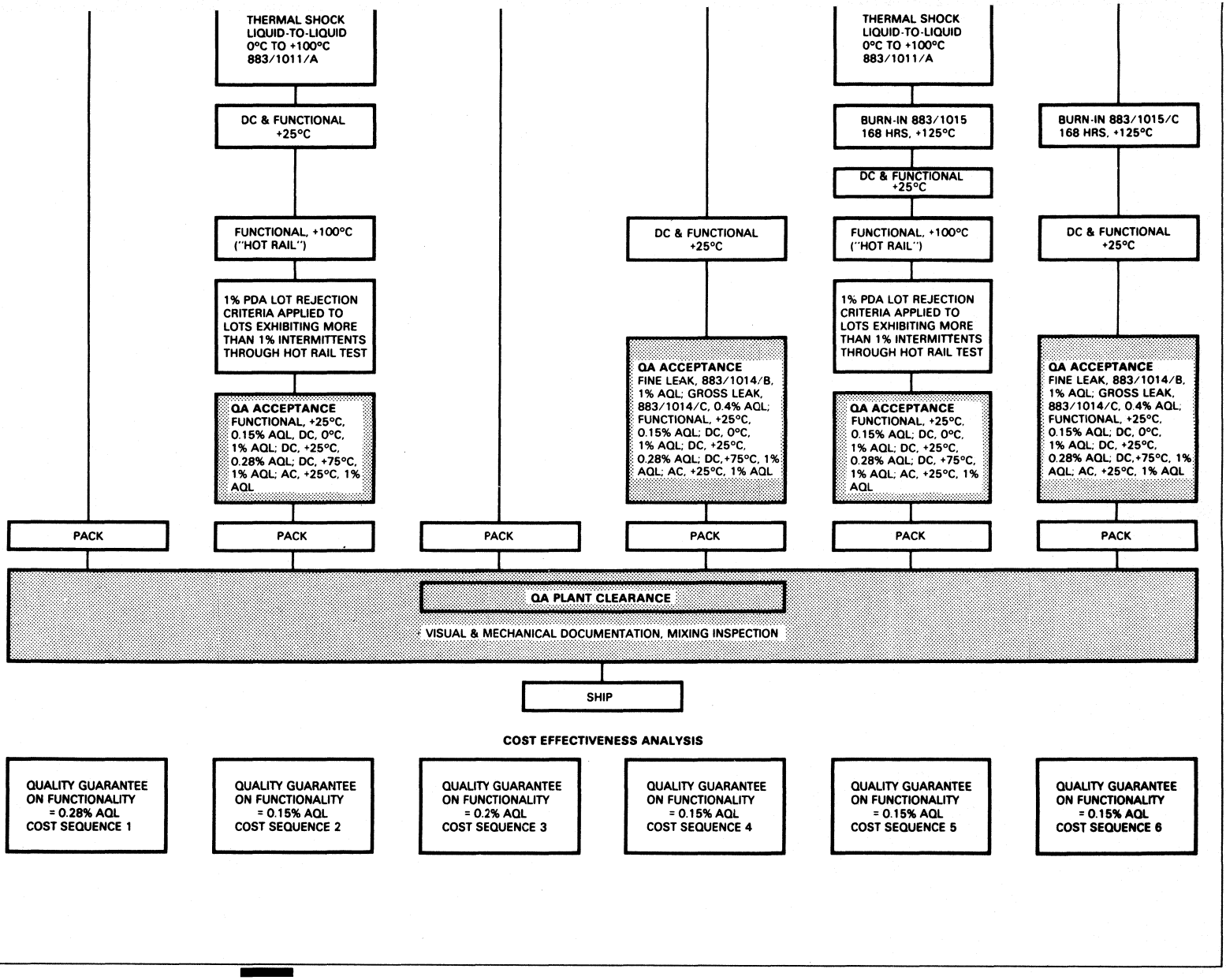
(d) 4001 DCQM — Device type 4001, packaged in ceramic Dual In-line, in commercial temperature range (C) with supplemental Matrix VI Level 4 screening including second 100% DC/functional testing and 0.15% AQL functional testing.

(e) 4001PCQR — Device type 4001, packaged in Dual In-line, in commercial temperature range (C) with supplemental Matrix VI Level 5 screening including 100% thermal shock, "hot rail" test, 168 hours 125°C burn-in and 0.15% AQL functional testing.

(f) 4001DCQR — Device type 4001, packaged in ceramic Dual In-line, in commercial temperature range with supplemental Matrix VI Level 6 screening including burn-in, three 100% DC/functional tests and 0.15% AQL functional testing.

6 MATRIX VI PROCESS FLOW OPTIONS & COST EFFECTIVENESS




THERMAL SHOCK
LIQUID-TO-LIQUID
0°C TO +100°C
883/1011/A
DC & FUNCTIONAL
+25°C
FUNCTIONAL, +100°C
("HOT RAIL")
1% PDA LOT REJECTION
CRITERIA APPLIED TO
LOTS EXHIBITING MORE
THAN 1% INTERMITTENTS
THROUGH HOT RAIL TEST
QA ACCEPTANCE
FUNCTIONAL, +25°C,
0.15% AQL, DC, 0°C,
1% AQL; DC, +25°C,
0.28% AQL; DC, +75°C,
1% AQL; AC, +25°C, 1%
AQL
DC & FUNCTIONAL
+25°C
QA ACCEPTANCE
FINE LEAK, 883/1014/B,
1% AQL; GROSS LEAK,
883/1014/C, 0.4% AQL;
FUNCTIONAL, +25°C,
0.15% AQL; DC, 0°C,
1% AQL; DC, +25°C,
0.28% AQL; DC,+75°C, 1%
AQL; AC, +25°C, 1% AQL
THERMAL SHOCK
LIQUID-TO-LIQUID
0°C TO +100°C
883/1011/A
BURN-IN 883/1015
168 HRS, +125°C
DC & FUNCTIONAL
+25°C
FUNCTIONAL, +100°C
("HOT RAIL")
1% PDA LOT REJECTION
CRITERIA APPLIED TO
LOTS EXHIBITING MORE
THAN 1% INTERMITTENTS
THROUGH HOT RAIL TEST
QA ACCEPTANCE
FUNCTIONAL, +25°C,
0.15% AQL; DC, 0°C,
1% AQL; DC, +25°C,
0.28% AQL; DC, +75°C,
1% AQL; AC, +25°C, 1%
AQL
BURN-IN 883/1015/C
168 HRS, +125°C
DC & FUNCTIONAL
+25°C
QA ACCEPTANCE
FINE LEAK, 883/1014/B,
1% AQL; GROSS LEAK,
883/1014/C, 0.4% AQL;
FUNCTIONAL, +25°C,
0.15% AQL; DC, 0°C,
1% AQL; DC, +25°C,
0.28% AQL; DC,+75°C, 1%
AQL; AC, +25°C, 1% AQL
PACK
PACK
PACK
PACK
PACK
PACK
QA PLANT CLEARANCE
VISUAL & MECHANICAL DOCUMENTATION, MIXING INSPECTION
SHIP
COST EFFECTIVENESS ANALYSIS
QUALITY GUARANTEE
ON FUNCTIONALITY
= 0.28% AQL
COST SEQUENCE 1
QUALITY GUARANTEE
ON FUNCTIONALITY
= 0.15% AQL
COST SEQUENCE 2
QUALITY GUARANTEE
ON FUNCTIONALITY
= 0.2% AQL
COST SEQUENCE 3
QUALITY GUARANTEE
ON FUNCTIONALITY
= 0.15% AQL
COST SEQUENCE 4
QUALITY GUARANTEE
ON FUNCTIONALITY
= 0.15% AQL
COST SEQUENCE 5
QUALITY GUARANTEE
ON FUNCTIONALITY
= 0.15% AQL
COST SEQUENCE 6

UNIQUE 38510 PROGRAM ORDERING INFORMATION

The Fairchild Unique 38510 Program is written in accordance with MIL-M-38510 and MIL-STD-883

To meet the need of improved reliability in the military market, CMOS Integrated Circuits are available with special processing. Devices ordered to this program are subjected to the 100% screening as outlined in the Process. Devices will be marked in accordance with MIL-M-38510 unless otherwise specified under number Option 6.

UNIQUE 38510 devices are not normally stocked by distributors.

Customer procurement documents should specify the following:

(a) Fairchild Product Code indicating the basic device type and package combination.
(b) The Unique 38510 Device Class. (A, B, C, S, P)
(c) Number and/or Letter Options required.
(d) Special Marking requirements.

The order code number consists of (a) and (b) as shown above. The order code detailed format is shown below.

DEVICE TYPE	PACKAGE TYPE	TEMPERATURE RANGE	DESIGNATES UNIQUE 38510 PROCESSING IF REQUIRED. SEE DESCRIPTION OF SCREENING REQUIREMENTS
	D = CERAMIC DIP	C = −40°C TO +85°C(59X)	
	P = PLASTIC DIP	M = −55°C TO +125°C(51X)	
	F = CERAMIC FLAT		

Order code examples are:

4029FMQB	4001DMQC
Class QB Unique 38510	Class QC Unique 38510

Number Options: These options apply to operations performed on each unit delivered:

OPTION 1	Lead form to dimensions in detail specifications, followed by hermetic seal tests.
OPTION 2	Hot solder dip finish.
OPTION 3	Read and record critical parameters before and after burn-in.
OPTION 4	Initial qualification, Group B & C quality conformance not required.
OPTION 5	Radiographic inspection shall be performed on all devices.
OPTION 6	Special marking required.
OPTION 7	Non-conforming variation – refer to procurement documents for details (must be negotiated with factory).

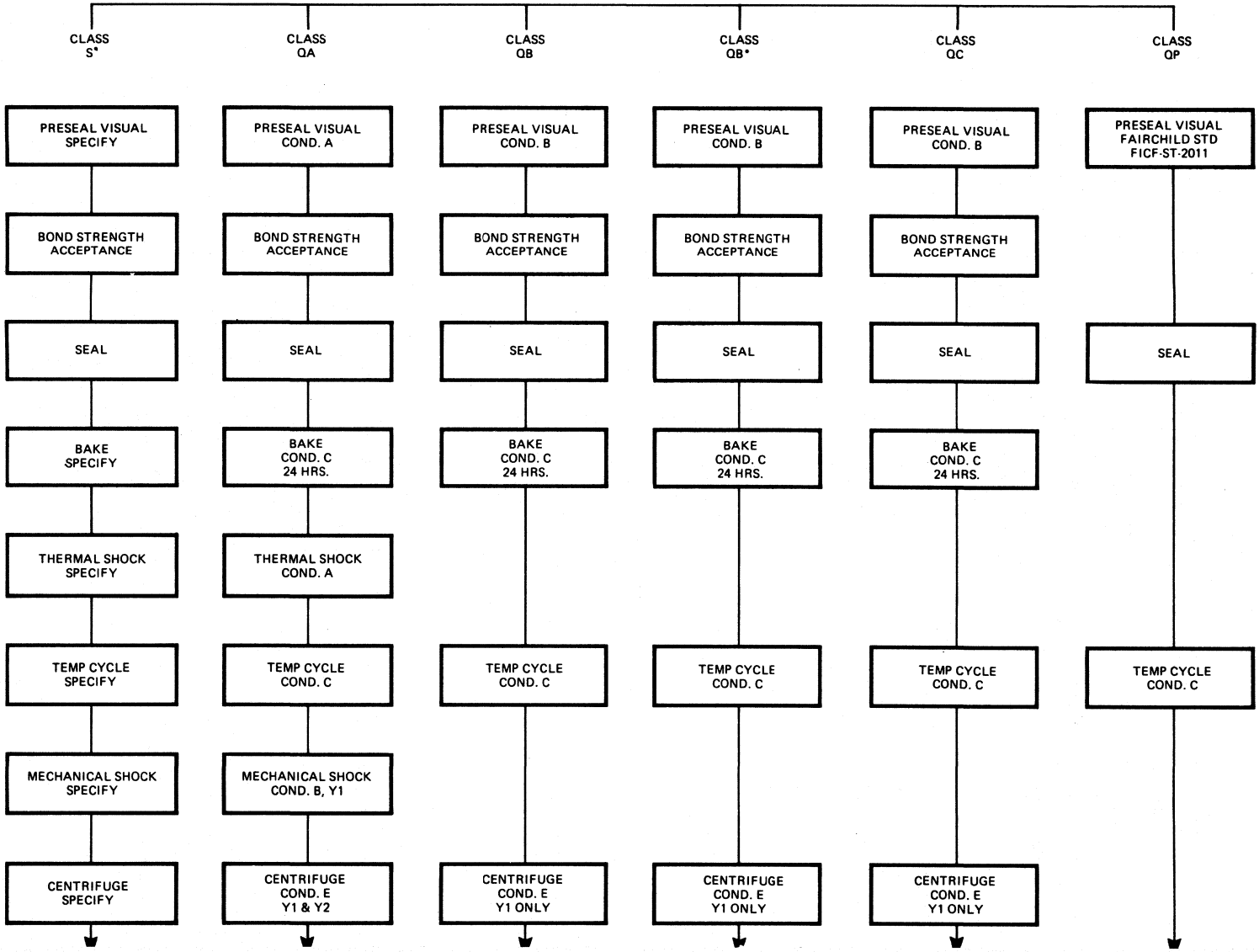
Letter Options: These options apply once per Purchase Order or line item and are considered Test Charges:

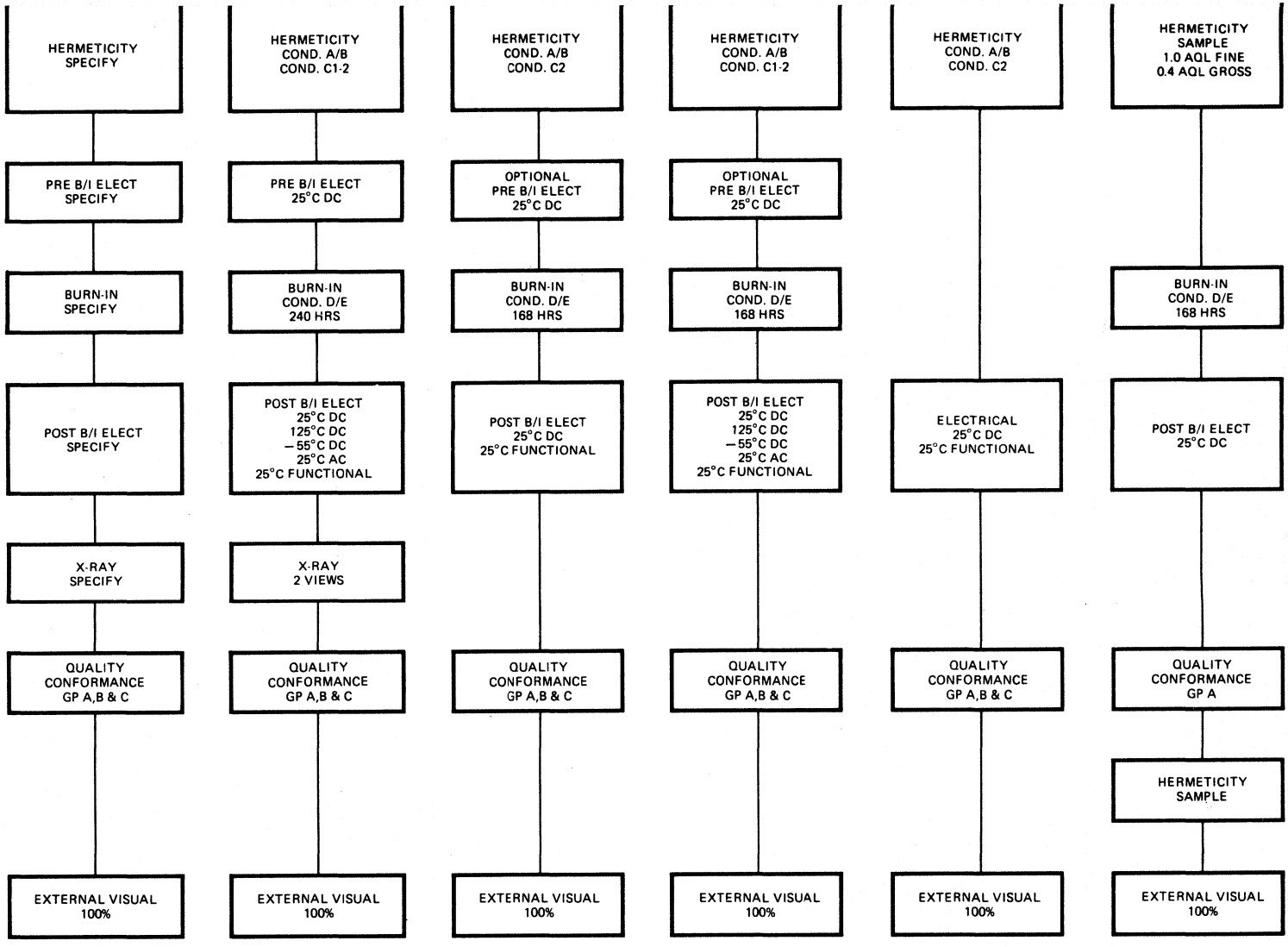
OPTION A	Group B testing shall be performed on customer's parts.
OPTION B	Group C testing shall be performed on customer's parts.
OPTION C	Generic data to be supplied from the latest completed lot.
OPTION D	Unique 38510 program plan, pertinent to the device family being purchased, shall be supplied.

PROCESS SCREENING REQUIREMENTS

MIL-STD-883 TEST METHODS	DESCRIPTION
Preseal Visual MTD. 2010.1:	Cond. A Maximum Visual Criteria Cond. B Optimum Visual Criteria FICF-ST-02011 Fairchild Standard
Bond Strength:	Bond strength is monitored on a sample basis three times per shift per mach.
Seal:	Devices are hermetically sealed for compliance to MIL-STD-883 requirements
High Temperature Storage:	Cond. B Tstg = 125°C Specify Time Cond. C Tstg = 150°C Cond. D Tstg = 200°C
Thermal Shock MTD 1011:	Cond. A 0°/100°C 15 cycles Cond. B −55°/125°C
Temperature Cycle MTD 1011:	Cond. B −55°/125°C Cond. C −65°/150°C 10 cycles Cond. D −65°/200°C
Mechanical Shock MTD 2002:	Cond. A 500 Gs 5 Shocks in X_1, X_2 Cond. B 1500 Gs Y_1, Y_2, Z_1 & Z_2
Constant Acceleration MTD 2001:	Cond. D 20000 Gs 2 minute in each Cond. E 30000 Gs X_1 X_2 Y_1 Y_2 Cond. F 50000 Gs Z_1 Z_2
Hermetic Seal MTD 1014:	Cond. A Fine-Helium $5x10^{-8}$ cc/sec Cond. B Fine-Radiflo $5x10^{-8}$ cc/sec Cond. C1 Gross-FC43/Hot 10^{-3} cc/sec Cond. C2 Gross-FC78/Vacuum 10^{-5} cc/sec
Pre Burn-in Electrical (5004.1):	25°C DC electrical testing to remove rejects prior to submission to burn-in screen
Burn-in Screen MTD 1015:	Cond. A, Cond. B, Cond. C Cond. D and Cond. E
Post Burn-in Electrical (5004.1):	Post Burn-in electrical screening to cull out devices which failed as a result of burn-in. Test Parameters may include: 25°C DC, 125°C DC, −55°C DC, 25°C AC and 25°C Functional tests.
Radiography MTD 2012:	6X, 8X magnification and criteria specify number of views
Quality Conformance Inspection MTD 5005:1:	Group A: Electrical Characteristics Group B: Package oriented Tests Group C: Environmental and Life Tests
External Visual MTD 2009:	3X, 20X magnification: Verify dimensions, configuration, lead structure, marking and workmanship

UNIQUE 38510



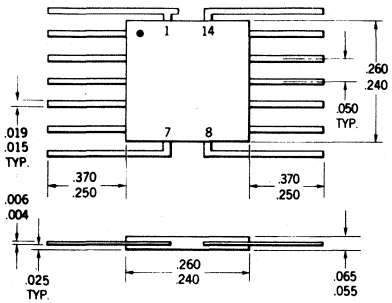


*Upon customer request only. Class B processing in this case includes adding post burn-in testing; dc testing at +125°C and −55°C and ac testing. at 25°C.

PACKAGE OUTLINES

3I

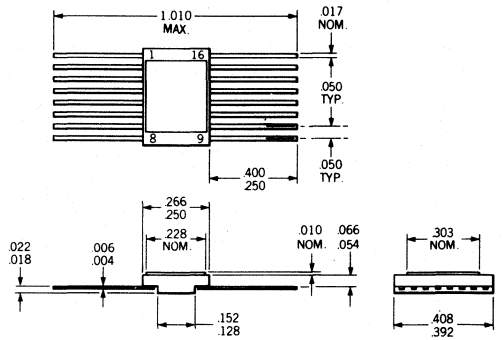
In Accordance with JEDEC TO-86 Outline 14-Pin Cerpak



NOTES:
All dimensions in inches
Pins are alloy 42
Package weight is 0.26 gram
Pin 1 orientation may be either tab or dot

4A

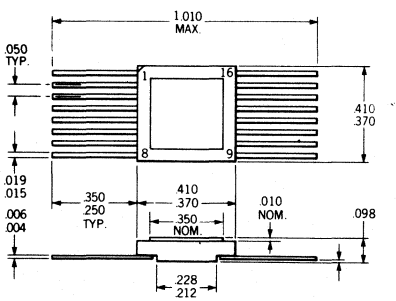
16-Pin Flatpak



NOTES:
All dimensions in inches
Pins are NiAu plated kovar
Cap is kovar
Base is Al_2O_3
Cavity size is .110 x .180
Package weight is 0.6 gram approx.

4D

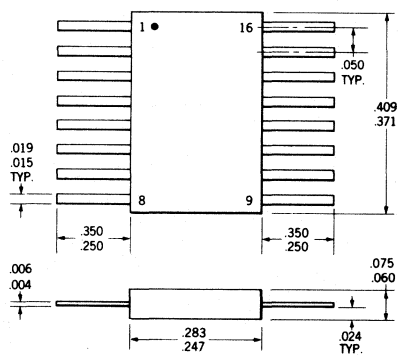
16-Pin 3/8 Pk Flatpak



NOTES:
All dimensions in inches
Pins are NiAu plated kovar
Cap is kovar
Base is Al_2O_3
Cavity size is .180 x .180
Package weight is 0.6 gram approx.

4L

16-Pin Cerpak

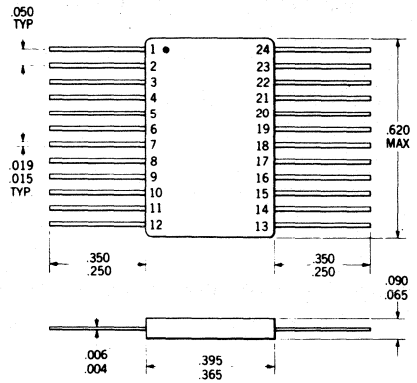


NOTES:
All dimensions in inches
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

PACKAGE OUTLINES

4M

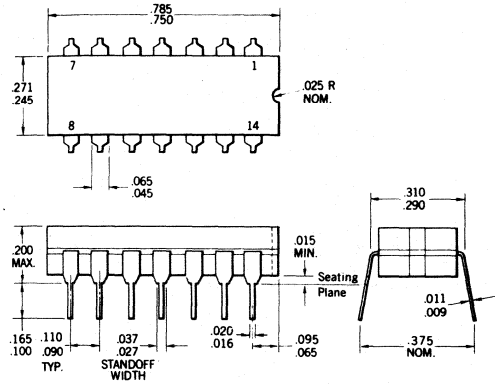
24-Pin BeO Cerpak



NOTES:
All dimensions in inches
Pins are alloy 42
Package weight is 0.8 gram
Hermetically sealed beryllia package

6A

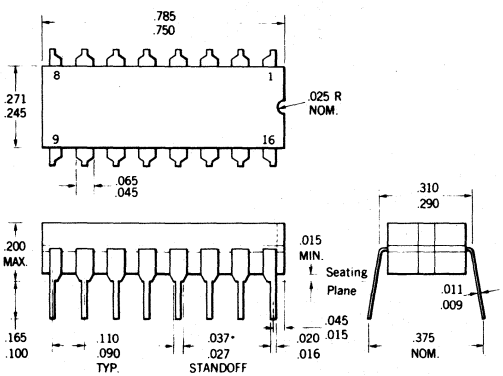
14-Pin Ceramic Dual In-line



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar
Package weight is 2.0 grams

6B

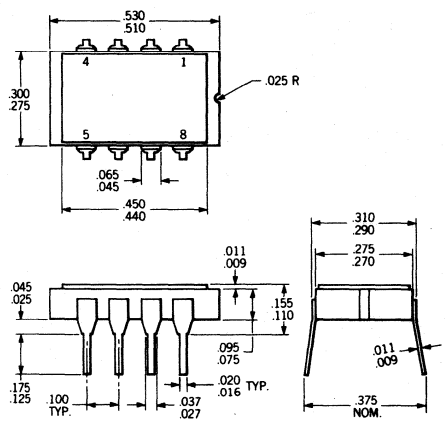
16-Pin Ceramic Dual In-line



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimensions does not apply to the corner pins

6C

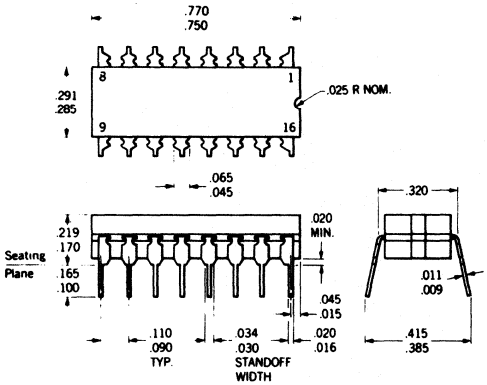
8-Pin Side Brazed Dual In-line



PACKAGE OUTLINES

6D

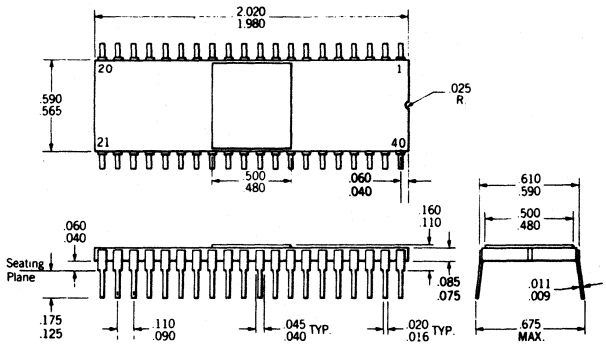
16-Pin Ceramic Dual In-line



NOTES:
- All dimensions in inches
- Pins are tin-plated kovar
- Pins are intended for insertion in hole rows on .300" centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Board-drilling dimensions should equal your practice for .020 inch diameter pin
- Hermetically sealed alumina package
- Cavity size is .130 x .230
- *The .034/.030 dimension does not apply to the corner pins
- Package weight is 2.2 grams

6I

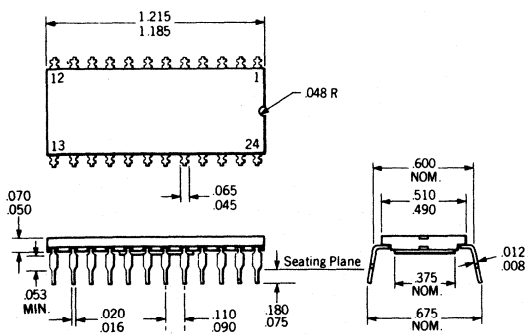
40-Pin Dual In-line Side Brazed, Large Cavity



NOTES:
- All dimensions in inches
- Pin material nickel gold-plated kovar
- Cap is kovar
- Base is ceramic
- Cavity size is .310 x .310
- Package weight is 6.5 grams

6K

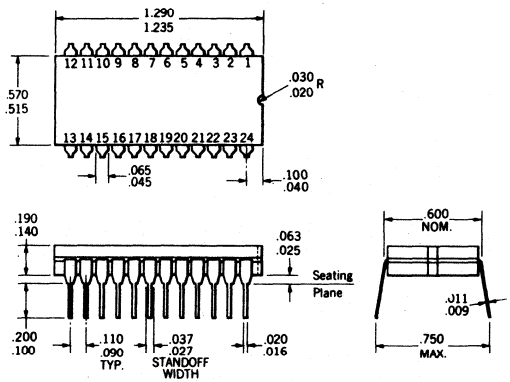
24-Pin Top Brazed Dual In-line



NOTES:
- All dimensions in inches
- Cap material is kovar
- Base material is Al_2O_3
- Cavity size is .210 x .210
- Pins may be formed as a top or bottom brazed package
- Package weight is 3.0 grams

6N

24-Pin Ceramic MSI Dual In-line

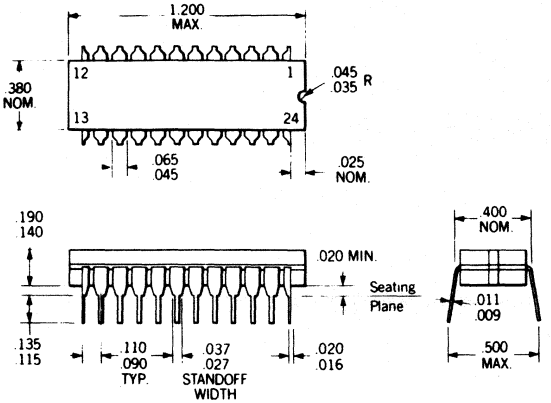


NOTES:
- All dimensions in inches
- Pins are intended for insertion in hole rows on .700" centers
- They are purposely shipped with "positive" misalignment to facilitate insertion
- Pins are tin-plated kovar
- Package weight is 6.5 grams
- Package material is alumina

PACKAGE OUTLINES

6Q

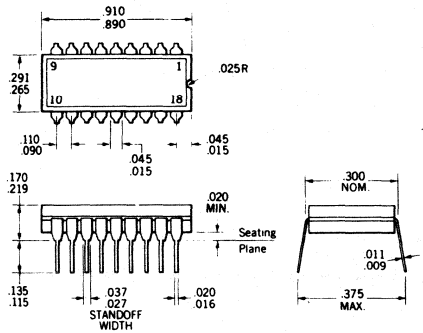
24-Pin Ceramic Dual In-line



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .500" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar

7D

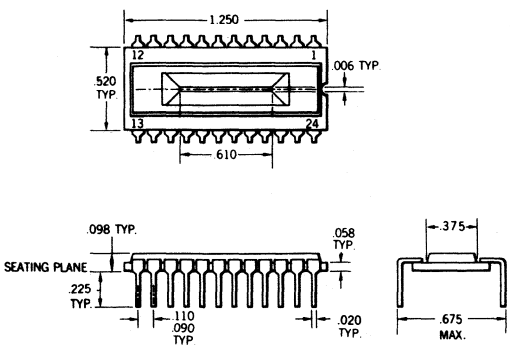
18-Pin Ceramic Dual In-line



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar

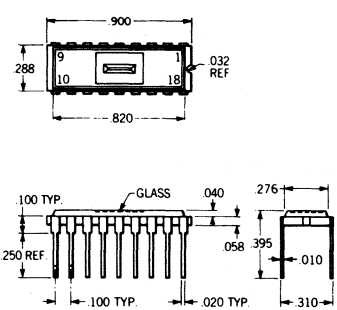
7E1

24-Pin Dual In-line Seated Glass Optical Window



7E2

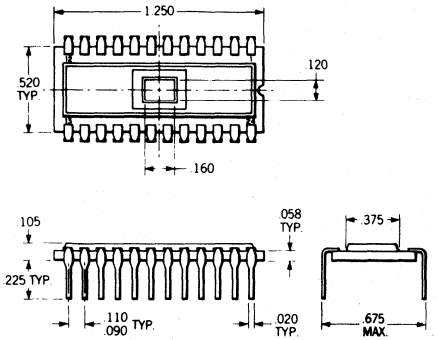
18-Pin Dual In-line Seated Glass Optical Window



PACKAGE OUTLINES

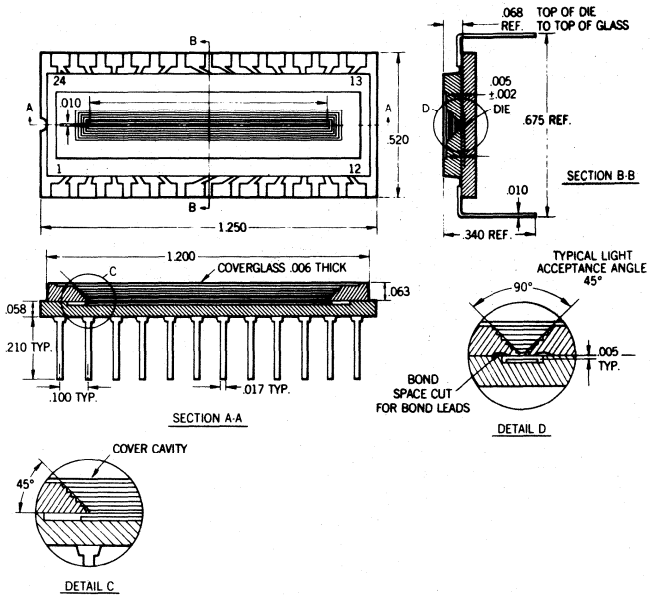
7E3

24-Pin Dual In-line
Seated Glass Optical Window



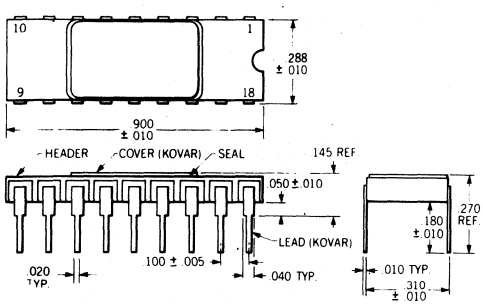
7E4

24-Pin Dual In-line
Seated Glass Optical Window



7E5

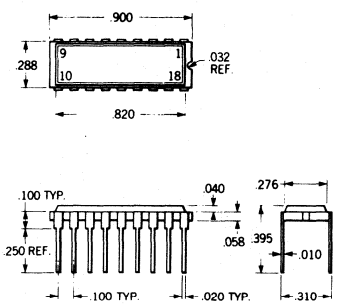
18-Pin Dual In-line
Seated Glass Optical Window
Side Brazed



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .300" centers
Pins are gold-plated kovar
Package weight is 1.4 grams

7E6

18-Pin Dual In-line
Seated Glass Optical Window
Side Brazed

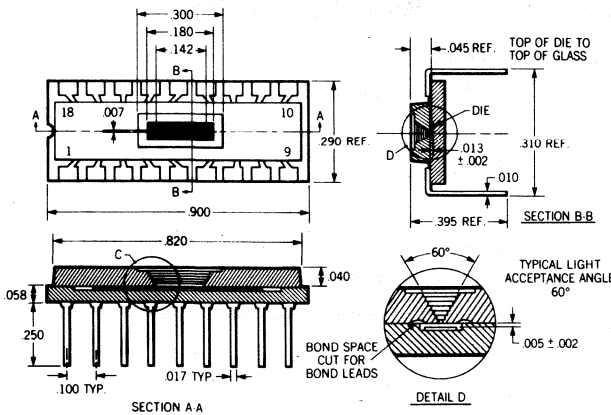


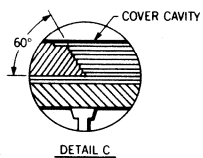
NOTES:
All dimensions in inches
Header is black ceramic (Al_2O_3)
Lid is plastic
Pins are gold-plated kovar

PACKAGE OUTLINES

7E7

24-Pin Dual In-line

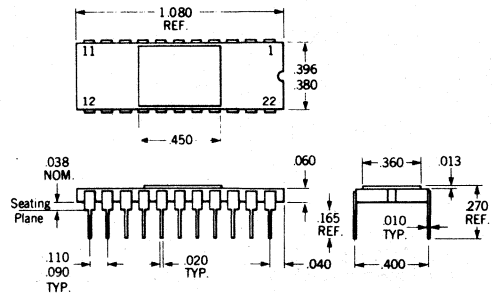




NOTES:
All dimensions in inches
Header is black ceramic (Al_2O_3)
Lid is plastic
Pins are gold-plated kovar
Transparent portion is glass
Photoelement No. 1 is at the end of the package with the notch

7E8

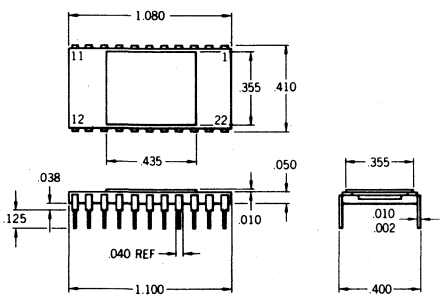
22-Pin Dual In-line Side Brazed



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .400" centers
Pins are gold-plated kovar
Package weight is 2.0 grams Typ.
Die mounting pad and cover both electrically connected to Pin 19 (Initial phototypes only)

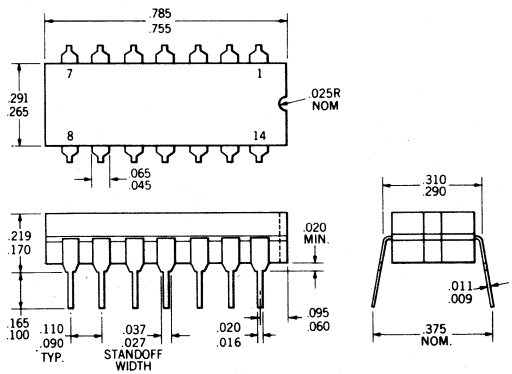
7I

22-Pin Dual In-line (Metal Cap)



7J

16-Pin MSI Dual In-line

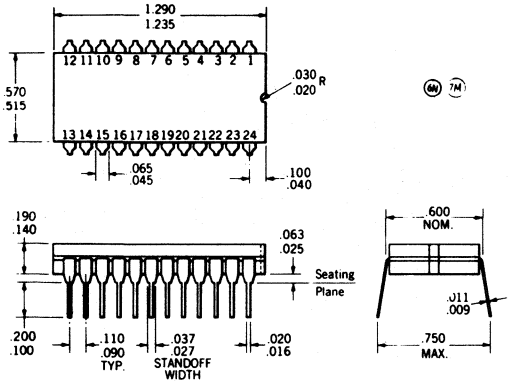


NOTES:
All dimensions in inches
Pins are tin-plated alloy-42
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Hermetically sealed alumina package
Cavity size is .130 x .230
*The .037/.027 dimension does not apply to the corner pins
Package weight is 2.2 grams

PACKAGE OUTLINES

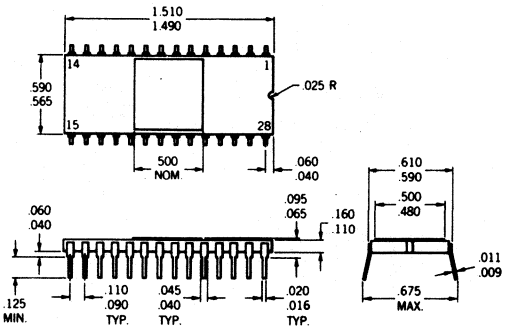
7M

24-Pin MSI Dual In-line



7Y

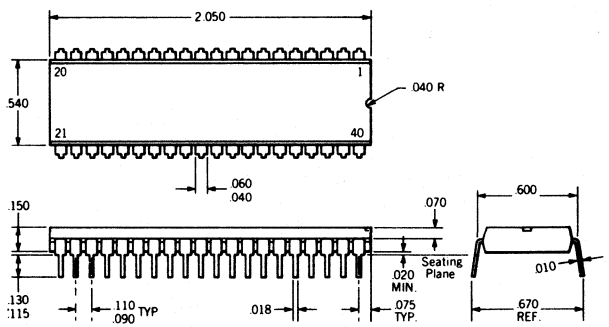
28-Pin Dual In-line Metal Cap, Side Brazed



NOTES:
All dimensions in inches
Pins are tin-plated alloy 42
Pins are intended for insertion in hole rows on .700" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 6.5 grams
Package material is alumina

8P

40-Pin Plastic Dip (Production Mold)

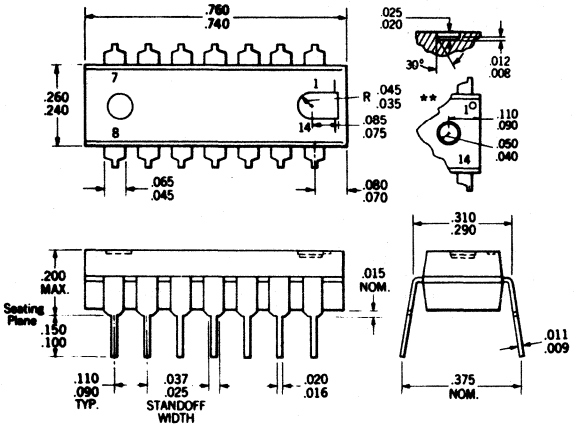


NOTES:
All dimensions in inches
Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on .600" centers
They are purposely shipped with "positive" misalignment to facilitate insertion

PACKAGE OUTLINES

14-Pin Plastic Dual In-line

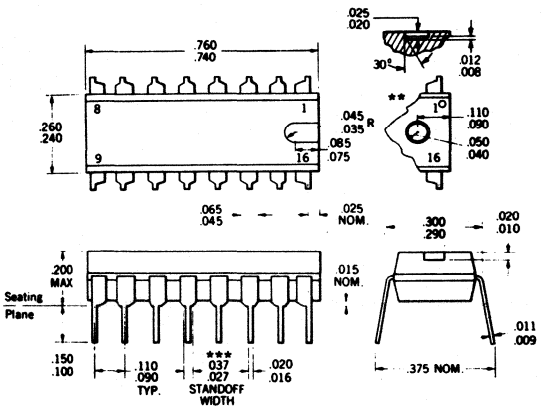
9A



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar
Package weight is 0.9 gram
Package material is silicone

16-Pin Plastic Dual In-line

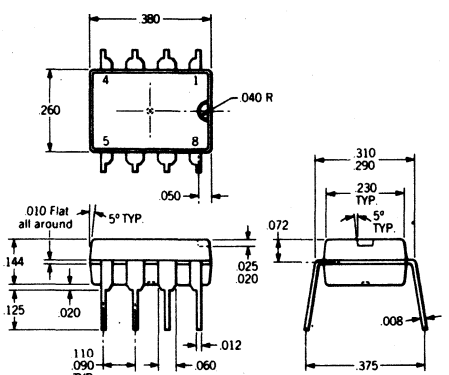
9B, 9R



NOTES:
All dimensions in inches
Pins are tin-plated kovar
*Package material varies depending on the product line
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
***The .037/.027 dimension does not apply to the corner pins
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 gram

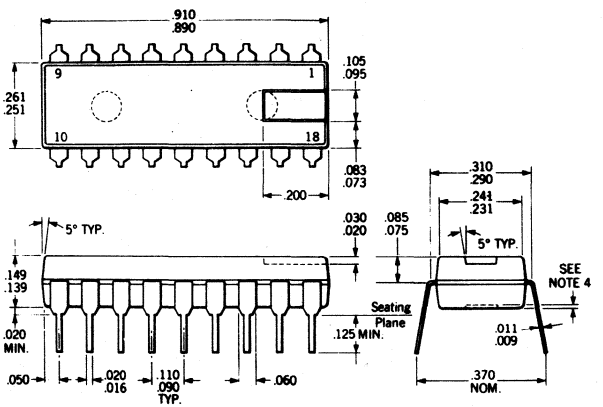
8-Pin Plastic Dual In-line

9L



18-Pin Plastic Dual In-line

9M

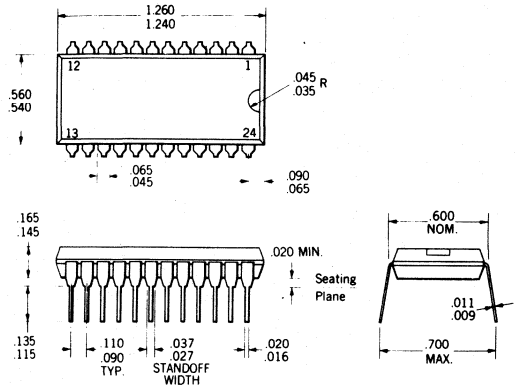


NOTES: All dimensions in inches
Pins are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar

PACKAGE OUTLINES

9N

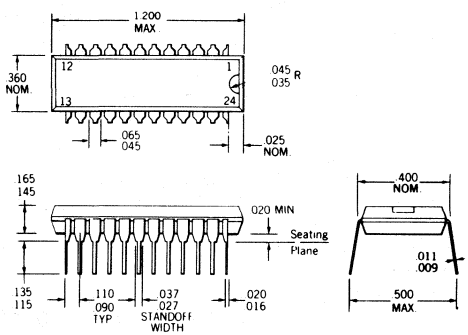
24-Pin Plastic MSI Dual In-line



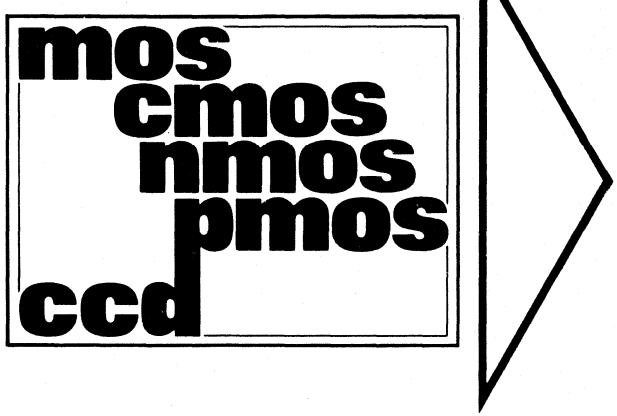
NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .700" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar

9U

24-Pin Plastic Dual In-line



NOTES:
All dimensions in inches
Pins are intended for insertion in hole rows on .500" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter pin
Pins are tin-plated kovar



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Printed in U.S.A./2020-12-0001-065/50M